Packaging Challenges for Emerging Semiconductor Technologies

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***Abstract*— As devices for quantum computing, AI hardware, power electronics, and magnetics mature enough to be commercialized, their unique packaging challenges must also be considered and solved. Advanced microelectronics technology platforms call for advanced packaging solutions, and these packages are not focused on traditional pitch scaling for high I/O count. Here, we discuss the distinctive packaging concerns around these emerging microelectronic devices, as well as avenues to address them.**

Keywords*— *microelectronics, quantum, superconductors, integrated photonics, magnetic memory, artificial intelligence hardware, power electronics, trapped ions

I. Introduction

While much of the semiconductor industry and attention to the microelectronics industry is focused on silicon-based transistors for logic and memory applications, other materials, device types, and chip architectures are leveraging the ecosystem. Recently, the United States Government decided to invest heavily in the semiconductor space through the CHIPS and Science Act, which primarily encourages domestic microelectronics manufacturing and advanced R&D. For their part, the Department of Defense stood up the "Microelectronics Commons", a network of eight regional innovation hubs working to accelerate the transition of microelectronics technology that are relevant to the DoD from the prototype stage to manufacturing relevance. The program looks to accelerate the "lab-to-fab" hurdle by leveraging the distributed expertise and capabilities within these hubs.

The Northeast Regional Defense Technology Hub, or "NORDTECH", is one of the eight Microelectronics Commons hubs that focuses on quantum devices, AI hardware, secure edge/IoT, and "commercial leap ahead" technologies (such as magnetics and power electronics). Starting in the second half of 2024, NORDTECH and the other seven hubs will begin executing projects in these kinds of technical areas with a focus on maturing DoD-relevant prototypes to a readiness level that would allow for commercialization. While much of the project work is around device design and process development for these unique technologies, eventually they need to be packaged into fieldable units.

Packaging, however, for these CMOS derivatives is not always as straightforward as packaging an advanced logic chip or even an application-specific IC. Maturing quantum systems from the lab into a commercial product, for example, requires the consideration of optical coupling and RF effects of the package. Chips with embedded magnetic materials need unique shielding, and power electronics require careful heat dissipation. Here, we will describe in brief the distinctive packaging needs for these emerging semiconductor technologies, as well as avenues to address these challenges. As the Microelectronics Commons projects progress, these open packaging questions should turn into resolved issues, paving the way for the commercialization of these technologies.

II. Quantum Technologies

Quantum computing promises to revolutionize the way we even think about computing, replacing the binary 1's and 0's (bits) with superpositions of 1's and 0's hosted in quantum bits (qubits). There are many different types of quantum computers that are under various states of development, and other quantum enabled devices like quantum sensors. Excellent review papers on the intricacies of different types of quantum platforms can be found elsewhere [1-3]. Here we will focus on the packaging challenges around quantum computers that rely on trapped ions, on entangled photonics, and on superconductors.

A. *Superconductors*

Superconducting quantum computers are a common type of quantum computer due to their development and commercialization by large technology companies like Google and IBM. These devices rely on the superconducting properties of materials when cooled to single digit or even fractions of a degree Kelvin.

State-of-the-art superconducting circuits conveniently operate within the 4-8 GHz range [4], ensuring that qubit frequencies remain compatible with conventional microwave components [5] as well as notably higher than thermal background at 10 mK. While the thermalization of qubits is a major topic in packaging superconducting qubits, the effective qubit temperature frequently reveals non-thermal noise sources dominating at low temperatures. Stray electric fields, magnetic fields, and noisy infrared photons can all pose a problem to superconducting circuits.

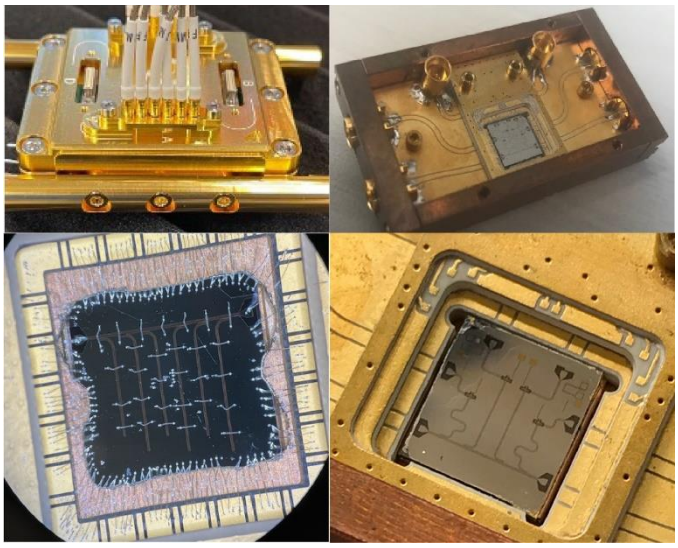

Fig. 1. Characterization of high coherent resonators at NYU using commercial sample holders as well as developing new low-cost qubit packaging solutions for the NORDTECH Hub. (J. Shabani, NYU)

To mitigate these sources of loss, it is important to incorporate electromagnetic shielding protection into sample packaging and low-temperature setup. These shielding mechanisms stabilize the environment of the qubit, more effectively isolating it from the surrounding environment. A typical and effective approach is to use a standard Faraday cage design as the first line of defense against stray electric fields and photons. While all Faraday cages operate on a similar principle it is important that the PCB packaging, chip attachment method, and shielding itself do not introduce extra losses into the device. For example, the qubit chips were traditionally adhered to the cavity using an acrylic adhesive. This polymer adhesive exhibits absorption in the microwave spectrum, contributing to considerable dielectric losses in addition to intrinsic qubit losses.

Sample packaging with a Faraday cage unintentionally creates a cavity box that can have non-zero coupling between the box and qubits [6]. Therefore, the sample holders must be engineered such that these box cavity modes are intentionally directed away from the chip, decreasing the coupling. This is achieved by suspending the chip, which removes the need of a ground plane directly below the chip. Without this, the ground plane would otherwise contribute to a high participation of the mode directly in the chip which in return increases the participation of the mode in the adhesive, increasing dielectric loss.

B. *Entangled Photons*

Quantum Photonic Integrated Circuits (QPICs) are playing a crucial role in advancing high-performance quantum information science for computing, communication, and sensing applications [6–11]. These integrated circuits combine all the necessary components for generating, manipulating, and detecting quantum states of light. The scalability of QPICs has facilitated quantum experiments integrating hundreds and even thousands of components [12–18]. Moreover, QPIC platforms are serving as interfaces with other qubit technologies, including defect centers [14], solid-state qubits [11,19,20], trapped-ions [21–25], and superconducting qubits [26,27]. The heterogeneous nature of QPICs, coupled with their demanding performance requirements, presents challenging packaging needs. Packaged QPICs must effectively control numerous components (Fig. 2) and meet the demands of applications spanning wide wavelength ranges (from UV to telecom), ultra-low loss optical fiber coupling, RF components, and, in many cases, harsh cryogenic or high vacuum environments.

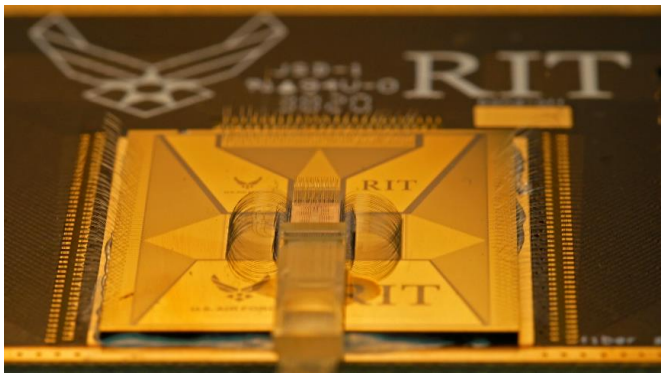

Fig. 2. Packaged quantum photonic processor QPIC with hundreds of electrical wirebonds and a fiber array attached to the QPIC. (S. Preble, RIT)

Ultra-low loss attachment of optical fibers to QPICs is one of the primary packaging needs. Any loss of single photons significantly impacts the performance of quantum systems, particularly those reliant on flying photonic qubits or quantum networks linking QPICs with other qubit types. To address this challenge, innovative methods for low-loss fiber packaging are under development. These include laser fusion splicing of fibers to undercut edge couplers [28,29], 3D printed mode couplers [30] and photonic wire bonds [31] (Fig. 3), along with the utilization of tapered optical fibers for evanescent coupling [32]. Fiber attachment techniques that are robust at UV-visible wavelengths (Fig. 3) with minimal fluorescence and loss are needed. Furthermore, the cryogenic operation is of critical importance as the best single photon detectors use superconducting materials and many of the qubit technologies

operate at cryogenic temperatures. There are promising reports of cryogenic-compatible fiber attachment using photonic wire bonds [33] or tapered-optical fibers [34], though further optimization of the materials and designs are needed to improve reliability and performance.

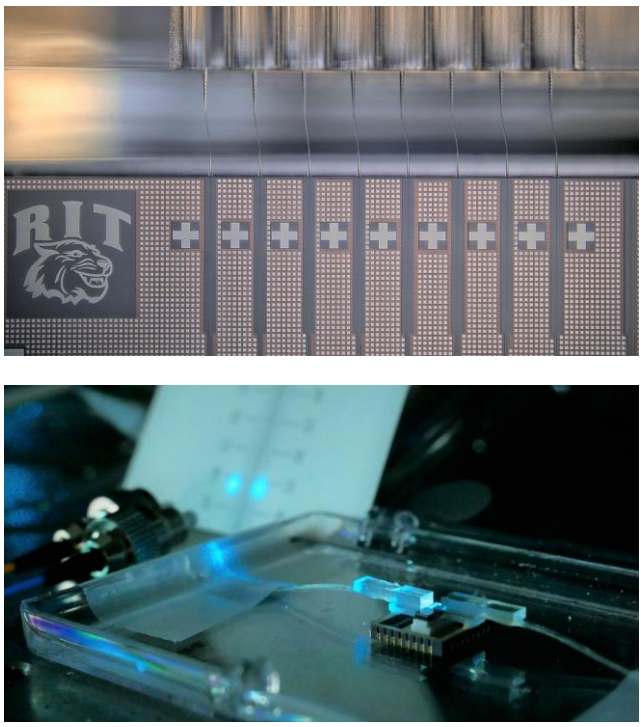

Fig. 3. Top: Fiber array attachment to a PIC using photonic wire bonds. Bottom: Packaged visible wavelength QPIC. (S. Preble, RIT)

Heterogeneous integration stands out as another crucial requirement for QPIC packaging. Semiconductor laser sources play a pivotal role in pumping QPIC photon sources [35,36], as well as facilitating other nonlinear interactions for quantum states of light [37–39]. Lasers are also required for controlling quantum emitters and trapped-ion qubits, necessitating the need for visible wavelength laser sources [40]. The QPIC platform is also being used for the hybrid integration of solid-state photonic qubits based on diamond membranes and III-V nanowires [41,42]. These materials are being transferred to QPICs using device-by-device pick-and-place techniques [11,43]. Micro-transfer printing is an emerging approach for heterogeneous integration that is compatible with wafer-scale integration [44], and has been employed for the transfer of lasers [45]. It has also been used to integrate quantum-dot single-photon sources on a CMOS silicon photonic chip [46] and is being used to integrate nonlinear materials, such as, lithium niobate on PICs [47].

Looking ahead, the QPIC community is going to continue to focus on lowering fiber-QPIC loss while increasing the density of fiber connections and operation in harsh environments. QPICs have greatly benefited from advancements in classical PIC hardware. Addressing the demanding challenges of QPIC packaging is likely to yield advances that can also greatly benefit classical technologies such as computing, artificial intelligence, and LiDAR.

C. Trapped Ions

Quantum information processing power in trapped ion systems has increased dramatically in recent years as the number of controllable, high-fidelity qubits continues to rise. For example, since mid-2020, trapped ion systems grew from a quantum volume of 64 (2^6) to over one million (2^20) while operating more than 30 qubits [48, 49], including the realization of a 32 qubit GHZ state [48]. The realization of high-fidelity entangling gates [50], along with error correction in logical qubits [51, 52], showcases the promise of this qubit platform.

As the number of trapped ion qubits increases, so too does the challenge of controlling large numbers of these qubits while maintaining high-fidelity gates. For example, the use of bulk optical components in state-of-the-art systems isn't feasible for delivering lasers to thousands of ions for individual control. Architectures to address huge numbers of ion qubits is needed, and developments in photonics chips offer promise to accomplish this [53-55]. Much like moving from hand-soldering circuit components to semiconductor fabrication of CPUs, the use of photonics chips should offer both scalability and increased performance for controlling trapped ion qubits [56].

Geometrical and optical constraints may limit further scaling of trapped ion systems, especially when performing multi-qubit entangling gates in systems with large numbers of qubits. Creating a quantum network of connected processors through photonic interconnects is a promising way to mitigate these limits on the number of qubits [57]. The speed of these interconnects has increased by many orders of magnitude [58, 59], and photonic chips offer a way to further increase the connection rate by creating multiplexed links between processors.

Lastly, advances in quantum transduction [60] and frequency conversion [61] offer promise to connect different types of qubits in a heterogeneous quantum network. This capability, leveraged through the use of photonics chips, could allow different types of qubits to specialize to different functions (ex: storage or high-speed processing), thus offering more architectural flexibility when scaling quantum information processors.

III. High Power Electronics

The field of high-power electronics today is increasingly dominated by the SiC and GaN material systems. Compared to conventional silicon field effect transistors, they can handle voltages of 1000V or more with switching speeds of a MHz or more [62,63]. More recently, these material systems have been leveraging the silicon semiconductor supply chain and expanding to larger wafer diameters.

SiC and GaN devices are able to operate in higher temperature regimes due to both self-heating and environmental effects. High-temperature packaging and thermal management materials, systems, and technologies are required to effectively dissipate the heat generated internally from active and passive components, in order to protect the critical parts. These packaging technologies must also be able to withstand high temperature environments. In the next 5-10 years significant gains will be essential with respect to these high-temperature (>

300 ºC) encapsulation materials having both high dielectric strength (30 kV/mm to 50 kV/mm) and low partial discharge (< 10 pC at recurring peak system voltages). In addition, there is a need for insulated metal substrates with improved insulator thermal conductivity (> 50 W/m-K) and low conductor sheet resistance (< 0.1 mΩ/sq). Finally, embedded cooling that is passive in nature and in close proximity to the power semiconductor devices will contribute to the overall solution.

Presently, dielectric performance within the package/modules is an issue beyond the 200-300 ºC range, as the insulating materials are unstable and exhibit degradation at high temperatures over extended periods of time. No functional power package/module can exist without reliable dielectrics acting as intended insulators. Ultimately, there remains a fundamental material problem, with a lack of extreme packaging materials that are both suitable for high temperature, high voltage, and high current packaging.

The lack of packaging materials for high temperature, high humidity, and high voltage is also a challenge. For example, availability of dielectric fluids with high conductivity and high flashpoint properties for use in multi-functional packaging architectures is highly limited. Also, due to the high frequency switching capability of WBG and UWBG power semiconductor devices, the series and parallel device integration remains a hurdle that must be overcome with impedance matching, static and dynamic circuit balancing, snubbing, thermal isolation, etc. within the packaging architecture.

Therefore, a lack of comprehensive device-level, converter-level and system-level design, simulation, and optimization tools are missing to be able to effectively overcome these detailed multi-physics circuit analysis issues. The interdisciplinary fashion of these issues is a significant hurdle in that this area crosses many materials fields, several electrical disciplines, mechanical design/modeling/thermal, and device physics. Co-design tools needed to couple electromagnetics and circuit designs with mechanical and materials opportunities to work on optimization are difficult or non-existent and need industry agreed upon data sets to support.

IV. AI HARDWARE

Generative AI and widespread automation demand technological advancements. These areas demand continued development in semiconductor core technologies including advanced GPU architectures, finer nodes of transistor, speed of data transfer, and memory bandwidth, which are essential for supporting the complex computations required by AI and other data-intensive applications.

In addition, the evolution of AI underscores the necessity for integrated hardware and software development. This integration ensures that advancements in semiconductor technology directly enhance software performance and capabilities, facilitating more sophisticated applications in artificial intelligence.

Of all the demanding requirements, the AI packaging must be accomplished in affordable cost and pricing. There are two types of AI packaging offerings. One is for high-performance computing (HPC) and the other is for commodity applications. Both offerings need to exercise innovative and aggressive adoption of the concept of heterogeneous integration for both technical and economic success.

Current technologies for HPC packaging for AI include subcomponents such as logic dies in a form factor of chiplets, HBMs, a Si or an organic interposer, possibly bridge dies and a high-density wiring substrate. To maximize the data transfer over short distances, the resulting package body size is getting bigger as a greater number of reticles are assembled in a single package. As of today, the package is expected to be as large as 100mm x 100mm. This causes serious challenges in package assembly and reliability issues. Also, the amount of power consumption is ever-increasing beyond the level conventional thermal management techniques can handle. Innovative packaging technologies including 3D packaging, advanced material development for effective heat transfer, and higher bandwidth communication schemes such as co-packaged optics (CPO) are highly sought after.

In the meantime, commodity applications are under the high pressure of lowering the cost while jamming more functions within a package. The higher level of heterogeneously integrated packaging technology is warranted. It means integration of digital and analog chips as well as sensors within a package to make a powerful yet cost-effective System in Package (SiP). Development and application of co-design tools that consider thermal, mechanical, and electrical aspects are highly needed.

V. MAGNETICS

Magnetoresistive Random Access Memory (MRAM) is a type of resistive memory in which the resistance state of the storage device is determined by the magnetic state of that device. Data is stored as a magnetic state and read by sensing the resistance. The magnetoresistive devices are integrated into the back-end-of-line (BEOL) process, between metal layers in the wafer fabrication process. MRAM technology is in production at leading semiconductor foundries around the world, mostly as an embedded nonvolatile memory (eNVM). Beginning at the 28 nm and 22 nm technology nodes, embedded MRAM is replacing embedded flash memory as the standard eNVM for a wide range of microcontrollers and other semiconductor chips [64].

To minimize error rates and maximize reliability, it is desirable to provide magnetic shielding in the package, with the MRAM-containing semiconductor chip, to protect the MRAM elements from external magnetic fields. A very simple shield, comprising a thin foil of an appropriate ferromagnetic alloy placed over the chip, can be very effective in canceling out magnetic fields directed parallel to the surface of the chip. Such shields are used in the production of first-generation MRAM, which employs magnetic tunnel junction (MTJ) storage devices that are magnetized in the film plane. The current generation of MRAM, based on perpendicularly-magnetized MTJs, is much less sensitive to external fields because of the strong magnetic anisotropy engineered into the MTJ devices, but it has some sensitivity to both the in-plane and perpendicular components of external magnetic fields. A simple, low-cost shielding solution to protect MRAM devices from perpendicular and in-plane magnetic field components would be very valuable for more

harsh environments where high external magnetic fields are expected [65].

Proposed solutions for shielding against perpendicular fields are generally in the form of metal shielding that surrounds the chip above, below, and to some degree from the sides [66]. This can be expensive and complicated to implement in high-volume manufacturing, and therefore considered only for certain specialized applications. A low-cost shielding scheme that can cancel both in-plane and perpendicular magnetic fields would be a breakthrough for extending embedded MRAM to the most demanding applications in industry, automotive, military, and aerospace products. The need for such shielding is increasing with time as embedded flash is not expected to be available in technology nodes beyond 28nm, driving demand for embedded MRAM in high-volume products [67].

VI. Conclusion

While all are based on decades-old semiconductor wafer processing, the cutting-edge technologies described above enable radically new and different types of computing or information processing. In order to field, commercialize or increase the impact of microchips that leverage magnetics, light, quantum physics or novel materials, appropriate advancements in packaging technology must be developed in parallel. The promise of these novel microelectronic components is massive, and the combined expertise of academia with public and private research labs is required to enable them. In part, the recent transformational investments in microelectronics enable heightened focus and process development through initiatives such as the Microelectronics Commons and its hubs like NORDTECH.

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