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Bridge-chip Interconnect Technologies

In recent years, the field of packaging has taken center stage as the semiconductor industry pursues ever more energy efficient, high-performance, and low-cost electronic systems. While the field of packaging is undergoing revolutionary technology advances today, there is little doubt that packaging in the new era of Moore's Law will offer extreme levels of die integration/bonding and begin to blur the boundary between on- and off-chip connectivity (especially in 3D architectures) due to ever denser physical I/O interfaces/bonds. This new form of 'packaging' is often referred to as 'Heterogeneous Integration' or HI today. A common goal for HI is to enable the interconnection of multiple dice (or "chiplets") of various functionalities in a manner that approaches monolithic-like performance yet utilizes advanced off-chip interconnects and packaging/assembly to provide flexibility in IC fabrication and design, improved scalability, reduced development time, and reduced cost. In fact, a cost-benefit analysis of monolithic die disaggregation was recently performed at the 3 nm node and showed that chiplets become cost competitive when monolithic die size exceeds 150 mm^2 due to yield considerations of larger monolithic die [1].

In this article, we focus on bridge-chip based 2.5D heterogeneous integration technologies, which have recently emerged as critical enablers for energy-efficient and high-bandwidth density signaling. The key drivers for bridge-chip based 2.5D integration include: 1) ability to provide physically-short and high-density interconnects locally between adjacent die that otherwise would communicate using 'coarse pitch' interconnects on an organic package (most commonly); 2) ability to scale package-substrate footprint containing high-density local interconnects beyond what could be accomplished using silicon interposer technology (which is typically limited to reticle size) and potentially at lower cost; and 3) in some applications, bridge-chips do not require TSVs, and thus, may provide a more effective pathway to heterogeneous integration than silicon interposer technology as well as reduced electrical parasitics. 2.5D bridge-chip based HI has been pursued by several institutions, including Sun Microsystems [2-3], Oracle Labs [4-7], Intel [8-9], imec [10-11], IBM [12], AMD [13], TSMC [14-15], and Georgia Tech [16-21]. A thorough review of these technologies is beyond the scope of this article. However, some of the key considerations for these bridge-chip based 2.5D technologies include: 1) the I/O interconnect densities possible between the assembled-chiplets and the bridge-chips, 2) the electrical performance of the bridge-chip links, 3) the manufacturing process for bridge chip bonding and integration with chiplets , 4) the flexibility/ability to mix-and-match different bridge-chip functions and technologies within the same package, 5) whether bridge-chip integration impacts the package substrate fabrication (i.e., making cavities in the package to receive the bridge-chips), and 6) how scalable (i.e., large-of-a-package) is the technology, among a few others.

At the Georgia Tech Integrated 3D Systems Lab (i3DS), several bridge-chip based technologies have been pursued. Some of our initial work focused on bridging two large-chips or silicon interposers (Figure 1) [16]. Silicon interposer size is limited by both technical and economical constraints, and in turn, ultimately limits the size and the number of chips that can be assembled. This presents a critical limiter to high-performance and energy efficient electronics as the interconnect benefits become limited to the

footprint of the interposer. Eventually, multiple interposers may become necessary and high-bandwidth interconnections between individual interposers will become vital in providing a contiguous large-scale and low-cost silicon interconnected system. To this end, we demonstrated a large-scale silicon platform consisting of multiple interposer tiles, which are essentially silicon interposers, that are assembled directly on the printed wiring board (PWB) in a tile-like pattern. Electrical interconnections between the tiles are provided through silicon bridges, which are mounted on top and span two or more interposer tiles. The tiles and the bridges are electrically interconnected using high-density mechanically flexible interconnects (MFIs), which are developed to allow repeatable (for rework) and low resistance contact with electrical pads. Positive self-alignment structures (PSAS) and inverted pyramid pits passively self-align the interposer tiles with the FR4 PWB and the interposer tiles with the silicon bridges without the use of high-alignment accuracy and low-throughput flip-chip bonders. Thus, the key features of this demonstration are: 1) micron-scale accurate alignment of interposer tiles, bridges, and PWB using passive techniques enabled through microfabricated PSAS-pits technology and 2) dense electrical interconnectivity among interposer tiles through the silicon bridges (i.e., bypassing the low-density and lossy interconnects on the PWB). Ability to integrate silicon photonics within the bridge-chips was also explored.

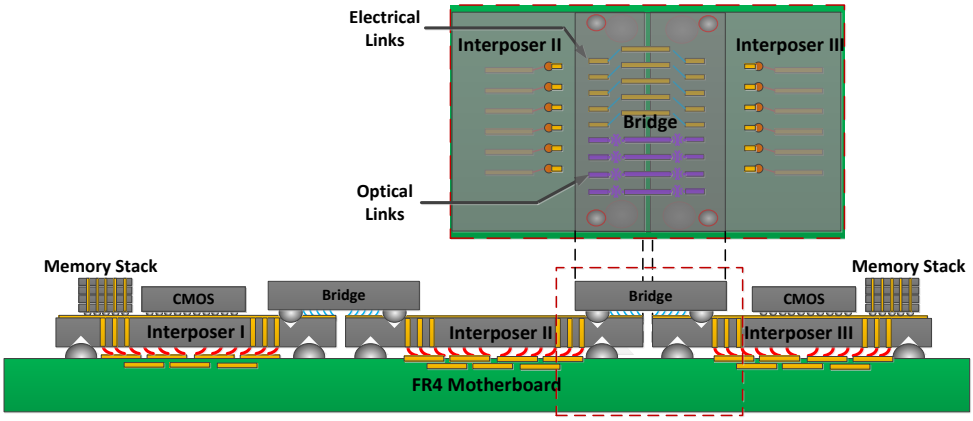

Figure 1: Interposer-to-interposer electrical and photonic interconnection using silicon bridges; the interposers are assumed to be reticle size limited. The bridge-chips provide high-density electrical and photonic connectivity between adjacent interposers

We have also explored the bridging of electronic chiplets using electrical and photonic 'stitch-chips' using Heterogeneous Interconnect Stitching Technology (HIST) [17-21]. A stitch-chip, in the simplest application, provides high-density and energy efficient, fine pitch wires and is placed between the package substrate and the chiplets (Figure 2). In one demonstration, fine-pitch microbumps were used to bond chiplets to the stitch chip to provide high-bandwidth density interconnects [17]. In another demonstration, compressible microinterconnects (CMIs) were also used for the assembly to compensate for package nonplanarity resulting from non-uniform height stitch-chips, on the same package, as the stitch-chips may be fabricated on different substrate materials (for example, silicon and glass) and sourced from different foundries when they provide different functions across a package [18-20]. CMIs are pressure-contact based interconnects designed to interface with a pad on the package substrate. They allow rework, which becomes important as the number of chiplets per package increases; it is possible for the package yield to drop as the number of chiplets with fine-pitch I/O increases. Photonic chiplet integration within HIST has also been explored with focus on fiber-to-stitch-chip self-alignment and interconnection (Figure 3) [21]; specifically, a passive fiber-array alignment and assembly approach

using Fiber-Interconnect Silicon Chiplet Technology (FISCT) was developed. FISCT consists of two key elements: 1) a silicon chiplet carrier with integrated lithographically defined mechanical self-aligning features and through-vias, and 2) 3D printed fiber ferrules that reside within the vias of the silicon carrier. FISCT enables massive precision self-alignment and assembly of optical fibers onto a package substrate or a photonic chiplet, and it is compatible with flip-chip bonding technology. In essence, FISCT is a chiplet that provides passive and precise mechanical self-alignment between a high-density fiber optical array and photonic ICs.

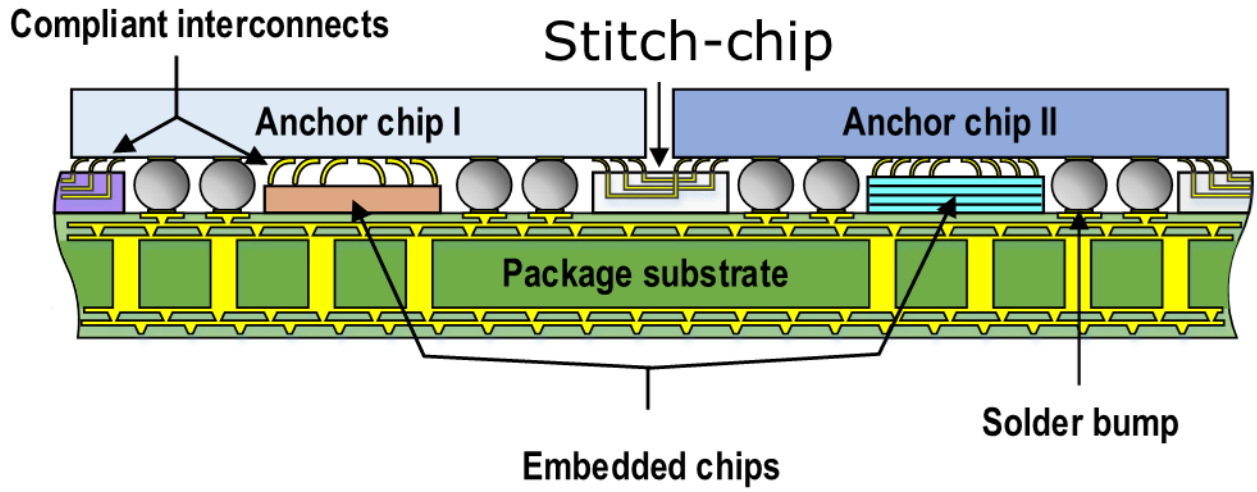

Figure 2: Stitch-chip technology for die-to-die dense interconnection

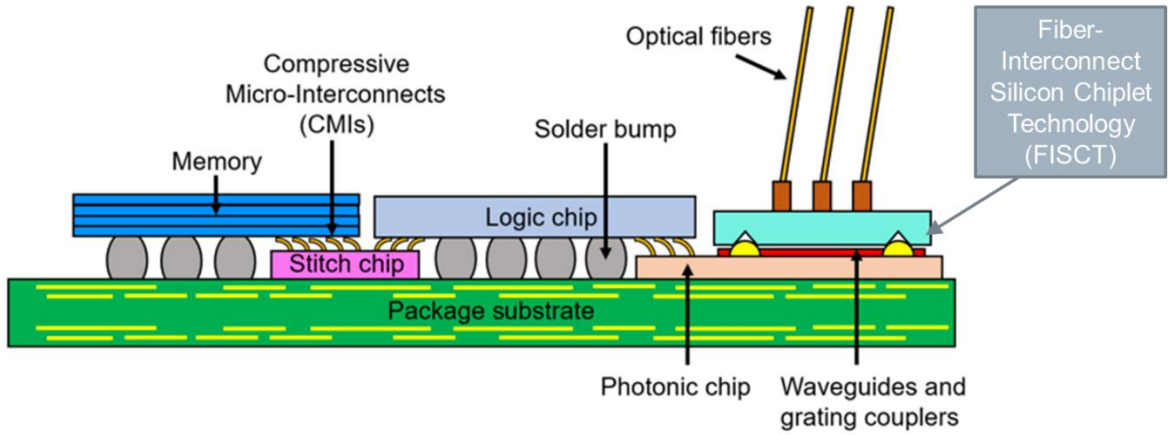

Figure 3: Photonic stitch-chips with Fiber-Interconnect Silicon Chiplet Technology (FISCT)

In pursuit of a reworkable high-density chiplet integration platform, a rePlaceable, INtegrated CHiplet (PINCH) assembly, as seen in Figure 4, was recently developed. As the number of chiplets with fine-pitch I/Os in a package increase, the need for rework becomes increasingly valuable. This necessitates the need for high-density I/Os and assembly methods that allow rework. To address this need, PINCH achieves a nonpermanent off-chip interconnection system via CMIs, which have been demonstrated to scale down to 30-μm pitch, and a nonpermanent self-alignment technology via PSAS-to-PSAS self-alignment [16]. These enabling technologies can be seen within the PINCH assembly in Figures 4 and 5.

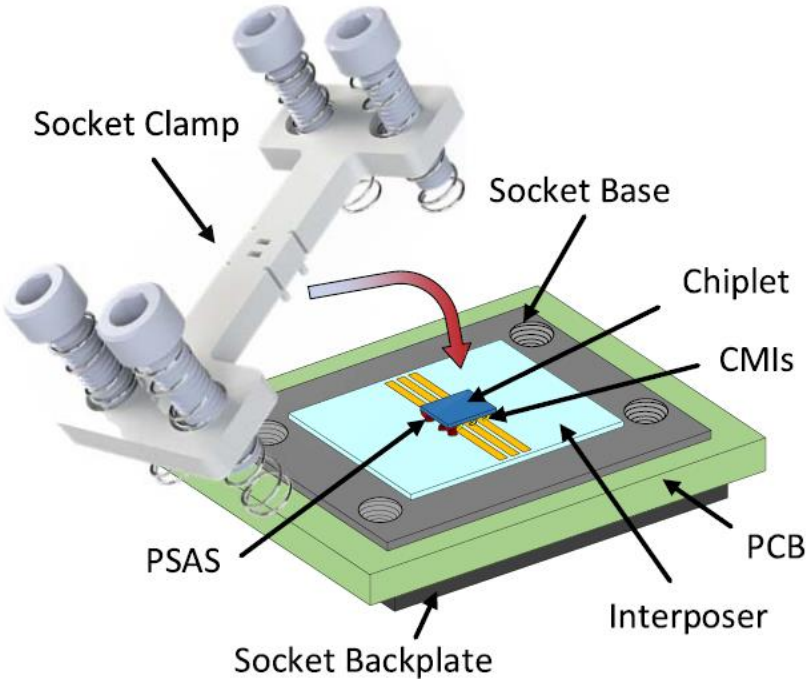

Figure 4: PINCH assembly for chiplets

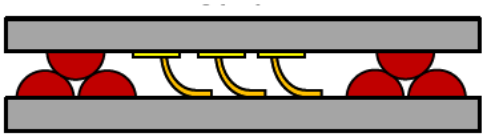
Figure 5: Self-alignment using PSAS-to-PSAS and electrical interconnection using CMIs

Lastly, beyond bridge-chip 2.5D technologies, a heterogeneous integration technology called 3D Integrated Chiplet-Encapsulation (3D ICE) was recently developed. The 3D ICE concept is illustrated in Figure 6. Multiple chiplets are encapsulated by low-temperature inductively coupled plasma-enhanced chemical vapor deposition (ICP-PECVD) of SiO_2 resulting in an SiO_2-reconstituted-tier. This SiO_2-reconstituted-tier is then post-processed with through-oxide-vias (TOVs) to enable dense vertical integration (compared to conventional FOWLP), Cu redistribution layers for fine-pitch lateral interconnections and Cu pads for bonding. Finally, the SiO_2-reconstituted-tier can be transferred and bonded to a silicon wafer. All processes can be accomplished using wafer-level processing, which improves fabrication throughput and alignment accuracy between stacked tiers as well as within-tier alignment as no curing (and thus shrinkage) of the SiO_2 film is used in contrast to FOWLP molds. Figure 7 shows a "Sea of Chiplets" within an ICP-PECVD SiO_2 reconstituted tier; smallest silicon chiplet in the reconstituted tier is 10x10 μm.

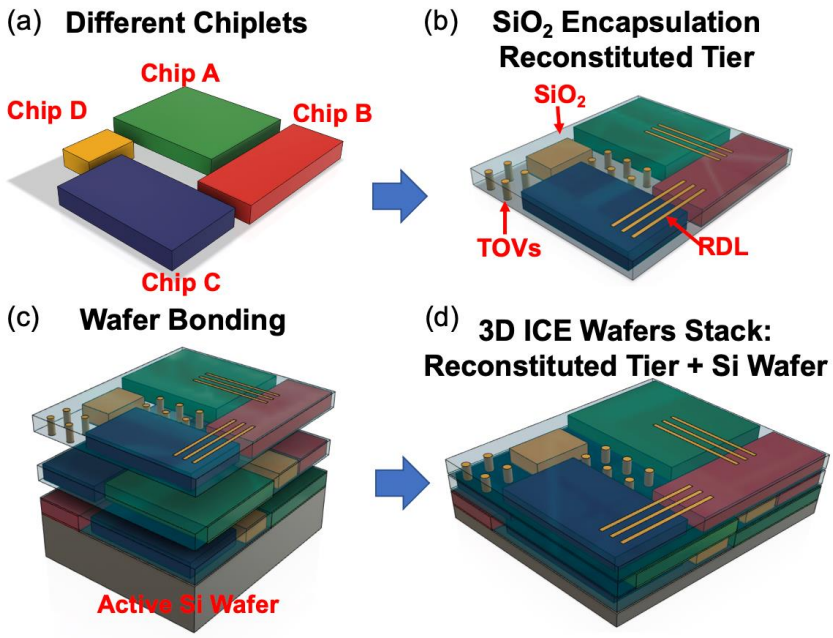

Figure 6: Chiplet reconstituted wafer process and stacking.

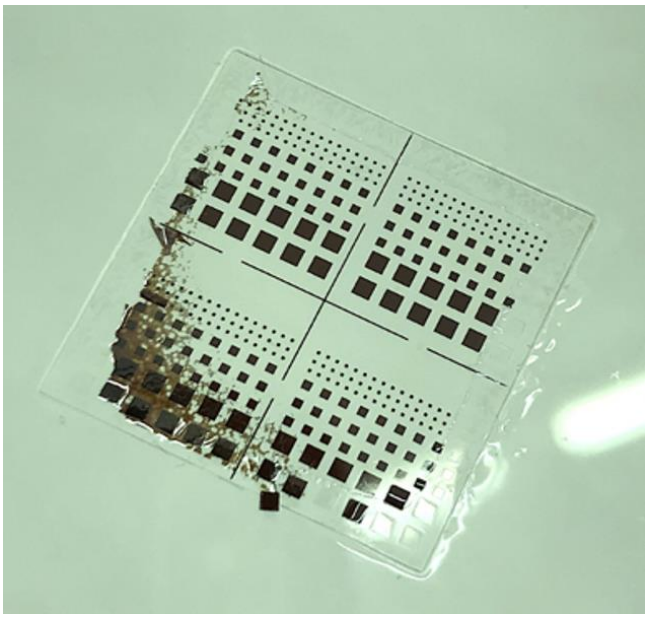

Figure 7: "Sea of Chiplets" within an SiO_2 reconstituted tier.

In summary, heterogenous integration has emerged a key enabler for the next phase of Moore's Law due to the high energy efficiency and high-bandwidth density interconnects such platforms provide [24]; the I/O pitch in some such platforms has already been demonstrated at the few-micron scale. While this article reported some of the technology options for bridge-chip based 2.5D technologies, thermal [25-26] and power delivery [27] designs in such chiplet integration architectures present unique challenges and opportunities; such a discussion is beyond the scope of this article.

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Biography

Muhannad S. Bakir is the Dan Fielder Professor in the School of Electrical and Computer Engineering at Georgia Tech. His areas of interest include 2.5D and 3D heterogeneous integration technologies, photonic interconnect networks and co-packaging, embedded cooling and power delivery for emerging heterogeneous integration architectures, and flexible electronics for healthcare. Dr. Bakir and his research group have received more than thirty paper and presentation awards including six from the IEEE Electronic Components and Technology Conference (ECTC), four from the IEEE

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In 2020, Dr. Bakir was the recipient of the Georgia Tech Outstanding Doctoral Thesis Advisor Award. He is also the recipient of several teaching awards, including the 2014 and 2015 Georgia Institute of Technology Class of 1940 Course Survey Teaching Effectiveness Award, and the 2020 Student Recognition of Excellence in Teaching: Class of 1934 Award.