3D PEIM Conference Reveals the Five "M"s in Power Electronics

Multiscale, Multiphysics, Modeling, Materials and Manufacturing

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The 3D Power Electronics Integration and Manufacturing (3D PEIM 2023) conference highlighted the need for multiscale multiphysics modeling to design for advanced topologies and architectures, coupled with innovations in materials and manufacturing to reliability for emerging computing, communication and automotive markets. This article points to selected key fundamental technology take-home lessons from the 3D PEIM conference held in FIU, Miami in February 2023.

The 3D Power Electronics Integration and Manufacturing Symposium, chaired by Markondeya Raj Pulugurtha, FIU was held from February 1-3, 2023 and hosted by Florida International University (FIU), in Miami, Florida. The Symposium is financially sponsored by Power Source and Manufacturing Association (PSMA) and technically sponsored by the IEEE Electronic Packaging Society (EPS) and Florida International University. The sponsor Chair, Devarajan Balaraman (Wolfspeed) engaged with seven Partner/Exhibitors: Amkor Technology, FIU Biomedical Engineering, KEMET a YAGEO Company, Wolfspeed, Indium Corp and Carbice, who also contributed to the success of the event. The workshop technical program was led by technical co-Chairman John Bultitude, KEMET, A Yageo Company, and Vanessa Smet, Georgia Tech. The Symposium focused on multiscale power electronics and addressing its key challenges through Multiphysics modeling coupled with emerging topologies and architectures, materials, integration and manufacturing to create state of the are power systems. The sessions were organized to provide technology updates for design, packaging, and manufacturing engineers and others engaged in research and the applications of materials, components, manufacturing, and qualification of power sources. This was through comprehensive technical sessions on advanced topologies, die-attach materials and advanced dielectrics from polymers to nanocomposites, WBG materials, active and passive components and 3D packaging, where several breakthrough technologies are presented and discussed. There were many excellent presentations in all themes related to power electronics. This article highlights a few technical take-home lessons.

FIU Graham Conference Center hosted the 3D PEIM 2023

3D-PEIM 2023 was a Hybrid Workshop with 95 in person attendees/speakers and 5 virtual speakers. The attendees and contributors represented 8 countries and came from industry, academia, and government. They were treated to 3 information packed days of 42 presentations (7 Plenary, 15 Keynote and 20 invited/submitted) with 7 posters. The in-person attendees were treated to a lab tour of FIU Electrical Engineering. The workshop consisted of many excellent presentations. The program opened with a welcome to FIU by John Volakis, Dean of the College of Engineering and Computing giving us a warm welcome and hints on the hot spots in Miami.

Vertical power delivery in high-performance computing with advanced topologies, minimum interconnect path, and high-density storage components are the need of the hour. This has been emphasized multiple times in the session on Integrated Power Delivery, cochaired by Siddharth Ravichandran from Chipletz. Plenary Speaker, Madhavan Swaminathan, Pennsylvania State University, presented the needs and challenges in integrated power delivery for future AI computing with a 10X increase in computing demand every year. In spite of the 2X increase in process gains and 3X architecture gains, the 300X scaling of systems is projected to lead to an energy crisis. Proliferation of on-die power domains will demand more fine-grain power management, as presented by Michael Hill from Intel. With this approach, the performance of each IC domain or core can be independently optimized with its separate independent power supply. There is an imminent need to reduce copper losses by getting higher voltages to the Integrated Voltage Regulator (IVR) and CPU chip stack. Mother board VR capacity is reduced and efficiency is enhanced through this approach. Vertical power delivery with integrated voltage conversion and regulation is the ideal approach to reduce power conversion losses. One key 3D IC architecture to realize vertical power delivery is to have backside power routing after the wafer is grinded to eliminate the silicon substrate parasitics and additional thickness. This requires a major increase in storage components such as inductors and capacitors.

Mahadevan Iyer, Amkor, presented on automotive packaging and accelerated adoption of advanced packages. Although presentations were live, recordings were also provided to all registrants later.

The higher voltage conversion ratios in the package has been driving new topologies for efficient power delivery. With package conversion from 48 to 1 V, multiple topologies are considered to meet the required regulation, efficiency and power density. These include single-stage, multistage and stacked power architectures, which are summarized in the keynote talk by Minjie Chen of Princeton University. In multistage conversion, regulation is performed at the final stage while intermediate stages are mostly dedicated to

DC conversion. One such architecture is based on the stacked switched capacitor network at the high-voltage end, followed by multiphase buck with coupled inductors. Another topology comprises of high-voltage (front-end) switched capacitors that are linked to the back-end switched capacitors through inductor links. This drove the innovation towards innovative vertical coupled inductor topologies presented by Daniel Zhou and Mian Liao from Princeton University.

Embedding technologies in high-volume manufacturing for realizing 3D power delivery were described in the subsequent keynote paper by Vikas Gupta from ASE. His talk highlighted ASE's innovations in vertical power delivery with embedded power components in advanced substrates, while emphasizing the need for shorter time to market. The key performance metrics such as shorter transmission path and better thermal dissipation are also highlighted with their semiconductor embedding in substrates and doubleside SIP.

Plenary Speaker Rao Tummala, 3D Electronics Systems Packaging Research Center gave an intriguing look into the future proposing that by 2040 computing speed would increase 1 million times and industry wants to power that capability with power sources the same size and cost as today. He and other speakers emphasized that the new Moore's law will only be possible when system components, and packaging keeps pace with chiplet integration. Keynote speakers Matt Kelly, IPC and Charles Woychik, Skywater reminded us that substrate advancement is key to this continuous size reduction, and government funding is needed to insure the substrate and packaging receives the same investment as chips.

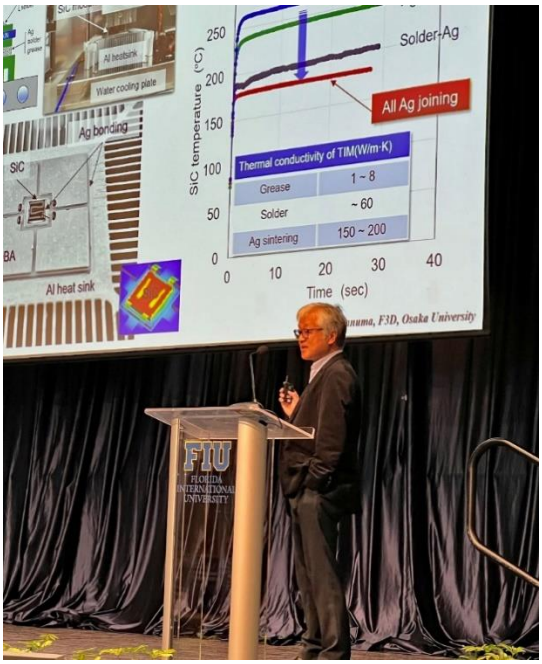
Automotive Power Packaging with 3D: The automotive session was led by a plenary talk from Mahadevan Iyer, Amkor on power packaging advances in automotive products. Amkor's pioneering advances in WBG semiconductor packaging, sintering die-attach materials, clip bonding for low inductance and high current density, doubleside cooling, stacked and embedded vertical packaging and associated material and design advances were presented. These are being applied to various power architecture stages such as power block (switches), power stage (switches with controller) and power module (switches, IC and passives). The poster presentation by Rando Raßmann from University of Applied Science, Kiel provided an extensive study on several 3D power packaging variants with WBG and driver chips for fast switching. The gate driver and sensor source signals, gate path and source path can be intelligently routed in different layers to effectively suppress the parasitic inductances and voltage ringing noise. The benefits of 3D packaging in simplified routing options for driver signals was presented.

Multiphysics simulations and predictive modeling: Heterogeneous Integration comes with Multiphysics problems that demand a holistic approach for manufacturing and reliability. The talks from the Multiphysics session, chaired by Rajen Murugan, Texas Instruments, brings out various scenarios where Multiphysics analysis brings out the failure modes that trigger from escalating power densities with vertical chip stacking in power packages. While we get high power densities with increasing switching frequency, reduced conduction and switching losses, and 3D packaging, they also increase the junction temperature and the associated electrothermal issues. The heat transfer coefficients for various convection conditions need to be extracted for accurate modeling. Validation is emphasized through measurements with a valuable lesson from Murugun's presentation that the junction temperature can be estimated simply from the case temperature by appropriate linear relationships. The importance of nonlinear coupled field problems is also emphasized. The trend of extending Multiphysics simulations towards other system metrics such as EMI compatibility by utilizing innovative polymer-graphene or copper-graphene composites was discussed by Ghaleb Al Duhni (FIU).

The plenary talk from Brandom Passmore set the stage for the whole conference by starting with the FEM predictions of solder joint reliability for realistic power package architectures. Such models become increasingly important to minimize over-design, reduce product cost, accelerate time to qualify the product, and to quantify the importance of material and geometry on the package performance. Audience walked away with key lessons on extracting total strain range, sensitivity analysis with key parameters such as bondline, substrate and copper thicknesses. In one interesting take-home message scenario, the correlation between the Rjc and number of thermal cycles was effectively used to estimate the thermal delamination.

The role of Machine Learning in bringing these system-level challenges such as “package inductance and capacitance on device parasitics through increased di/dt and dV/dt”, “thermal densification, and near-junction cooling” was comprehensive covered in the keynote talk by Vanessa Smet from Georgia Tech. System performance parameters such as junction temperature, package inductance, interfacial joint straints etc. are effectively optimized under various constraints such as volume, architecture, material selection, geometry using ML and post-optimization techniques. The importance of radial visualization techniques and Pareto fronts was demonstrated to see the correlation between “cooling footprint, area and junction temperature”, “parasitic inductance and junction temperature” and other system performance metrics.

Advancing WBG devices: The hottest overall topic was how to create new packaging concepts to accommodate the demand for higher power density power sources with low parasitics using wide bandgap semiconductors to reduce size (or keep the size the same but increase power output) and increase efficiency. The audience engaged in lively conversations on how to unite the progress in semiconductor fabrication, optimal packaging including substrates and passives, combined with state-of the-art modeling and testing to achieve the next generation power sources. NRL’s talk by Travis Anderson revealed the breadth of emerging materials from silicon to diamond. Semiconductor devices on WBG and UWBG circuit breakers (or limiters of fault current) that can turn off MW systems at faster time scale, vertical GaN, integration of nanocrystalline diamond for thermal management, optical isolation of the gate driver from the switch with photoconductive switches



Katsuaki Suganuma, Osaka University presents a plenary talk on sinter joining and lifetime prediction.

Embedding planar inductors and capacitors (storage components): The technical session on embedded passives, reminded us that without shrinking magnetics and capacitors, power sources would not be able to keep pace with shrinking packages. High power and high conversion ratio conversion is often based on inductor-based topologies. Noah Strucken, Ferric Inc. and Matt Wilkowski, Enachip, presented solutions for integrating and packaging inductors. The talks led to key discussions on the pros and cons for on-chip sputtered magnetics Vs plated magnetics. The properties of

sputtered magnetics have always been superior with their low coercvity, stable properties and higher permeabilty over broad frequency range. Plated magnetics enjoy higher throughput at lower cost. Enachip presented their innovation on creating wafer-plated magnetics with superior frequency stability with a unique sequentially-electroplated metal-polymer layered structures. Plenary Speaker, Fred Lee from Virginia Tech introduced the possibility of integrating inductors in PCB's at power levels up to 9 kW for increased efficiency and cost reduction. In the realm of capacitors, significant break throughs in capacitor size for embedding in PCB's were highlighted by Mohamed Jatlaoui, Murata introducing a 1 μF 0404 chip capacitor only 50μm high. B. K. Summey, KEMET, described circuit board packaging technology for embedding aluminum foil capacitor passives and a commitment to increasing the capacitance of an 0402 package by 2X-3X. Louise Duker, SMOLTEK announced a partnership with KEMET to bring ultrathin carbon nanofiber capacitors to market starting with samples of 0402's less than 100 μm thick in 2023.

An innovative advance in cold-sprayed Aluminum capacitors was presented by Reshmi Banerjee (FIU) towards integrating DC link and Snubber capacitors in package aluminum and copper leadframes and busbars. Cold-spray is an additive manufacturing approach to create porous aluminum on most metal structures and allows for easy integration of high-density and high-voltage capacitors in power packages.

Material and Manufacturing Technologies: As you would expect in this manufacturing conference, the material session (cochaired by Ninad Shahane, currently at Apple Inc.) was loaded with extensive information on advances in copper and silver sintering, die-attach reliability, 3D power packaging architectures and advances, all the way from fundamentals to system reliability. Christina DiMarino from Virginia Tech presented on substrate technologies for medium-voltage SiC modules. Various options such as PCB embedding, stacked substrates, Insulated-metal substrates (IMS) were comprehensively compared in terms of their advantages and specific limitations. Parametric electrothermal modeling and experimental validation was discussed to reduce the thermal resistance, common mode current and nonlinear field concentration at the triple points. Gordon Elgar (Technische Hochschule Ingolstadt, Ingolstadt) provided a comprehensive benchmarking of their innovative copper sintering with state-of-the-art technologies in terms of sintering pressure, temperature, time and the final bonding strength. An innovative in situ nanoparticle generation from copper salt during sintering was shown to provide unique benefits towards copper die-attach. Innovative copper and brass flakes were also described in his presentation.

Along with doubleside cooling and sintered die-attach materials, a new strategy to enhance power module packaging was presented by GQ Lu (Virginia Tech) on lowering the field gradients and increasing the pulse discharge insulation voltage. This was achieved with unique nonlinear resistive materials that are based on polymer nanocomposites. When coated on trenches or tripled points in DBC substrates, these materials showed 100% improvement in the PDIV. The role of additive manufacturing in integrating these wide variety of materials is covered in a comprehensive talk from Fraunhofer ENAS and ZfM at TU Chemitz by Frank Roscher. Versatile functionalization options using a combination of aerosol and inket printing, CW laser, IR sintering of metal, UV curing of polymer, pick-and-place and thermal camera are now available with 3D printing.

Power harvesting and telemetry solutions at multiscale: The conference committee was intentional in covering the latest advances in power harvesting and power telemetry. This session kicked off with an exciting overview from Brian Zahnstecher, PowerRox, on the wide variety of applications such as predictive maintenance, remote control, medical to industry conditional monitoring and most importantly

for the whole future IoT ecosystem. Several key innovations were discussed. One such breakthrough 3D power harvesting technology at large laminate scale was presented by Jorge Capridis (FIU). This approach integrated solar cells in the top, thermoelectric generators on the backside and RF harvesting with linear antenna arrays on the side. The whole trimodal power harvesting system was integrated in a laminate package with standard substrate manufacturing techniques, making it a scalable solution. The other innovation from Veeru Jaiswal at FIU highlights multiferroic power telemetry as an innovative way to delivery power at small scale. These multiferroic substrates are copackaged with rectifier and storage elements for the total power harvesting package solution. The talk from UF described the utilization of high-gain antennas with unique metamaterial superstrates for higher efficiency in wireless power transfer.

Student Awards: Prof. Rao Tummala graciously sponsored the student award recognitions. The student award judges (Prof. Christina DiMarino from Virginia Tech., Mr. Girish Wable from Jabil, and Dr. Urmi Ray from iNEMI) had tough decisions to make with all the high-quality student presentations. The winners are listed here.

- First Prize - Oral Presentation: Inductor-Linked Multi-Output Chiplet Power Delivery Architecture, Daniel Zhou and Mian Liao, Princeton University
- Second Prize - Oral Presentation, Cold-sprayed aluminum capacitors for 3D power packaging, Reshmi Banerjee, Florida International University
- First Prize - Poster Presentation, New Design Concepts for PCB-Integration Technology in Power Electronics Reducing Circuit Parasitics to a Minimum, Rando Raßmann, University of Applied Science, Kiel

3D-PEIM is held every two years. The location and date of the 2025 edition will be announce in society and industry publications in 2023.