

To: US Department of Commerce

Date: March 25, 2022

Subject: Commerce Department Requests Information on Supporting a Strong U.S. Semiconductor Industry

From: Heterogeneous Integration Roadmap (HIR)

We are writing in response to the Commerce Department Requests Information on Supporting a Strong U.S. Semiconductor Industry. <https://www.commerce.gov/news/press-releases/2022/01/commerce-department-requests-information-supporting-strong-us>.

In the four (4) items listed in the Commerce Department document, we have no input on the 1st topic semiconductor financial assistance program.

Our input will have a specific emphasis on the 3rd topic, “An advanced packaging manufacturing program” and linking relevance to the 2nd and 4th topics.

- A semiconductor financial assistance program that would provide funding, through a competitive process, to private entities, consortia of private entities, or public-private consortia to incentivize the establishment, expansion, or modernization of semiconductor manufacturing facilities and supporting infrastructure.
- A National Semiconductor Technology Center to serve as a hub of talent, knowledge, investment, equipment and toolsets.
- **An advanced packaging manufacturing program that focuses on the challenge of embedding fragile computer chips into very small configurations that combine multiple systems resulting in benefits including lower costs, increased functionality and improved energy efficiency.**
- The current and future workforce development needs of the semiconductor industry.

BLUF (Bottom Line Up Front)

- The Heterogeneous Integration Roadmap (HIR) is both a critical reference for advanced packaging technologies for multiple major market segments across the economy. HIR is freely available and regularly updated.
- The HIR effort brings together 400+ technologists from across the world to create a global innovation community from design to manufacturing.
- Pre-competitive collaboration among academia, industry, and government related to HIR is crucial for continuing electronics resurgence well into the future.
- Twenty-three HIR chapters constitute a comprehensive technology framework for academic packaging research and teaching for future workforce development.
- No interest in seeking financial assistance program.

Heterogeneous Integration Roadmap

The world's first open-source technology roadmap, the National Technology Roadmap for Semiconductors (NTRS), was sponsored by the Semiconductor Industry Association (SIA) when it was started in 1991 in the United States. In 1998, NTRS was joined in sponsorship by industry associations across Europe, Japan, Taiwan and Korea. It was renamed International Roadmap for Semiconductors (ITRS) and continued until all sponsoring organizations took the decision to end the ITRS in 2014. The last edition of ITRS was published July 6th 2016.

With the major shift to system- and application-centric focus from silicon device centric focus, we strongly believed in establishing the Heterogeneous Integration Roadmap as the premier application-critical and technology-relevant open source technology roadmap for the profession, industry and the entire semiconductor/electronics technical community. The goal is precompetitive collaboration among industry, academia, and government so that there is sufficient lead time to address technical challenges that could otherwise become major roadblocks and prevent continued progress and innovations in electronics towards improved performance, lower cost, energy

efficiency and enabling faster time-to-market.

Towards that end the ITRS Heterogeneous Integration Focus Team signed a Memorandum of Understanding (MOU) with IEEE Electronics Packaging Society (EPS previously known as CPMT) in March 2015, initiating the formation of Heterogeneous Integration Roadmap (HIR). Three IEEE Societies (Electronics Packaging Society, Electron Devices Society, and the Photonics Society), SEMI and Electronics and Photonics Packaging Division (EPPD) of the American Society of Mechanical Engineers (ASME), came together to form the Heterogeneous Integration Roadmap as the founding sponsoring organizations.

The Electronics Packaging Society, Electronic Devices Society and Photonics Society represents global technical professionals in electronics packaging, semiconductor devices and photonics. Their technical fields of interest includes design, assembly and test, materials science and materials engineering, from research, development and manufacturing, reliability and metrology across the ecosystem from electronics system companies, IDMs, fabless companies and foundries, start-ups, mid-size and major companies, universities and research institutes across the world. SEMI is the global industry association that unites the entire electronics manufacturing and design supply chain. ASME EPPD is the leading professional society in all thermal, fluid, mechanical and materials aspects of devices, packaging and systems, nano & micro mechanics. These founding sponsoring organizations represent the technical practicing professionals in semiconductors, electronics and photonics – for the total ecosystem worldwide.

The roadmap work started in earnest to design roadmap technology profiles, develop transparent governance, and, very importantly, recruit leading technologists, scientists and engineers to join the HIR effort.

The 1st edition of Heterogeneous Integration Roadmap was published on October 10th 2019. Below is the IEEE press release:

PISCATAWAY, N.J.--(BUSINESS WIRE)--IEEE, the world's largest technical professional organization dedicated to advancing technology for humanity, today announced the 2019 release of the Heterogeneous Integration Roadmap (HIR), a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration among industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of emerging devices and materials with longer research-and-development timelines.

The crucial change from ITRS to HIR is the shift from silicon device-centric focus to the system-centric focus. Electronics packaging bridging electronics system and electronics device has become the crucial factor for system product performance, cost and time to market. Innovations in packaging and systems have emerged to be a significant full throttle engine of innovation and creativity across diverse market applications from high-performance computing and data centers, to mobile, medical health and wearables, automotive, internet of everything, and aerospace and defense. Some examples of the packaging technology innovations include:

- Silicon Interposer
- Fan out on Substrate
- Silicon Bridge
- 3D stacking
- Chiplets
-more

These technologies are associated with innovations in architecture and design, process, test & assembly, and materials and equipment.

The HIR comprises twenty-three Technical Working Groups, each representing a specific technology area in the electronics ecosystem. The technical working group members are all volunteers (about 400 strong) from industry, universities and government research organizations from across the globe. The HIR comprehensively represent the total semiconductor and electronics ecosystem.

The Heterogeneous Integration Roadmap may be downloaded from the IEEE Electronics Packaging Society Website [Heterogeneous Integration Roadmap \(HIR\)](#) for free.

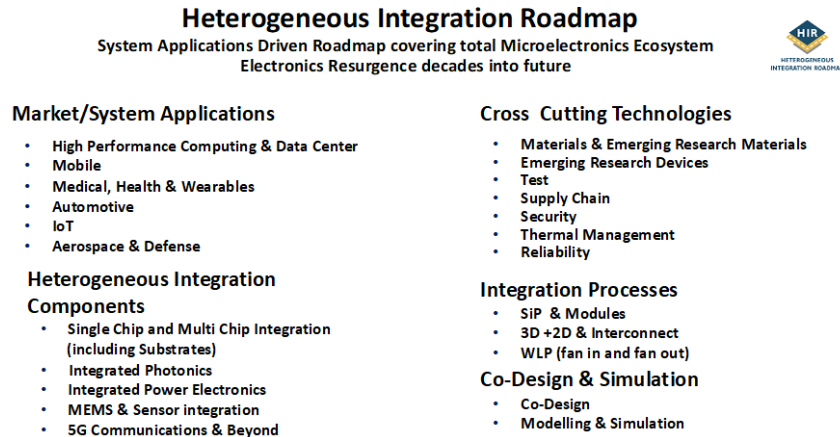


Figure 1 : Twenty Three (23) Technical Working Groups

The HIR twenty-three Technical Working Group (TWG) teams, while leveraging the global reach of societies and membership connections, have been highly successful in reaching out to the semiconductor and electronics packaging technical communities in North America, Europe and Asia through technical workshops, technology seminars, and keynote presentations. With COVID-19 global restrictions, HIR technical conferences and workshops are held in virtual or hybrid formats. Since launch, public release download has surpassed 53,000 HIR documents.

Heterogeneous Integration is defined as the integration of separately manufactured components into a higher-level assembly (Chiplets, SiPs, Modules) that, in the aggregate, provides enhanced functionality and improved operating characteristics. Figure 2 shows die of different sources, passives, and perhaps MEMs and Sensors integrated into a single package.

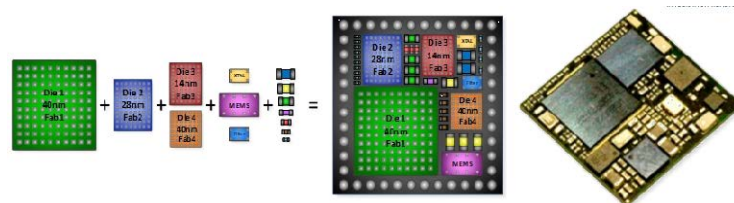


Figure 2 : Definition of Heterogeneous Integration: Chiplets, SiP & Modules

Willy Shih, Robert and Cizik Professor of Management Practice in Business Administration at Harvard Business School wrote on progress in high performance computing unveiled by Intel and AMD at the International Solid State Circuit Conference (ISSCC) in February 20 – 24 2022, where they both highlighted the significant role that advanced packaging will play in their respective future products. Professor Shih noted that impressive new performance capabilities come from modular approaches that combine building blocks made at different fabs and using different manufacturing processes, illustrating the vast potential of chip packaging for the future of semiconductor and microelectronics innovation. Professor Shih continued that the Intel Ponte Vecchio design is a case study in heterogeneous integration – combining 63 different die with a total of over 100 billion transistors in a single package measuring 77.5 mm x 62.5 mm. <https://www.forbes.com/sites/willyshih/2022/02/22/intels-ponte-vecchio-and-amds-zen-3-show-the-promise-of-advanced-semiconductor-packaging-technology/?sh=3e29393a5abe>

The modular partitioning of silicon microsystems enabled by advanced packaging herald a significant technology shift. Shih concluded that “granted many of the capabilities displayed here are still out of reach of most start-ups, but we can imagine that when the technology becomes more accessible, it will unleash a wave of mix-and-match innovation.”

Given ongoing digital transformation fueling the global economy, semiconductors and microelectronics are changing the world as we know it, whether desktops and tablets, smart phones, automotive, health care, communication, robotics, finance, or leisure. Professor Shih’s words “when the technology becomes more accessible it will unleash a wave of mix-and-match innovations” are another way to describe the rising tides of innovations in Heterogeneous Integration. The modular approach well exemplifies the incredible impact of heterogeneous integration on the resurgence of the electronic industry today and years into the future.

The theme and promise of Heterogeneous Integration and the crucial importance of pre-competitive collaboration across industry, academia, and government is well founded. A best practice case is the Semiconductor Research Corporation (SRC) for the quality and relevance of research output as well as education and mentoring of students into the semiconductor and microelectronics related work force.

HIR has provided technical input to SEMI for the nine questions from the Roundtable on February 23, 2022 and we will not repeat them here.

We would like to conclude with the “Bottom Line up Front” as shown previously

- The Heterogeneous Integration Roadmap (HIR) is both a critical reference for advanced packaging technologies for multiple major market segments across the economy. HIR is freely available and regularly updated.
- The HIR effort brings together 400+ technologists from across the world to create a global innovation community from design to manufacturing.
- Pre-competitive collaboration among academia, industry, government related to HIR is crucial for continuing electronics resurgence well into the future.
- Twenty-three HIR chapters constitute a comprehensive technology framework for academic packaging research and teaching for future workforce development.
- No interest in seeking financial assistance program.

Respectfully

The Heterogeneous Integration Roadmap Community

Reference

1. Shih, Willy, “Intel’s Ponte Vecchio And AMD’s Zen 3 Show The Promise Of Advanced Semiconductor Packaging Technology” <https://www.forbes.com/sites/willyshih/2022/02/22/intels-ponte-vecchio-and-amds-zen-3-show-the-promise-of-advanced-semiconductor-packaging-technology/?sh=3e29393a5abe>