Power Supply stabilization by Embedded Film Capacitor Substrate and 2nd level connection method for Large size Package

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I. Introduction

There are two problems in the enlargement of the High-performance CPU/ASIC package. One is the power consumption increasing of Hi-performance chips mounted on packages. Second is the assembly yield and reliability of the 2nd level connection such as BGA or LGA socket.

While a large power consumption requires stable power supply to the LSI, the allowable margin decreases and becomes difficult as the clock frequency increase and the driving voltage decreases. Therefore, the low impedance of the power supply in the package substrate is one of the important issues for improving power integrity. We solved this problem by embedded thin film capacitor technique in the package substrate.

For the 2nd level connection, BGA is adopted. This is because the BGA has a large allowable current and a low inductance, so that it is advantageous for an LSI having a large power consumption and a low driving voltage. On the other hand, in order to adopt BGA in a large package, it is necessary to keep the reflow mounting yield by controlling the thermal warpage behavior. Therefore, we adopted Full Low temperature Solder process. Reliability was also successfully ensured by optimizing the composition of low-temperature solder.

By adopting these technologies, a large package that can handle large power consumption with large number of BGA was realized while maintaining the conventional package structure.

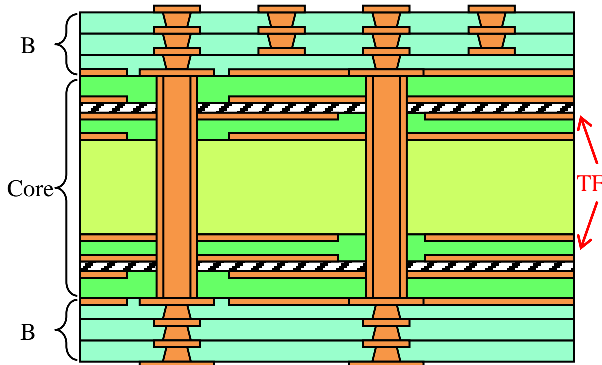


Figure 1. Cross sectional structure of embedded TFC layers.

II. TFC EMBEDDING PROCESS

The manufacturing process flow of the TFC embedded substrate is shown in Figure 2. The base TFC material was covered by conductor layers on both side of the BTO layer. This TFC material was developed by TDK Corporation. After patterning the conductor layers, two TFC materials were laminated on both sides of core layers.

The core layers were formed by conventional processes and ordinary bonding sheets were sandwiched in between the TFC and the core layers. The same bonding sheets covered the TFC surfaces completely and PTH was formed from top to bottom by mechanical drilling and plating processes. Through these processes, the TFC embedded core layers were formed. For the substrate completion, general build-up

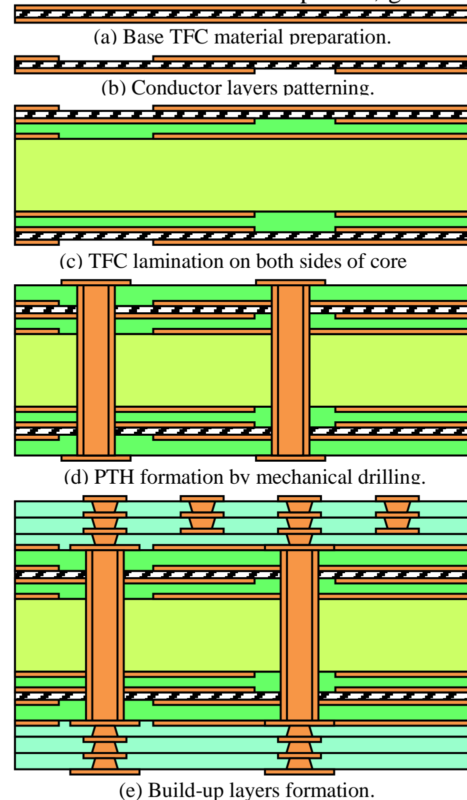
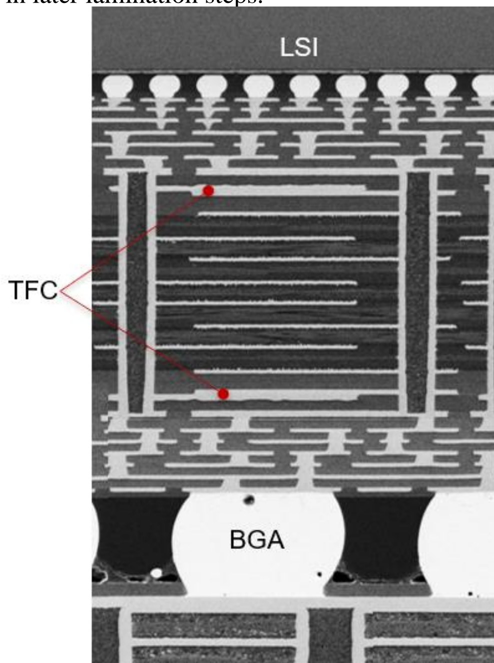


Figure 2. Manufacturing Process Flow

processes (laminating, laser drilling, and patterning) were applied in later lamination steps.



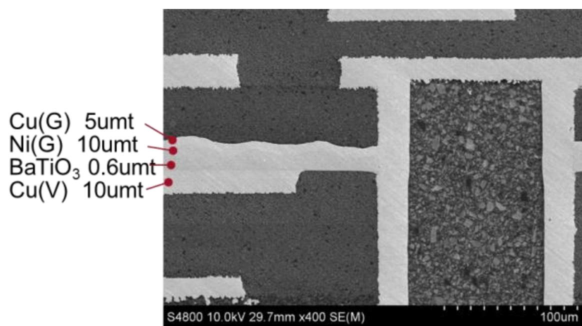


Figure 3. Cross sectional photograph of package substrate

SEM images of the cross section are shown in Figure 3.

We adopted ABF GZ41 for build-up layers and E679FG(R) for core layers.

It was confirmed that two TFC layers are clearly embedded as part of the core layers. More importantly, there was no connection defect between the TFC layers and the side wall of PTH.

There are two reasons to embed TFC in core layers and not in the build-up layers. The first reason is that the manufacturing process is much more efficient. It also allows for the layers to be wider.

If the TFC layers were embedded in build-up layers, several skip via structures which are formed by laser drilling are required. This complex laser drilling operation will lead to lower connection reliability, especially, when the embedded layers have been increased. Therefore, TFC embedded processes in core layers have huge advantages to enlarge the capacitance.

III. TFC'S ELECTRICAL PERFORMANCE

A. Impedance Measurement in power supply path

A test vehicle was prepared to evaluate the effect of impedance reduction by TFC layers. This substrate had a 1-8-1 layer structure and seven different plane areas named VDD [0:6] with 0.25 mm pitch probe pads on the surface layer. VDD-0 and VDD-6 are the minimum and maximum plane area, respectively. The impedance (Z11) from 1 KHz to 3 GHz was measured.

Figure 4 shows the measurement result. The electrical performance that the capacitance increases in proportion to the power / ground plane area demonstrated. From the slopes around 1 MHz in Figure 4, the correlation between area and capacitance was calculated. For comparison, the same measurements and calculations were carried out on a test vehicle with one TFC layer. Figure 5 shows the calculation results. It became apparent that the capacitance per unit area doubled by TFC layer number. These results indicate that with the increasing of TFC layers, it provides the same effect as enlarging the plane area. Therefore, it is unnecessary to widen the package substrate size.

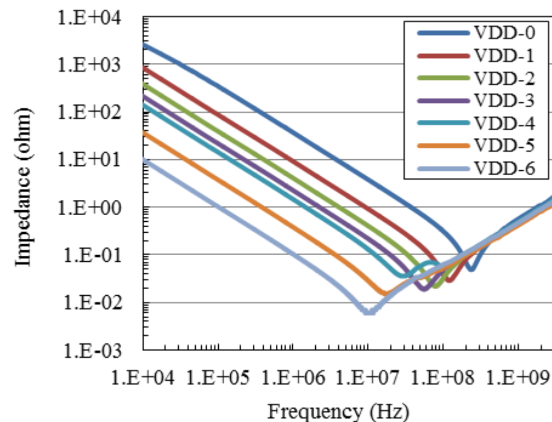


Figure 4. Impedance measurement results in the test vehicle

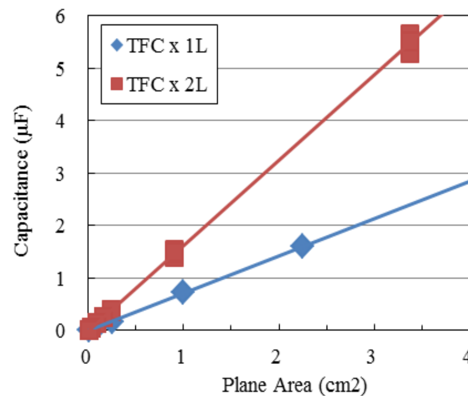


Figure 5. Relationship between the capacitance and the plane area.

TABLE 1. TFC EMBEDDED SUBSTRATE PROPERTIES.

Item	*Specification*
Number of Layers	6-14-6 (with 2 layers TFC) 6-10-6 (without TFC)
Thickness	1.43 mm (with 2 layers TFC) 1.xx mm (without TFC)
Via diameter	Laser: 0.06 mm, PTH: 0.15mm
Dielectric material	Build-up: GZ41, Core: E679FG(R)
Substrate size	75.8 x 63.0 mm

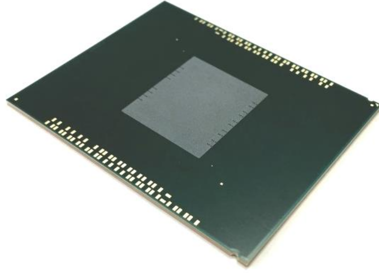


Figure 6. Photograph of FCBGA package substrate.

In order to evaluate the product adoption, flip-chip ball grid array (FCBGA) package substrates were prepared as shown in Figure 6. The specifications of the substrate were listed in Table 1. Two substrates were designed under the same specifications; one with double TFC layers and the oter without. Figure 7 shows the impedance measurement result. The capacitance reduction was confirmed by TFC layers as in figure 4. It was also determined that it can be reproduced by simulation data with SIwave (Ansys, Inc.).

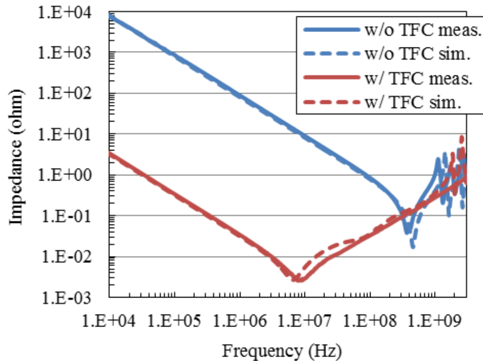


Figure 7. Measurement (solid) and simulation (dot) results of impedance.

B. *Power Delivery Network (PDN) Simulation with die-package-board integration model*

By the circuit simulation with advance design system (ADS, Keysight Technologies, Inc.), the impact of TFC was investigated through the integration circuit model as shown in figure 9. The RLC circuit models of the die and board were set up any values with reference to our current product data and the package models were alternately use with double TFC layers model and without TFC model which were simulated with SIwave.

In addition, traditional ceramic capacitors were mounted on package surface and bottom layers, also on the board. Figure 9 shows the impedance profiles in the PDN simulation. In both models, the impedances in low frequency were controlled with ceramic capacitors on the board or on the package and the upwards to the right near 10 MHz were caused by the inductance of power supply path. However, from 10 MHz to 1 GHz, the impedance behavior was completely different in each model. The first resonance peak was reduced from 5m ohm to 2m ohm and the right downward inclination shifted to lower frequency. Because the inductance from the TFC and to C4 pads is very low, it enables to affect the impedance behavior in high frequency region.

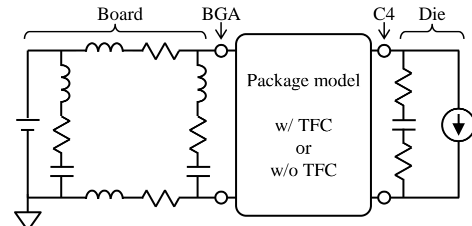


Figure 9. Simple PDN circuit model for simulation.

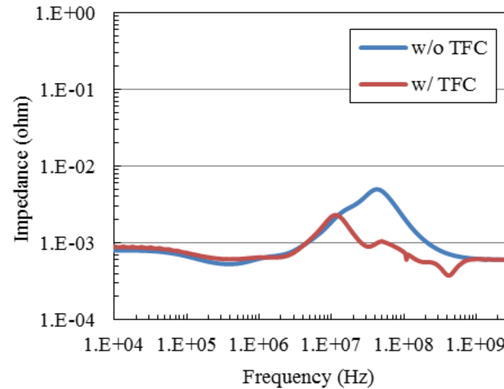


Figure 10. Impedance simulation result in frequcy domain.

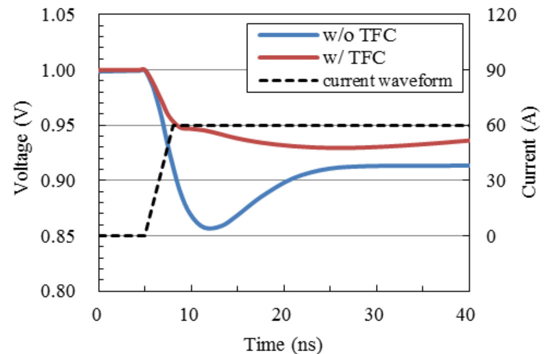


Figure 11. Voltage noize simulation result in time domain.

Figure 11 shows the results of time domain simulation. The first droop voltage noises were compared when the current was simply raised from 0 to 60 A during 3 ns. The voltage drop could be reduced by approximately

50 % with the TFC embedded substrate. This noise reduction could be resulted from the impedance improvement around 100 MHz. This result will be able to greatly contribute to the power integrity, for example, higher frequency CPU clock and lower voltage driving.

IV. 2ND LEVEL CONNECTION METHOD

Figure 12 shows the appearance of the BGA package. This package size is 63.0×75.8mm. The maximum total height of this package is 5.14mm. The BGA ball pitch is 0.80mm, and the diameter of the ball is 0.50mm. 5124 of BGA are formed on this package.

LID size is 51.0×63.8mm. The connection of chip and Cu-LID satisfies high thermal conductivity with In-3Ag TIM. The Cu-LID is composed of heat spreader and stiffener, and is attached to the organic substrate with the adhesive.

Figure 12. Appearance of BGA-Package

It is the largest BGA package size ever, and the BGA pitch is 0.8mm, so it is necessary to ensure the mounting yield on the motherboard. The most important problem is the thermal warpage behavior of the package during the reflow for the BGA mounting. At the reflow peak temperature of the conventional Sn-3Ag-0.5Cu, the package warps more than the BGA ball diameter, and it is predicted that the open/short failure occurs frequently. Therefore, low melting point solder was used for both solder balls and solder pastes of BGA, and the reflow peak temperature was lowered to suppress thermal warpage behavior of the package and

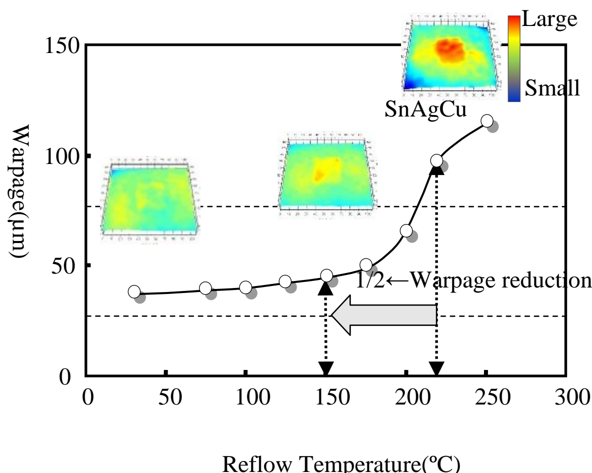


Fig.13 Warpage of package-substrate during reflow soldering.

ensure the yield in the 2nd level connection.

Fig. 13 shows an example of the thermal warpage behavior, it is shown that warpage deformation of the package substrate can be reduced to 1/2 by lowering the temperature.

In order to lower the melting point temperature, we chose Sn-58Bi composition solder. Melting point is 138 ° C. However, in Sn-Bi solder, the brittleness caused by containing hard Bi lowers the reliability of the joint. Fujitsu has developed Sn-Bi solder with a small amount of 0.4%Ag, and evaluated, taking into account the results of application to MCM since 2000.

Because the selection of the composition had been completed, the reliability test was executed.

For understanding BGA location that we should be paid attention, thermal stress simulation was executed. Figure 11 shows the simulation model. For estimate BGA stress by simulation, we enter all mechanical parts such as cooling plate and stiffner.

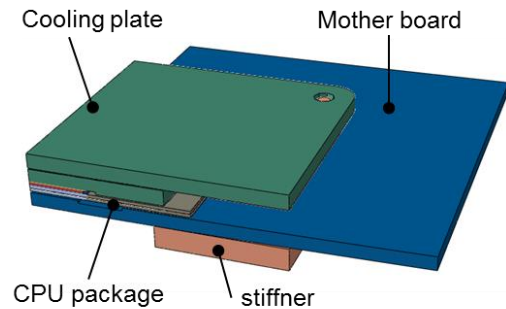


Figure 14. BGA Reliability Simulation model

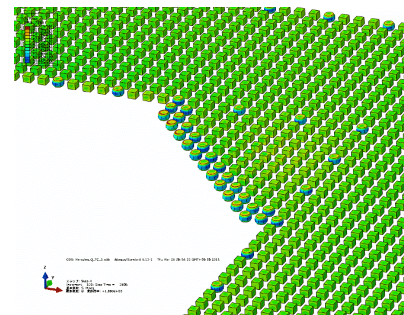


Figure 15. BGA Reliability Simulation Result

By this simulation, we decided to observe inside corner area bumps.

For BGA connection reliability test, thermal cycle test was performed, condition is 0/100C, detailed profile is shown in Figure 16.

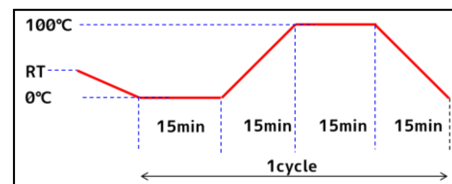


Figure 16. Thermal cycle profile

Figure 17. show the location that BGA cross sections were observed after thermal cycle test. Figure14 is actual cross sections of BGA after 400cycle and we could successfully confirm.

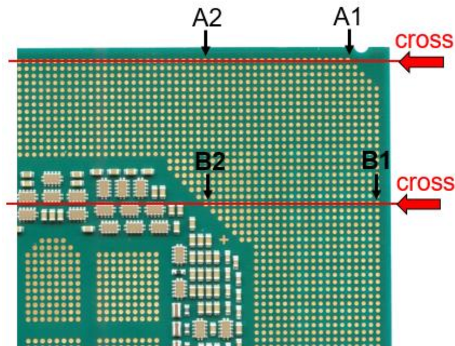


Figure 13. Observed BGA location after TC

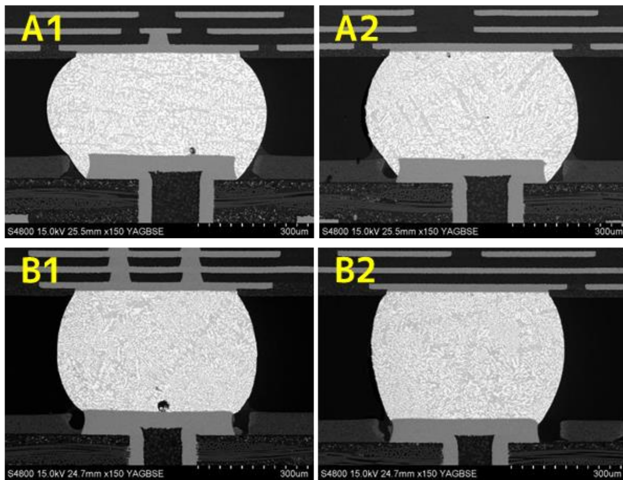


Figure 14. Cross Section of BGA connection after TC

V. Conclusions

Two technologies have been developed to solve the problems of power supply noise and high-pin count BGA mounting due to future enlargement. The first is a low inductance embedded capacitor package substrate. The other is the mounting technology for large and high-pin count BGA by using Full Low Temperature solder process. These will be important technologies to contribute future performance enhancement of LSI.

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