Manufacturing Challenges for Large Substrates

Rich Graf/Marvell Semiconductor

Adoption of advanced packaging methods, such as 2.5D and chiplet based MCM assembly, combined with higher speed I/O, increasing I/O counts, and increasing product complexity have resulted in significant growth to FCBGA substrate size and complexity, which has strained the industry FCBGA substrate supply the last few years. Significant application drivers for increasing substrate complexity have been high performance computing (HPC, including server CPUs and AI accelerators), 5G base stations, and high-end networking. Substrate complexity requirements have increased with higher layer counts, reduced chip and package interconnect pitch, finer substrate line and space wiring, increased stacked via counts, higher package I/O requirements, and custom requirements such as embedded bridge die[i] or passive components.

The increasing product size and complexity have a significant impact on substrate capacity, which resulted in a supply shortage throughout 2021 and 2022. As Figure 1 shows, increasing body size and layer count results in a non-linear increase in wiring area. This increased wiring area per substrate means each substrate requires a larger area of defect free processing and the impact of a single manufacturing defect is significantly larger compared to smaller lower complexity substrates.

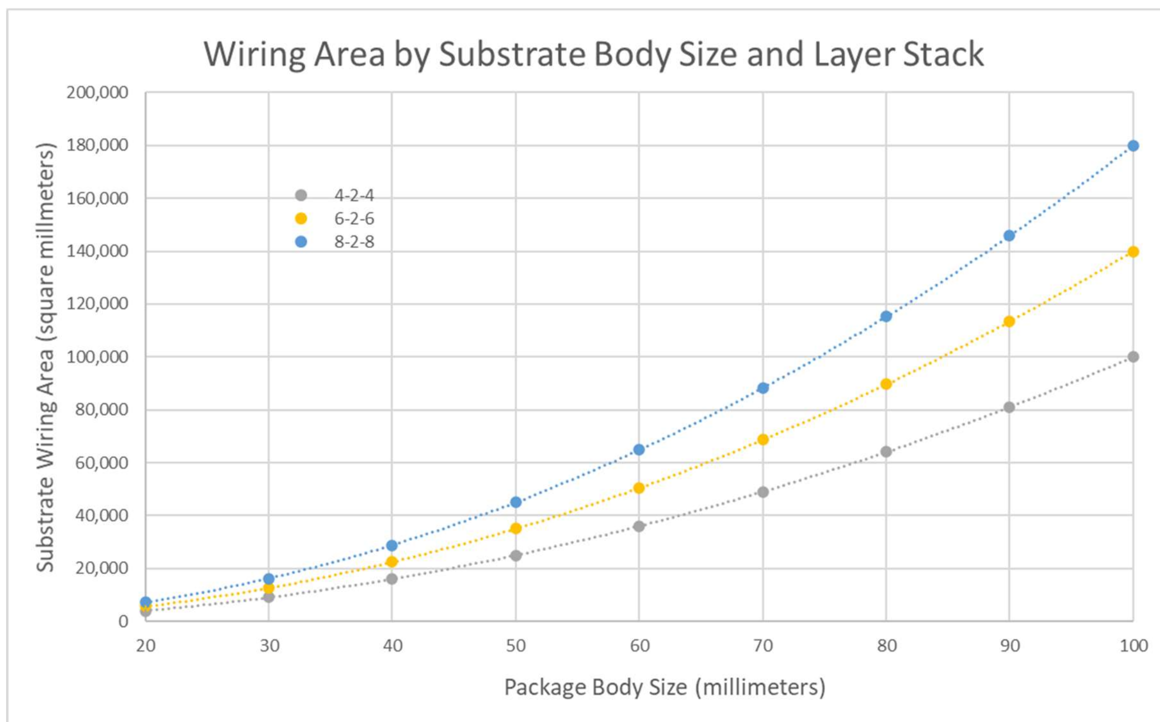

Figure 1. Graph of Substrate Wiring Area by Body Size and Layer Stack

Another challenge introduced by increasing substrate size and complexity is substrate warpage. To join large 2D chips or 2.5D interposers to a substrate, the substrate must have controlled warpage at room temperature through reflow temperature of approximately 245 degrees Celsius[ii]. This requires both substrate supplier manufacturing optimization, advanced materials[iii], as well as substrate design optimization to address both global and local copper density.

To improve the mechanical and electrical performance of large build up substrates, advanced materials are available and new materials and manufacturing methods are in development. For the fiberglass weave core, lowering the material coefficient of thermal expansion (CTE) improves the reliability of the assembled package by lowering the overall substrate CTE closer to the CTE of silicon. For the build-up film material, key improvements come from lowering the CTE of the material to reduce the stress in the package as well as reducing the dielectric constant (DK) to improve high speed signal integrity. Large substrates also result in longer signal trace length to route from the chip interconnect to BGA. This longer signal trace length results in additional signal loss due to increased trace length. To maintain adhesion to the build-up film material the copper is chemically treated to roughen the copper, which improves adhesion between the copper and build up film, but results in additional signal loss. To minimize the signal loss, new copper roughening methods have been developed to reduce the high-speed signal loss while maintaining adhesion between the copper and build-up film.

Further improvements to package assembly of substrates can also benefit complex packaging using large substrates, especially for chip join processing. Two compelling technologies are laser assisted bonding[iv] and using low temperature solder[v]. Laser assisted bonding improves chip to substrate join performance by isolated heating of the silicon chip and solder bumps with reduced heating of the substrate. This results in reduced substrate warpage and can improve the yield of large substrate chip join. Using solders with a lower liquidus temperature can also reduce the warpage of the substrate through chip join to improve the yield.

As product complexity and size continues to increase, continued advancement in substrate materials, substrate manufacturing methods, large substrate yield capabilities, and assembly processes will enable the next generation of advanced products.

References:

[i] G. Duan, Y. Kanaoka, R. McRee, B. Nie and R. Manepalli, "Die Embedding Challenges for EMIB Advanced Packaging Technology," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), 2021, pp. 1-7, doi: 10.1109/ECTC32696.2021.00012.

[ii] Okamoto, K, Kohara, S, & Mori, H. "Effects of Build-Up Material Properties on Warpage Dispersion of Organic Substrates Caused by Manufacturing Variations." Proceedings of the ASME 2017 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems collocated with the ASME 2017 Conference on Information Storage and Processing Systems. ASME 2017 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems. San Francisco, California, USA. August 29–September 1, 2017. V001T02A018. ASME. https://doi.org/10.1115/IPACK2017-74098

[iii] S. Ikehira, "Novel insulation materials suitable for FOWLP and FOPLP," 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), 2021, pp. 729-735, doi: 10.1109/ECTC32696.2021.00126.

[iv] M. Gim, C. Kim, S. Na, D. Ryu, K. Park and J. Kim, "High-Performance Flip Chip Bonding Mechanism Study with Laser Assisted Bonding," 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), 2020, pp. 1025-1030, doi: 10.1109/ECTC32862.2020.00166.

[v] M. Koide, K. Fukuzono, M. Watanabe, T. Yamamoto and S. Sakuyama, "Full Low Temperature Solder BGA Development for Large size BGA Package," 2020 IEEE 70th Electronic Components and Technology Conference (ECTC), 2020, pp. 1265-1269, doi: 10.1109/ECTC32862.2020.00201.