Impact of Thermal Congestion on Advanced Package Test

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***Abstract*— The aggressive demand for integration results in multiple dies from the same or completely different fabrication technologies and perhaps different chiplet providers being combined within a single package. Each die may contains functional blocks that together form a complete platform when they are combined. Intrinsic use-case operational temperatures of each functional block are different for a variety of reasons. Package architecture, design and layout, along with material types play an important role to minimize thermal congestion.**

Keywords*— *Semiconductor, Chiplet, OSAT (Outsourced Semiconductor Assembly and Test), Multi-die Packages, Heterogeneous Integration, Test, Functional Test, Structural Test, System Level Test, Production Test Flow.

I. Introduction

In recent years there has been a sharp rise in multi-die package designs because die disaggregation results in higher levels of integration. Numerous publications targeting a large variety of applications exist in the public domain [1, 3]. Multi-die packages include Artificial Intelligence (AI), central processing unit (CPU), field-programmable gate array (FPGA), memory, analog, radio frequency (RF), input/output (I/O), serializer/deserializer (SERDES), silicon photonics, sensors, etc.

OSAT houses are in a unique position in the industry since they experience a wide sampling of customer products. Higher volumes and a higher mix of products result in a unique perspective of key learnings and avoiding missed steps for product packages with multiple die. Furthermore, 2D, 2.5D and 3D package layouts have unique thermal considerations.

II. Multi-Die Architecture, Design, Layout & Package Material

The building materials of a package include the substrate, the interposer, the solder balls, the die, the interconnect, the heat sink, the thermal interface material, the conformal and shielding material type, die-attach adhesive and the package mold compound material type. The material coefficient of thermal expansion and resistivity of each of these and their geometries impact the overall IC performance. For this reason, the material type and cost have to strike an acceptable balance.

Heat generated within the package is a function of the electrical power delivered to each die. The package thermal resistance is defined as the rise in temperature when one watt of power is dissipated.

$$\theta = \frac{\Delta T}{P} \text{°C/W}$$

ΔT is the change of temperature of the die relative to the package. This change of temperature results in heat flow from the die to elements within its close proximity, which could be a neighboring die or package material. The delivered power changes dramatically, depending on the functional state of the die block. In other words, it cannot be modeled as a static power level. Advanced package architectures and designs are designed so care is taken to optimize the heat flow path to the integrated heat spreader on the top or bottom of the package or through the package pins or balls. Any thermal energy trapped within the package is a source of thermal stress and results in poor performance during production testing and the end application. The rise in package temperature depends on factors like the die density, size of the die, the area of the die getting functionally exercised and hence, the amount of consumed electrical power.

The terms 2D, 2.5D and 3D refer to the layout of chiplets within the package. Since a chiplet's critical XYZ dimensions are different, there is a higher probability of a non-symmetric mechanical positioning of these chiplets around the package center. This aggravates package co-planarity challenges. Optimal floor architecture, simulation and modeling helps manage the thermal stress points within the package.

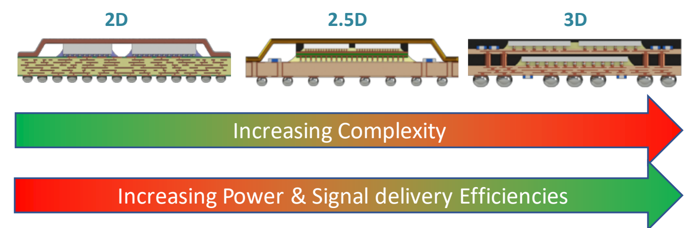

Fig. 1. Package complexity increases left to right, while the power and signal delivery & bandwidth interconnect efficiencies improve as the geometries shrink.

Thermal Congestion

Trapped heat within an advanced package may emerge on die that may result in detrimental performance of the victim die, in cases where certain specific design constraints such as thermal stress relief are not adequately applied. Fig. 2 shows the 2-dimensional block representation of a 3-dimensional layout.

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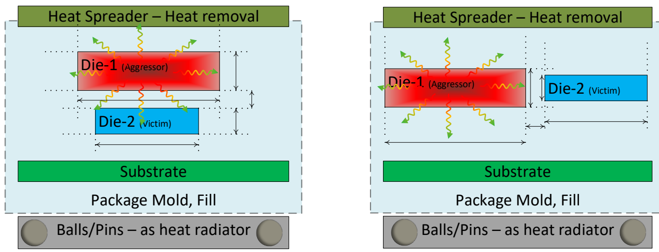

Fig. 2. Die-1 is the aggresor die that generates non-isothermal heat flow within the package. This may be a logic die, like a processor. Die 2 is the victim die that generates less than a couple of milli-watts of heat. Die-2 may be a memory die like a Double Data Rate (DDR) or High Bandwidth Memory (HBM) [4].

Unlike Fig. 2, in actual package component layout there are more than a single pair of aggressors and victims and the sum total thermal energy to manage at the package level quickly adds up. For instance, the range of thermal design power (TDP) of the aggressor die can typically be from ~30W to 150W or beyond and the TDP of the victim die can be up to ~10W, nominal [4]. This creates a thermal gradient within the package. The XYZ inter-die separation within the package plays an important role for thermal congestion caused by the aggressor on the victim. In a 2-dimensional layout, the integrated heat spreader is effective in thermal management. However, in a 3-dimensional stack, the sandwiched victim die will be subject to thermal congestion and requires the much-needed thermal relief.

Ansys's Icepak and Siemens's Flotherm simulation tools help with thermal modelling of the package design. Accurate identification of each of the design constraints allows predicting trapped thermal congestions within the package geometries. See Fig. 3.

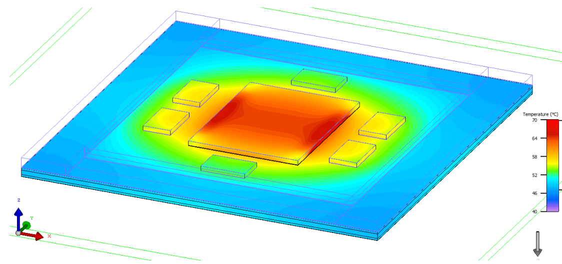

Fig. 3. Sample thermal modeling results.

III. Test Impacts from Thermal Congestion

There is a large overlap of thermal management requirements for production testing and the end-use applications. Numerous production test methodology improvements, such as being able to serialize testing of each processor logic block, thermal throttling, on-chip temperature sensing and sophisticated clocking schemes exist to keep chip junction temperature under their desired limits.

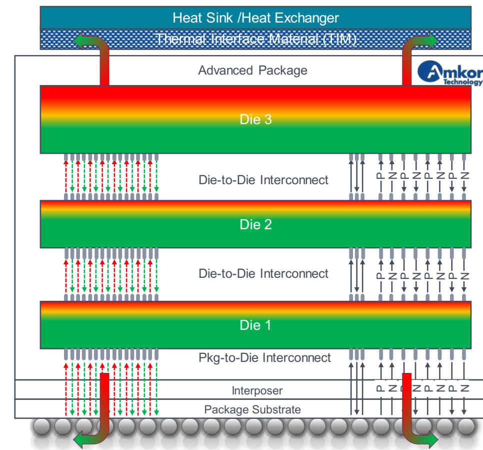

Fig. 4. Production test for power, data I/O, bias and clocks for multi-die packages.

The production test environment is different and perhaps more demanding, in some cases, than the end-use application because the intent is to comprehensively test every datasheet attribute in specific corner cases. Chiplet intellectual property (IP) providers feeding the 2.5D and 3D packages have an additional responsibility to architect their chiplet block so they are resilient to thermal sensitivities and corner cases that may be catastrophic and costly when not accounted for. Sensing of key attributes including thermal hot spots and control loops to throttle performance over outright production failure is acceptable methodologies.

Interconnects enable power delivery and signal paths to all die within the package. Wire-bonds, flip chip, interposers, Through Silicon Vias (TSVs) are examples of interconnect types. Interconnects within the package are made of high conductivity, lower resistivity material types. These interconnects have a dual role. In addition to servicing power and signal delivery, they provide lower thermal resistance to allow the heat to escape through the package substrate and balls. TSV interconnect technology is mature, and the thermal impacts are published in literature [5, 6]. See Fig. 4.

In Fig. 2, thermal energy that propagates from the aggressor to the victim, results in temperature rise of the victim. Higher temperature of the victim die results in degraded Vmin and maximum frequency problems, as shown in Fig. 5.

Poor thermally architected, designed and laid out packages result in marginal power performance and, in some cases, un-warranted loss of yield during production testing.

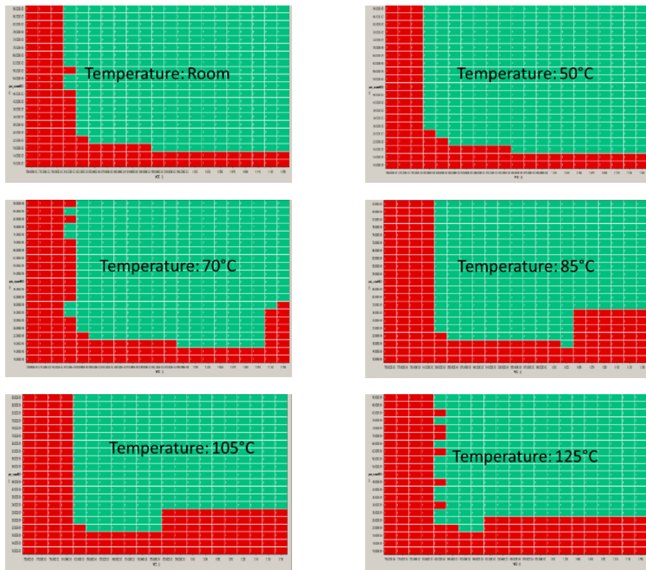

Fig. 5. V_{DD} and Frequency Shmoos – showing a shrinking envelope with increasing temperature. Courtesy: Test Development Engineering, Amkor Technology Inc.

IV. Production Test Methodologies

IEEE-1687 describes the test methodology for accessing instrumentation embedded within a semiconductor device [7]. Electronic Data Automation (EDA) vendors like Synopsys, have defined IP blocks to monitor environmental attributes including process, voltage and temperature (PVT) on-die [8]. Solution providers like ProteanTecs have a similar concept of adding sensors within the logic design and have documented numerous benefits to the overall manufacturing workflow [9].

PVT sensor placement in the vicinity of the thermal congestion is vital to analyze the severity and sensitivity of thermal densities within the package architecture and design implementation. It is simpler and more cost effective to sprinkle these sensors within the die rather than separately including them on-package. The telemetry stream under various corner cases are read back and analyzed to allow verification against the simulations. Fig. 6 shows a block representation of the Package Environmental Control for monitoring.

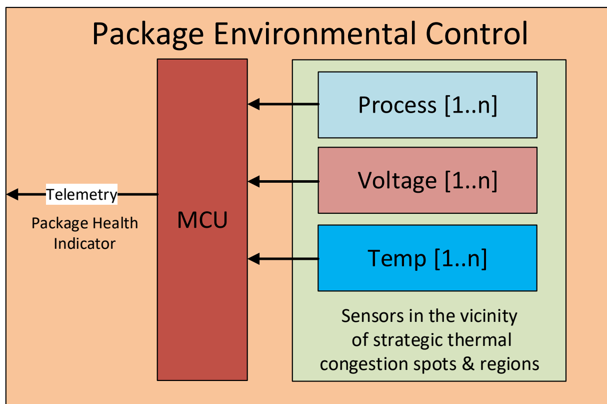

Fig. 6. A block representation of Package Environmental Control with a variety of sensors that allow a telemetry stream to monitor package health during active operation, including the production test process.

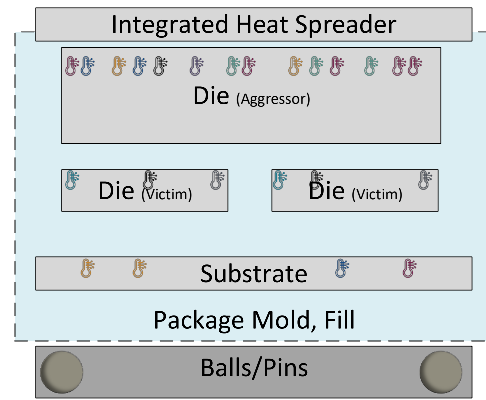

Fig. 7. Digital temperature sensors (DTS) sprinkled at suspected thermal congestion XYZ coordinates within the package.

There are increasing number of artificial intelligence (AI) engines and machine learning (ML) IP models as of the writing of this article. These engines allow data analytics tools to further refine the layout of chiplets within a package that greatly minimize large thermal gradients that may exists. These tools also help in pre-silicon simulation and post-package performance verification.

Test methods that allow feedback into package design and test are expected to help accelerate technology. Representatives within the Heterogeneous Integration Roadmap team [10] and the IEEE Test Committee with the testability best known methods (BKMs) [11] have continued to help the test industry, including OSATs to collaborate, compete and succeed in accelerating the path to technology maturity.

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