Thermal Interface Materials (TIMs) in Advanced Electronics: Status, Challenges, and Opportunities

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INTRODUCTION

The removal of heat from electronics—digital, analog, and for power management and control—to a final heat sink is becoming increasingly important as power densities (Watts (W) per unit volume or W per unit area) rise [1] and stacked (3D) logic and memory devices become increasingly common [2].

LOGIC MODULES

Logic devices (central processing units (CPUs) and graphics processor units (GPUs)) operate with much higher clock speeds, at greater efficiency, and have higher reliability when operating at lower temperatures [3], [4]. For digital electronics, the scaling efficiencies of power usage with reduced transistor size are noted to have hit an inflection point at the 7nm node for GPU architectures [5]. As nodes shrink below 7nm, power density increases, and the die will operate at higher temperatures unless steps are taken to remove heat from the chip. At the system design level, a typical goal is to have the die operating at a specific speed and overall system TDP (total design power) with the maximum transistor junction temperature (TjMAX) typical of a much lower TDP. The only means to achieve this is by removing heat more efficiently.

GPUs, due to their parallel compute structure, have larger, lower temperature, hotspots while CPUs tend to have smaller (few hundred nm), much higher temperature ones. Those CPU hot spots vary by chip or chiplet architecture and are already at heat fluxes of 1,000 W/cm^2 [6] and above. The coefficient of thermal expansion (CTE) mismatch between inorganic silicon (CTE = ~3 ppm/K) and organic materials used in packaging (CTE ~ 20 ppm/K or higher) results in warpage during thermal and power cycling and is also one of the reasons for the increasing usage of lower-temperature assembly [7], so that the reflow temperatures are typically much higher than those seen in actual system usage.

POWER DEVICES

For novel and emergent power devices, much has been made of the high current density, high bandgap, low forward-biased source-drain resistance ($R_{DS}ON$), and high-switching-frequency capabilities (due to the higher electron mobility) of compound semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN) devices, versus silicon power devices such as isolated gate bipolar transistors (IGBT) [8]. However, the final packaged SiC devices show a negative trend in $R_{DS}ON$ versus temperature. For example, the "normalized" $R_{DS}ON$ of 1.0 at ambient rises to 1.85 at 175°C for an exemplar packaged SiC die [9].

The compatibility of die bonding and encapsulation materials in contact with power die at temperatures above 175°C is also highly problematic, with delamination (interfacial failure) being a major issue [10].

NATURE AND CHARACTERIZATION OF TIMs

For free (heat source/heat sink) surfaces immediately adjacent to each other, with only air as a gap filler, the typical thermal resistance varies considerably, perhaps from 0.3 to >1 K.cm^2/W, varying a little with pressure and only slightly with temperature [11]. Therefore, the introduction of a more thermally conductive TIM as a

means of heat transfer from the hotter to the cooler surface is highly desirable (Figure 1).

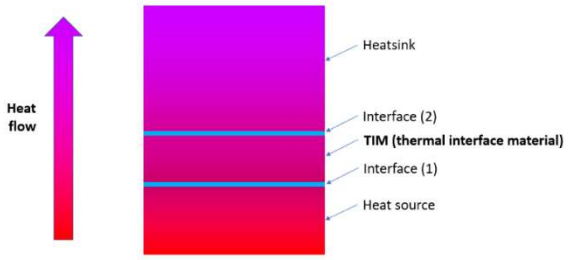

Figure 1. Basics of Heat Flow

The TIM is assumed to be homogeneous on the scale of its bondline thickness (BLT). The total thermal impedance (θ_{tot}) from Interface 1 to Interface 2 is therefore:

$$\theta_{tot} = \theta_{interface1} + \theta_{interface2} + (BLT / k_{TIM})$$

Where θ is the thermal impedance (S.I. units $K.m^2 / W$), and k_{TIM} is the bulk thermal conductivity (S.I. units W/m.K) of the TIM.

For many decades, ASTM D5470 [12] has been the standard for measuring thermal impedance. This standard has driven the design of suitable test equipment, including highly flexible tools that can control and cycle mean sample temperature, pressure, and bondline thickness [13].

	Typical Usage				
General TIMs Categories	TIM0	TIM1	TIM2	Heat spreaders	Bulk Thermal Conductivity (W/m.K)*
Thermally conductive adhesives			■		0-2
Die-attach adhesives		■			1-2
Gap fillers			■		1-3
Graphite sheets and films			■	■	1-5
Thermal greases and gels			■		1-5
Elastomeric sheets			■		2-8
Phase change compounds	■	■	■		5-15
Liquid metals and their pastes/gels	■				15-25
Metal preforms	■	■	■	■	20-86
Sintered metals and transient liquid phase metals/IMCs+		■	■		30-400
Vertically aligned carbon nanofibers/nanotubes/graphite	??	??	??		>200 (z-axis)

+IMC=intermetallic compounds **approximate range*

Table I. Types of TIM and Usages

NOMENCLATURE OF TIMs FOR DIGITAL PACKAGES AND MODULES, AND POWER MODULES

By convention, a TIM directly touching the semiconductor die is referred to as TIM1. In the case of standard silicon IGBT and SiC metal oxide semiconductor field effect transistors (MOSFETs), where electrical current passes in the z-axis, both thermal and electrical conductivity, and reliability, must be high. A lid or an intermediate substrate acts as a heat-spreader to conduct the heat to a local heat sink—this is referred to as a TIM2 or even a TIM3 (sometimes seen in power module assembly), if a third thermal interface is required. Figure 2 shows a simple diagram for logic devices.

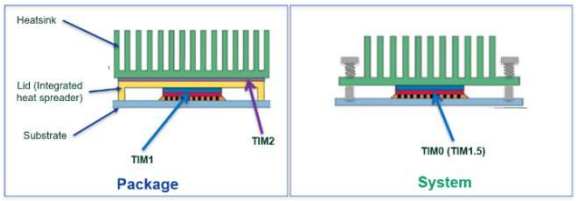

Figure 2. TIMs Nomenclature: Single Die

DIFFERENT TYPES OF TIMs

Gases and liquids, except for liquid metals [14] and helium, are not typically used as static (non-flowing) TIMs. Most TIMs are, therefore foams, gels, pastes, and solids, with more details given in Table I.

Most of the market for liquid, semi-solid, and solid conductive TIMs is for low-cost TIM2 materials and "gap fillers" with bulk thermal conductivities typically of around 1-3W/m.K [6]. However, the closer to the heat source, the lower the required thermal impedance.

Metals typically have a linear relationship between the two conductivities in the case of pure metals and most of their alloys, as seen in Figure 3. Most TIM1 materials are therefore soldered or sintered metals (reflowed solders or sintered pure metals), which has the disadvantage of necessitating a metallized die backside to create a reliable and continuous thermal pathway. The use of liquid metals is not necessarily subject to this constraint, but does lead to potential leakage issues. By using metals, because of their high bulk thermal conductivity, a thicker (greater BLT) TIM can be used, which greatly reduces the impact of mechanical and thermomechanical stresses [15].

TIMs INITIAL APPLICATION AND FINAL ASSEMBLY RELIABILITY

Taking a TIM from its initial design and test, to evaluation, to high-volume manufacturing is a complex process. Often a TIMs supplier's material product data sheet only has rudimentary data (usually some basic material characteristics and a bulk thermal

conductivity), with insufficient data to fully thermomechanically characterize the material in its final usage (noted in the 2021 version of the IEEE

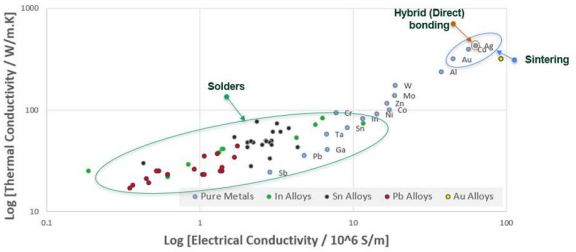

Figure 3. Wiedemann-Franz Law: Correlation between metal electrical and thermal conductivity

Heterogeneous Integration Roadmap (Thermal)) [16].

In most cases, TIM1 materials are part of a packaged device, meaning they will probably be subject to a series of high-temperature stresses during both lid and TIM application, lid-adhesive cure, and subsequent surface-mount-technology (SMT) assembly. Depending strongly on the nature of the final package type, the TIM1 and its package may typically experience 1-3 high-temperature (reflow) process cycles.

TIM0 materials, typically applied during the final assembly of a finished system, are usually free of major thermal stresses during their application but are subject to pressure. The increased total die area of high-performance-computing (HPC) compute modules (now at 10,000 mm^2 and more), along with the increased fragility of both the stacked thinned DRAM (dynamic random access memory) and logic die, has led to a drastic drop in allowable pressure for TIM0 applications, from 30-45psi (200-300kPa) to 5-10psi (35-70kPa) [17].

TIM RELIABILITY AND USE CASES

The reliability of the TIM in the final assembly depends on the overall impact of sequential and simultaneous stressors. Key initial stressors are those that occur in manufacturing (package or module assembly) and transportation. The finished assembly's use case ("mission profile") dictates the required lifetime. Use profiles help a reliability engineer to outline the stressors, both environmental (drop shock, thermal cycling, vibration, high-temperature storage life) and as a function of the system in use (high-temperature operating life, power cycling). The final user of the finished module or system dictates the use case, but guidelines such as JEDEC standard JESD94B [18] can provide a general overview. Test methods typically derive from the JEDEC JESD22 [19] series standards.

As an example of stresses on the TIM0, Figure 4 illustrates just some of the concerns in some more organic-based HPC modules (logic die + high-bandwidth memory (HBM)) mounted on a final organic substrate. Increasingly, these die may also be mounted on a separate inorganic interposer substrate (silicon or, in the near future, glass) to minimize thermomechanical stresses.

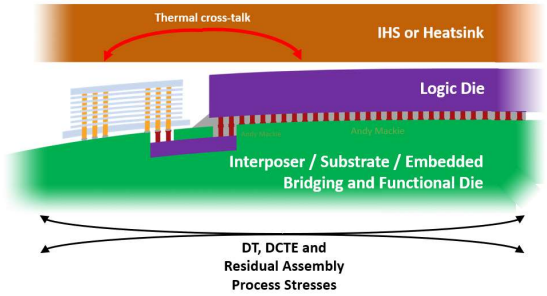

Figure 4. Simplified Thermal and Mechanical Challenges in Advanced Logic Modules

Figure 5 is a visualization of the issues that can and do arise during the initial application and final assembly utilizing the TIM. IMC is an intermetallic compound.

It shows why a generalized usage of the "supplier datasheet" bulk thermal conductivity (k) data to estimate thermal resistance (Rth) often results in a final TIM performance that fails to meet expectations.

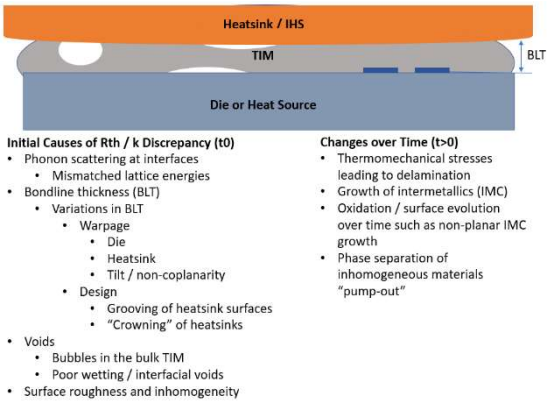

Figure 5. Generalized Time Zero (t0) and Reliability Concerns with TIMs

While there is an understandable desire to force some degree of failure in TIMs in reliability testing, there is increasing evidence from Intel and others that a more knowledge-based qualification may reduce the reliability test burden and speed-up time to market for TIMs users [20].

For die-on-organic-substrates at room temperature, soldered flip-chip dies typically show a "crowning" profile, whereby the die has edges and corners that are at a much lower level than the center of the die due to the difference in CTE between the silicon die and the organic substrate after the flip-chip solder has cooled and solidified. This differential CTE also creates serious problems for TIMs during power and thermal cycling, as the TIM at the die corners (the largest distance to neutral point (DNP)) is not only non-planar with the surface, but can then be subject to significant stresses beyond the nominal +/-50um [15].

HETEROGENEOUS INTEGRATION: 2.5D AND 3D

The need for reduced latency and increased efficiency of data transfer between logic die/chiplets and memory, any distributed (that is, not on the same die as the logic functionality) cache memory (usually L2, L3), and DRAM means that the interconnects between these devices must be much shorter and with much fewer losses by, for example, replacing solder bumps with direct copper-copper (so-called "hybrid") bonds. Initially, this meant die-attach to either a large silicon through-silicon-via (TSV) substrate with organic redistribution layers (RDL) or an organic substrate with a localized interconnect bridge (such as seen in Figure 4). However, more recently this has meant stacking the (less temperature sensitive) L3 cache memory die as separate chiplets on top of logic die.

Inorganic flip-chip substrates are designed with minimal differential CTE stresses: silicon interposers [21] and, more recently, glass substrates [22] alike. Figure 6 illustrates how HPC modules have changed with time and are evolving to include larger areas and increased capabilities, such as integrated photonics.

This "ossification" (move from organic to more stable inorganic materials) [23] of HPC logic modules will continue as a necessity of heterogeneous integration of chiplets, minimizing warpage due to the presence of larger interposer substrates and "stiffener/TIM" silicon interposers [24].

The announcement of die backside power delivery (BPD) [25] creates an interesting challenge to conventional thermal design considerations for heterogeneously integrated logic devices. The copper power vias, and their associated inorganic dielectric materials, must act as local heat channels to remove

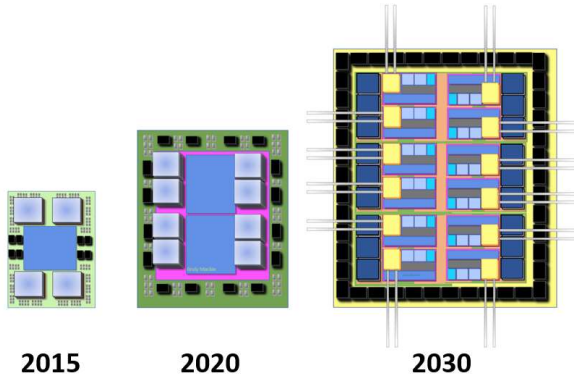

Figure 6: HPC Module Evolution

heat from the die backside to a final planar surface. The nature of the TIM to be applied to this surface is not well known at this time.

Even though HPC modules are getting larger, the overall reduction in assembly process temperatures, and CTE-matching of die and substrate alike, means that even large-area TIMs will not be subject to major bending stresses over their assembly and life cycle. This has led to the potential for usage of very thin BLT, relatively low k, but highly adhesive materials as TIMs.

Immersion cooling in dielectric fluids is becoming common in hyperscale datacenters, and it is important that any TIM exposed to these fluids be compatible with them. Metals-based TIMs show a distinct advantage over organic TIMs here, as metals do not react with the inert fluids used. As, and when, non-fluorinated, low-flammability, two-phase fluids become necessitated for vapor-phase heat transfer, specialized boiling enhancement coatings (BEC) [26] will become important as a means of transferring heat from the hot die to the phase-change fluid.

CONCLUSIONS

The increased power densities seen in advanced logic and power modules are placing increased emphasis on the need for thermomechanically reliable and low-thermal-resistance TIMs to meet evolving application and usage challenges.

For logic devices: The perceived need for both a high k and very soft (low modulus) TIM1 or (increasingly) TIM0 for advanced large-area HPC modules is being somewhat moderated by the increased use of stiffer, low-CTE inorganic materials, the use of lower assembly temperatures, and moderate environmental temperatures during their lifetime.

For power devices: Die are getting smaller at extremely high power density, and the emphasis is therefore on an extremely low thermal- and electrical-resistance TIM1 material capable of withstanding up to 200°C, with associated TIM2/3 materials.

Thermal interface materials are continually being developed to meet these challenges, and customers are increasingly demanding that TIMs suppliers provide reliability data, especially thermal cycling and power-cycling data above and beyond the simple "design from datasheet k value" approach that has been common until recently

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