Understanding Voids in Flip Chip Interconnects

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Outline

1st and 2nd Level Packaging Introduction

Voids
- Ball Drop (BGA and u-BGA) Voids
- Solder Screen Voids
- Surface Voids
  - Fabrication Voids
- Stress Driven Voids
  - Thermal Stress Voids
  - Electromigration Stress Voids

Testing Methods

Summary
1\textsuperscript{st} and 2\textsuperscript{nd} Level Packaging Technology Elements

**Chip- 1\textsuperscript{st} level interconnect**
- C4(solder) + Underfill

**1\textsuperscript{st} level packages**
- organic, ceramic

**1\textsuperscript{st}-2\textsuperscript{nd} level interconnect**
- solder, mechanical

**Heat spreaders**
- passive, active

**Thermal Interface Materials**
- paste, gels, metals

**Heat sinks**
- Cu, Al, complex design

**Printed Wiring Board (PWB)**

**Chip Carrier Options:**
- Ceramic
- Laminates
- Interposer
Bumping General Dimensions

- **Cu-Pillar**: UBM: 10 – 80 um
- **C4**: 80 – 150 um
- **uBGA**: 0.20 – 0.4 mm
- **BGA**: 0.35 – 0.9 mm

- **Flip chip interconnect pitch (um)**: 30 – 1300 um

- **Electroplating**
- **Paste Screening**
- **Preformed Solder Balls**
Cu Pillar is the fastest growing segment of the flip chip portfolio.

Source: 2015 Yole Flip Chip Report
Interposer Assembly

Possible Assembly:
- Join Laminate to interposer
- Underfill 1
- Join Top Chip to interposer
- Underfill 2
- BGA SAC attach
- Module Test

Materials:
- u-Cu Pillar
- C4 SAC solder
- Cu/Ni/Au pads
- UBM
- C4 SAC solder
- Cu pads
- SAC solder Coined
- Ni/Au or Cu OSP

Processes:
- Underfill 5X reflows
- Ball Grid Array (BGA)

Board Types:
- Top Chip
- Laminate
- Ball Grid Array (BGA)
- PWB

Solder Paste, and/or Imm Ag or Cu
Sn-Ag-Cu Solder Ternary Phase Diagram

Ni/Cu is a very effective barrier for Pb-free applications – typically used on the chip side.

Thick Cu or solder on laminate side.

Ni-Solders results in $\text{Ni}_3\text{Sn}_4$ Intermetallic (IMC)
# BGA and u-BGA Void Types

<table>
<thead>
<tr>
<th>Types of Voids</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Macrovoids</td>
<td>Voids were formed as volatile ingredients of the fluxes within the solder paste, usually found everywhere in solder joint.</td>
</tr>
<tr>
<td>Planar Microvoids</td>
<td>Voids generated by anomalies in surface finish application process, generally located in one plane and found at the solder-to-land interface.</td>
</tr>
<tr>
<td>Shrinkage Voids</td>
<td>Caused by the solidification of SAC solders, formed as linear cracks with rough edges from the surface of the solder joints.</td>
</tr>
<tr>
<td>Micro-via Voids</td>
<td>Caused by microvias in lands.</td>
</tr>
<tr>
<td>Pinhole Voids</td>
<td>Voids generated by excursions in the copper plating process at board supplier.</td>
</tr>
</tbody>
</table>

![Void Types Diagram](image)

S = Solder
P = Landing Pad

R. Aspandiar, presentation at SMTA Chapter meeting (2005)
BGA: Shrinkage and Pinhole Voids

Shrinkage Voids:
Hot tear voids are formed during the solidification of the solder during BGA joining. Increase cooling rate can minimize this defect.

Pinhole Microvoids:
1 to 3 um in diameter crevices in the plated Cu matrix of the BGA receiving pad can entrap fluids resulting on void formation above IMC at ball attach.

BGA: Microvia Voids

Microvia Voids:
Via cavities within the BGA landing pad results on poor solder paste coverage, entrapping air. Large bubbles are attached to the UBM and do not escape. No solder paste fill results in increased voids propensity.

Mitigation:
- Eliminate the via topography: dog-bone, plugged or inverted microvias.
- Increase via size for better fill
- Optimize surface finishing for solder wetting and better fill.
- On chip to laminate joining, solder paste is first reflowed and coined (mechanically flattened) prior to chip joining.

Solder paste voids can be form during reflow due to solder dewetting.

- Flux volume, Flux evap. temperature, paste volume, pad surface area, pad surface finish and reflow environment, all play a role in void formation.

Solder paste Flux Selection and Voids

http://www.indium.com/blog/voiding-in-bgas.php
BGA: Planar Voids Root Cause and Solution

Microetch preceding plating → Silver Immersion Plating → Subsequent reflow/assembly

“High Risk” Process Cycle:
- Unfavorable peroxide etch creates micro-topography and sites susceptible to subsequent cave formation.
- Caves formed when high plating rate electrolyte forms silver roof over micro-topography and high risk sites. Cave volume magnified as roof forms.
- During reflow cycle, caves are exposed via solder melt, silver dissolution, and copper consumption. Voids formed do not escape.

Optimized Process Cycle:
- Preferred etch creates “rolling” topography and less high risk sites for subsequent cave formation.
- Minimal cave formation: Lower rate plating electrolyte permits controlled plating and copper displacement over “rolling” copper surface.
- No significant void formation due to minimal cave presence entering reflow operation.

## Pattern Electroplating Process

### Electroplated Pb-free Process

<table>
<thead>
<tr>
<th>Step</th>
<th>Process Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sputter Seed</td>
<td></td>
</tr>
<tr>
<td>Resist Apply</td>
<td></td>
</tr>
<tr>
<td>Define Pattern</td>
<td></td>
</tr>
<tr>
<td>Electroplate UBM (Cu, Ni) + SnAg solder</td>
<td></td>
</tr>
<tr>
<td>Resist Strip</td>
<td></td>
</tr>
<tr>
<td>Seed Etch</td>
<td></td>
</tr>
<tr>
<td>Reflow</td>
<td></td>
</tr>
</tbody>
</table>

![Image: UBM and C4 – As plated](image_url)
Electroplating Induced Interfacial (Planar) Voids

Post Reflow x-section:

Top view SEM of expose IMC after the solder was chemically etched:

Voids are between IMC and solder

Incorporation of Species at SnAg Plating which contribute to Void Formation

- Corrosion of bottom metal in SnAg bath
- Co-deposition of organics within solder (more prevalent as bath ages)
- Colloidal deposition

Electroplating Induced Interfacial (Planar) Voids

- Bath age impacts the onset of interfacial voids
- Propensity for Ag to corrode Ni (zero @ 150 sec) < Cu (25A at 5 sec / 110A at 150 sec)
- Propensity to form room temperature intermetallics with solder Cu >> Ni

Experimental matrix:
- Plate pure metal (Ni, Cu,)
- Immerse in SnAg bath (5 sec or 150 sec)
- Repeat with old SnAg plating bath (5 sec or 150 sec)
- Depth profile using Auger

Upon joining the Sn-based solder to the electroless Ni(P) UBM pad, the Ni reacts with the solder forming a Ni$_3$Sn$_4$ intermetallic. This reaction results in the formation of a crystalline Ni$_3$P layer also known as P-rich layer between the IMC and the Ni(P). Microvoids form on this layer.

NiV, NiW and NiSi UBM barrier have the same problem as Ni(P). This is known as reaction-assisted crystallization.
HTS: Electroless Ni(P) voids

Voids are generated in the crystalline Ni₃P layer after thermal stress.

- ENEC/OSP (Electroless Ni(P) + Electroless Copper + OSP) results in a robust (Cu, Ni)₆Sn₅ IMC which reduces the Ni consumption and so the Ni₃P formation.

HTS Stress and Kirkendall Voids

3 days of 125°C aging

Solder

Cu₆Sn₅

Cu₃Sn

Cu

10 days of 125°C aging

Solder

Cu₆Sn₅

Cu₃Sn

Cu

40 days of 125°C aging

Solder

Cu₆Sn₅

Cu₃Sn

Cu

Tz-Cheng Chiu, et. al., “Effect of Thermal Aging on Board Level Drop Reliability for Pb-free BGA Packages,” 2004 ECTC
Kirkendall Voids and IMC Voids

Kirkendall Voids - Mechanism 1:
- During Joining of Sn solders with Cu surface the \( \text{Cu}_6\text{Sn}_5 \) intermetallic crystallizes, along Cu layer, stopping further dissolution of Cu.
- Also a thin intermetallic layer, \( \text{Cu}_3\text{Sn} \), forms between Cu and \( \text{Cu}_6\text{Sn}_5 \).
- During thermal aging, atomic vacancies are left by Cu atoms migration from the Cu side – which are not filled by the Sn atoms.
- These vacancies coalesce into the so called Kirkendall voids at Cu - \( \text{Cu}_3\text{Sn} \) interface, and in \( \text{Cu}_3\text{Sn} \) layer.
- Voids can increase to form a discontinuous layer.

Impurities - Mechanism 2:
- Impurities in the plated Cu resulting in morphology and diffusion changes and void generation.

Vol. Reduction - Mechanism 3:
- Volume reduction and therefore voids during the conversion of \( \text{Cu}_6\text{Sn}_5 \) to \( \text{Cu}_3\text{Sn} \).

Mitigation:
- Replacing the Cu OSP layer with a Ni(P) or Ni(P)/Cu layer.
- Solder additives such as Ni, Bi, Zn.
- Increase purity of plated Cu.
Effect of %Ag in Cu₃Sn IMCs Growth

After thermal aging at 150 C/500 hrs, the size of Cu₆Sn₅ grains remains stable.

Cu₃Sn layer was reduced with increase of Ag% in the solder, but the thickness of total IMCs was similar. (Kirkendall voids reduction)

Increase in %Ag, reduces the Cu₆Sn₅ grain size

Moon Gi Cho, et. al., “Effect of Ag on Ripening Growth of Cu₆Sn₅ Grains,” 2010 ECTC
The size and number of Kirkendall voids increased with 500 hrs at 150 C HTS and remained stable at 1000hrs HTS.

Full conversion of intermetallic prior to HTS testing mitigated the Cu$_3$Sn IMC and the amount of Kirkendall voids at that intermetallic.

Microvoiding Vs. Kirkendall Voids

Where $D_{Cu}$ and $D_{Sn}$ are the intrinsic diffusion coefficients of Cu and Sn, respectively.

- If the voids are solely due to diffusion effects, the voids will concentrate at the $Cu_3Sn–Cu_6Sn_5$ interface.

S. Kumar, et. al., “Microvoid Formation at Solder-Copper Interfaces During Annealing,” JEM V40, No.12, 2011
Voids Generation vs Impurities in Plated Cu

Commercial Cu foils for PCB

Foil A

Foil B

Foil C

1 week@175°C

SIMS impurity measurement (ppm)

<table>
<thead>
<tr>
<th></th>
<th>Foil A</th>
<th>Foil B</th>
<th>Foil C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cl</td>
<td>57</td>
<td>8</td>
<td>59</td>
</tr>
<tr>
<td>C</td>
<td>28</td>
<td>8</td>
<td>47</td>
</tr>
<tr>
<td>O</td>
<td>5</td>
<td>1</td>
<td>12</td>
</tr>
<tr>
<td>S</td>
<td>0.5</td>
<td>0.02</td>
<td>6</td>
</tr>
</tbody>
</table>

In the high voiding Cu foils, the impurity levels are in the tens of ppm or less

Suppressor: polyethylene glycol (PEG)

Bath additives: Brightener: Bis-(3-sulphopropyl)-disulfide (SPS)

Accelerators: Thiol (-SH) or Sulfonate (-SO3)

From P. Borgersen

Cu Impurity Voids and UBM

Un-annealed sample, aging 1 wk/175°C

Foil 44
Foil 45

Cu Grain structure of annealed sample

Foil 44, 130 μm thick
Foil 45, 130 μm thick

Annealing: 2 hours at 650 °C

Correlation between impurities that can be decomposed/gasified and voiding is clear, and they do affect further grain growth:

From P. Borgersen

Voids Understanding: Cu Plating Bath Age

SPS+PEG+Cl-, 10 mA/cm² SPS replenishment at 1160 min.

At 550 and 1710 min. the voiding level appears to be the least.

➢ Bath Temperature and current density can also modulate void formation.

Solder Additives Mitigates IMC Voids

Joints Aged at 150 C for 1000 hrs

Also Ni and Co addition into the solder reduce the Cu3Sn and voids.

Soaking condition = 260°C 45min

Volume decrease @ IM formation:

- $6\text{Cu} + 5\text{Sn} \rightarrow \text{Cu}_6\text{Sn}_5 \rightarrow \sim 5\%$
- $3\text{Cu} + \text{Sn} \rightarrow \text{Cu}_3\text{Sn} \rightarrow \sim 7.6\%$

Voids and impurities migrate to the IMC center
Electromigration fails

IMC spalling into the solder

Current crowding:
Highest current density occurs at the point where the UBM meets the BEOL wiring

M. Lu, et. al., “Comparison of Electromigration Performance for Pb-free Solders and Surface Finishes,” 2008 ECTC

Chia-Ming Tsai, PhD Thesis
Testing Methods

- Ball Shear: Destructive
- Chip Pull: Destructive
- Ball Pull: Destructive
- X-ray (2D): Non-Destructive
- X-ray tomography (3D): Non-Destructive
- X-section: Destructive
Individual Solder Shear Test

% Voids can influence shear force (and failure mode).

Chip Pull Testing

- **Purpose**
  - Destructive test to check for structure and process robustness.
  - Chip is attached to the organic carrier and pulled with an Instron tool. Fail interfaces and pull strength is examined.

- **Sample Chip Pulls (destructive)**
  - Inspect for solder joints: good wetting, contact non-wets, non-contact non-wets
  - Large I/O chips require support substrate to prevent sample breakage.

**Failure modes**

- **In the BEOL**
- **Within the UBM**
- **At the Intermetallic**
- **In the solder**
Individual Bump Pull Test

Dage tool Testing Setup:

- Test speed: 1000mm/s (high speed ball pull)
- Land force: 10 gram.

- Typical force: 60 gf
- Failed interfaces:
  - At solder
  - At BEOL (pulled out)
  - At UBM or intermetallic

➤ New addition is automatic wire placement and wire pull.
3D X-Ray (X-Ray CT) Computed Tomography

3D X-Ray (X-Ray CT)
- 2D images are mathematically superimposed and processed to obtain a three dimensional map of the sample
- Virtual cross-sections at any give location. Resolution is limited by:
  - position wrt the source to freely rotate without hitting it.
  - the spot size of the x-ray source


Eric Perfecto – 2016 CPMT Webinar
X-Ray 2D Inspection

2D X-ray is the most common monitor tool for in-line solder void monitoring.

- BGS /CSP Package to substrate criteria:

<table>
<thead>
<tr>
<th>Location of Void</th>
<th>Class I</th>
<th>Class II</th>
<th>Class III</th>
</tr>
</thead>
<tbody>
<tr>
<td>Void in Solder (Solder Sphere)</td>
<td>60% of Diameter = 36% of Area</td>
<td>45% of Diameter = 20.25% of Area</td>
<td>30% of Diameter = 9% of Area</td>
</tr>
<tr>
<td>Void at Interface of Solder Sphere and Substrate</td>
<td>50% of Diameter = 25% of Area</td>
<td>35% of Diameter = 12.25% of Area</td>
<td>20% of Diameter = 4% of Area</td>
</tr>
</tbody>
</table>

Table 1: IPC 7095 Requirements for Void Classification

Michael A. Previti, et. al., “Four Ways to Reduce voids in BGA/CSP Package to Substrate Connections,” Cookson Electronics
X-section Method for Void Detection

X-section options:

1) Mechanical polish for large voids
2) Focus Ion beam (FIB) for small voids

http://www.indium.com/blog/voiding-in-bgas.php / CALCE
Summary

- Pb-free solder interconnect in Flip Chip, Cu-Pillar, CSP, and BGA continues to grow each year. And one of the major defect types in Pb-free applications is solder voids.

- There are many root causes for solder voids: fabrication, assembly and life stress. Most of them are understood and structure or process changes are available to produce a more robust Pb-free interconnect.

- By looking at the voids size and location, a good prediction of its origin can be estimated.

- Additionally, there are several testing methods that are used to characterize and monitor the fabrication and assembly processes to control any process drift and void formation.
Thank you.