Interconnect Materials in Electronic Packaging

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Student Program, IEEE CPMT
Consumers’ Electronics-
IC chips are packaged
Electronics Buffet – All-in-One Function Integration

Convergence #1 - Smartphones

source: 3D ICs-SEMICON Taiwan 2009
Notebook – packaged components

Flip Chip BGA

PGA

BGA
Various Levels of Electronic Packaging

- **Die level**

- **Module level**

- **Substrate/Board**

- **System level**
Multilayer Ceramic PGA (wire bonded)
Interconnect – Die Level

- Wire Bond
- Flip Chip
- TAB
- ACF
Die Level Interconnect – Wire Bond


- Ball Bond
- Wedge Bond

chip-terminal-to-wire interconnection

wire-to-chip carrier interconnection
Wire Bonding Process


(a) Electric flame-off (EFO) process to produce a spherical ball

(b) Al pad (1 um thick); heat (200°C).

(c) Normal force (0.6 N)

(d) (e) (f) (g) (h)

(c) Transverse ultrasonic vibration (150 mW); 0.025 sec

Ball Bond

Wedge Bond
Cu Wire Ball Bond

Ivy Qin,, Hui Xu, Horst Clauberg, Ray Cathcart, Viola L. Acoff, Bob Chylak, and Cuong Huynh
2011 Electronic Components and Technology Conference, 1489

Cu wire
Al pad splash
Si
Cu bonded ball
PdCu bonded ball
Terminal Metallization Materials for Wire Bonding

- On Si
  - Al, Cu doped Al
- On Lead (e.g., Cu alloy, Fe-Ni alloy) and Carrier
  - Pd-Ag
  - Au-Pd
  - Ni
Material Criteria for Bonding Wire

- drawability into fine wire
- strength for wire handling
- feasible with bonding techniques
- ductility for plastic deformation during bonding
- high electrical conductivity
- corrosion resistance
Wire Bonding Materials

- 0.8 mil ~ 0.6 mil (moving finer) diameter
- Au, Au-Be
  - Au-Be alloys: e.g., 1~2% or 30~100 ppm Be to inhibit grain growth, increase yield
- Cu, Pd plated Cu
  - Pd plating to prevent Cu from oxidation
- Ag, Ag-Pd, Pd (100 nm) plated Ag (2N)
  - 96~97% Ag + Pd to enhance mechanical strength and oxidation resistance.
Pd Plated Cu Wire

Ivy Qin, Hui Xu, Horst Clauberg, Ray Cathcart, Viola L. Acoff, Bob Chylak, and Cuong Huynh, 2011 Electronic Components and Technology Conference, 1489

TEM showing a Pd layer of ~80 nm abutting Cu.
IMC formed in Cu Wire Bonding on Al


Secure Bonding Strength
Wire Bonding Interaction

- **Ag-Al Interconnection**
  - Formation of AgAl₂

- **Au-Al Interconnection**
  - Formation of intermetallics (IMC): Au₅Al₂, Au₂Al, AuAl₂, AuAl, Au₄Al

- **Cu-Al Interconnection**
  - Formation of IMC: CuAl, Cu₂Al, Cu₉Al₄
• Electronegativity:
  \( X_{\text{Au}} > X_{\text{Cu}} \); Chemical Affinity for Al: Au > Cu

• Atomic size difference:
  \( \Delta r (\text{Al-Au}) < \Delta r (\text{Al-Cu}) \)

- the larger size difference between Al and Cu
  - the lower electronegativity of Cu
    - hinder Al solubility in Cu

<table>
<thead>
<tr>
<th>Properties</th>
<th>Gold</th>
<th>Copper</th>
<th>Aluminum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atomic radii (nm)</td>
<td>0.144</td>
<td>0.128</td>
<td>0.143</td>
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<tr>
<td>Electronegativity</td>
<td>3.1</td>
<td>2.2</td>
<td>1.5</td>
</tr>
<tr>
<td>Valence electron</td>
<td>1</td>
<td>1</td>
<td>3</td>
</tr>
</tbody>
</table>
**Wire Material Comparison: Au vs. Cu**


**Enthalpy** of formation of intermetallic compound:

\[ \Delta H = -96.6Z(\chi_A - \chi_B)^2 \]

\[ \Delta H (\text{Al-Au}) > \Delta H (\text{Al-Cu}) \]

- \( Z \): number of valence bonds
- \( X_A, X_B \): electronegativity of elements A and B

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**Table 3**
Heats of formation of aluminides in gold–aluminum and copper–aluminum systems [10]

<table>
<thead>
<tr>
<th>Compounds</th>
<th>Heats of formation, (-\Delta H) (kJ/g at.)</th>
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<th>Heats of formation, (-\Delta H) (kJ/g at.)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlAu (β)</td>
<td>38.7</td>
<td>AlCu (η')</td>
<td>20.0</td>
</tr>
<tr>
<td>Al₂Au (α)</td>
<td>42.1</td>
<td>Al₂Cu (θ)</td>
<td>13.4</td>
</tr>
<tr>
<td>AlAu₂ (γ)</td>
<td>34.9</td>
<td>AlCu₂ (γ)</td>
<td>23.0</td>
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</tbody>
</table>
**Wire Material Comparison: Au vs. Cu**


<table>
<thead>
<tr>
<th></th>
<th>Gold</th>
<th>Copper</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Ball bonding</td>
<td>Stitch tail bonding</td>
</tr>
<tr>
<td>Compressive force (gf)</td>
<td>35</td>
<td>50</td>
</tr>
<tr>
<td>Time (ms)</td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>Ultrasonic power (mW)</td>
<td>79</td>
<td>208</td>
</tr>
<tr>
<td>Impact velocity (mm/s)</td>
<td>8–10</td>
<td>15–20</td>
</tr>
</tbody>
</table>

**Cu wire bonding needs:** higher bonding power; longer bonding time
Interconnect – Die Level

- Wire Bond
- Flip Chip
- Ball Bond
- Wedge Bond
- Bumping
- Bonding
Solder Bump

UBM (Under Bump Metal)

63Sn/37Pb Solder Bump

Solder

Si
Flip Chip Solder Bump

Top side metallurgy (TSM)

Substrate

Chip

Solder bump

Oxidation barrier layer

Wetting layer

Adhesion/barrier layer

Chip passivation

Al or Cu pad
Bumping Process (1/2) – Ti/Cu UBM

- **STEP 1. Redefine Passivation**
- **STEP 2. Sputter Ti/Cu**
- **Step 3. Coat With Resist**
- **Step 4. Pattern For The Bump**
Bumping Process (2/2) – Ti/Cu UBM

Step 5. Electroplate Cu and Sn/Pb

STEP 7. Strip Cu/Ti

STEP 6. Remove Resist

STEP 8. Reflow
Electroplated Solder Bump

Reflow

Temperature (°C)

175°C
215°C

Time (seconds)

0 500 1000
IMC formed between Solder and Electroless Nickel Barrier Layer

Flip Chip Bonding vs. Wire Bonding

- **Flip Chip** -
  - Bonding is performed at once, a gang bonding process

- **Wire Bonding** -
  - Bonding is performed one by one individually

*Figure 2. CSP loops created by a ball bonder. Special bends are formed that provide this shape with the second*
Module Level Interconnect – Leaded and Leadless

SMT

Surface Mount Technology

Through Hole Technology

BGA

Ball Grid Array

THT

Leaded

Leadless

2015
THT – Wave Soldering
SMT Component - Pick and Place


Pick and Place

Solder Paste

Figure 6. MCM Type 2

Fig. 10.11 Solder paste applied to solder lands of a VSO component with a pitch of 762 μm. The effect of the wires of the screen is still visible in the solder deposit. Note also the shift of the solder print with respect to the solder lands, due to tolerances of board and screen. The small amount of split paste (in the centre lower region) will, upon soldering, lead to a solder ball. (Courtesy of G. Teeuwen, Finschhoorn).
Screen Printing of Solder Paste

BGA Substrate/Solder Ball

Ball size: 300 ~ 760 μm

Die pad
Ball pad

solder ball bonded
solder ball

Residue-free after Cleaning

SMT Magazine • May 2011
Notebook – packaged components
Solder Products (the form of solder) for Electronics Manufacturing

- Solder bump
- Solder preform
- Solder powder
- Solder paste
  - Solder powder + flux
- Solder ball
- Solder wire
- Solder ingot
Enhance wetting through:

- Clean tarnish film on substrate (e.g., CuO)
- Clean tarnish film on solder powder (e.g., SnO)
- Lower surface tension of solder and substrate (air to flux atmosphere)
Sn-Pb Phase Diagram

Pb: (prohibited by WEEE, RoHS)

- Low price
- Enhance oxidation resistance
- Lower surface tension
  - 470 dyne/cm for 63Sn-37Pb at 230°C, 550 dyne/cm for Sn at 232°C
- Eutectic with Sn
- Toxic
Sn-Ag Phase Diagram

Forms IMC at high Ag%

Eutectic 221°C
Sn-Cu Phase Diagram

Forms IMC

Eutectic 227°C
One of the major Pb-free solders: Sn-Ag-Cu

Eutectic Sn--Cu
- 99.3Sn-0.7Cu
- Eutectic temperature: 227°C

Eutectic Sn-Ag
- 96.5Sn-3.5Ag
- Eutectic temperature: 221°C
One of the major Pb-free solders: Sn-Ag-Cu

- **Eutectic Sn--Cu**
  - 99.3Sn-0.7Cu
  - Eutectic temperature: 227°C

- **Eutectic Sn-Ag**
  - 96.5Sn-3.5Ag
  - Eutectic temperature: 221°C

![Ultimate Tensile Strength Graph](image-url)

- Red: Quenched
- Blue: Air Cooled

<table>
<thead>
<tr>
<th>Composition</th>
<th>UTILITY TENSILE STRENGTH (UTS, MPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sn-3.2Ag-0.8Cu</td>
<td>32</td>
</tr>
<tr>
<td>Sn-3.2Ag-0.8Cu</td>
<td>30</td>
</tr>
<tr>
<td>Sn-3.5Ag</td>
<td>28</td>
</tr>
<tr>
<td>Sn-3.5Ag</td>
<td>28</td>
</tr>
<tr>
<td>Sn-0.7Cu</td>
<td>19</td>
</tr>
<tr>
<td>Sn-0.7Cu</td>
<td>22</td>
</tr>
<tr>
<td>63Sn-37Pb#</td>
<td>30.6</td>
</tr>
</tbody>
</table>
Substrate/Board Level Interconnects

BGA Substrate

- Plastic substrate (BT)
- Wire bond pad
- Ball pad
- Die pad
- Bonded solder ball
Metallization on BGA Substrate

- Contact Material: Au
- Barrier Material: Ni
- Base Material: Cu (Cu circuit)
- OSP: Cu

Organic solder preservative
3-D Sketch of PC Board

source: Principle of Electronic Packaging, C. Li
Plated Through Hole

Wassink, Soldering in Electronics

Glass fiber

Through Hole

25 μm Cu plating

(0.8mm)

Circuits

Cu plating

FIGURE 17-2
Typical plated through hole.
Through-Hole Activation (Electroless Cu Deposition) source: Principle of Electronic Packaging, C. Li

The electroless Cu provides the conducting base for electroplating.
Integration of Interconnects in Electronic Packaging
Integration of Interconnect Technology and Material – Stacked/3D IC Packaging


Figure 6: Triple-chip Stacked CSP contribution to compact, lightweight cellular phones

Figure 5: Triple-chip Stacked CSP Cross-section

Figure 3: Flash + SRAM Integrated into S-CSP

Alternative 2 Single-chip CSP (1.2 mm Max. Package each)

Significant (67%) Area Reduction on Motherboard
3D Packaging

Fig.1: Cross section picture and schematic of the Virtex 7 2800 T module (Courtesy of Xilinx Technologies and File Development)

source: 3D Packaging, Issue No. 23, May 2012

Samsung's 8-Stack Flash used in Apple's iPhone 4 (provided by Chipworks)

Fig. 11

source: SEMICON Taiwan, 2009

http://www.infoneedle.com/category/tags/wide-i/o?snc=20641