Interconnect Materials in Electronic Packaging

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Student Program, IEEE CPMT

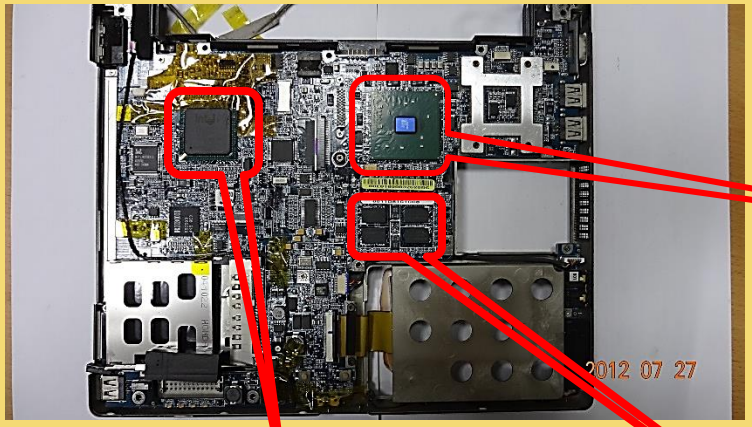
Consumers' Electronics-
IC chips are packaged

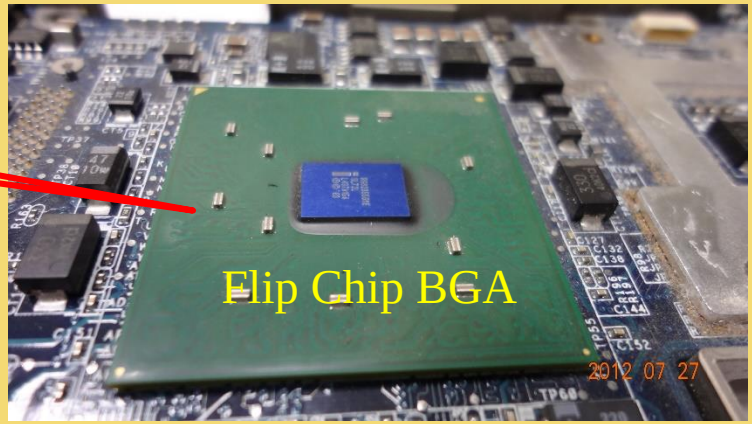
Electronics Buffet – All-in-One Function Integration

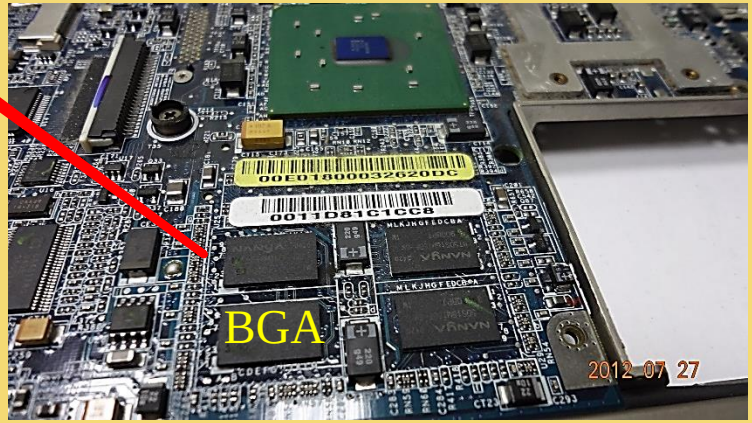
source: 3D ICs-SEMICON Taiwan 2009

Notebook –

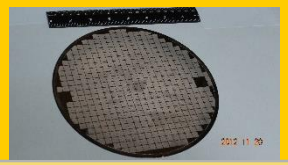
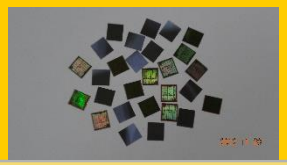
packaged components



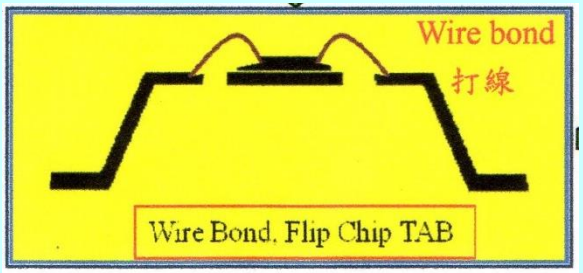




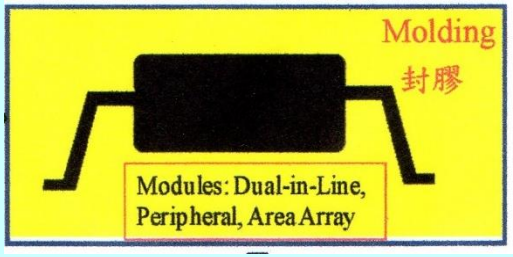
Various Levels of Electronic Packaging

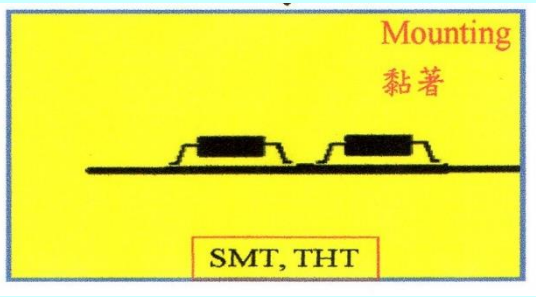

- Die level



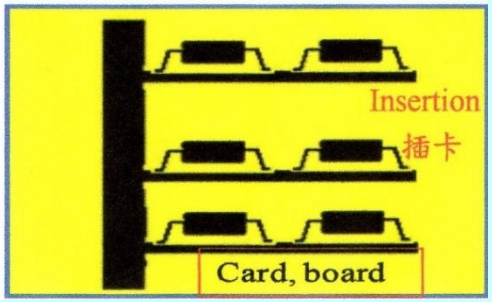
- Module level



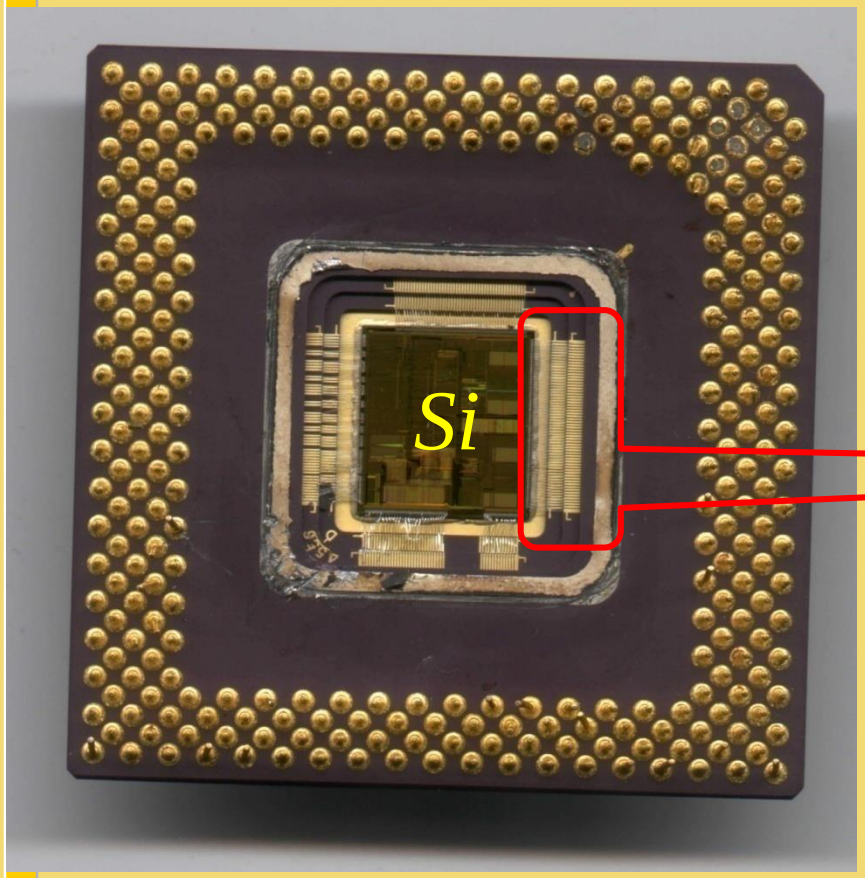
- Substrate/Board

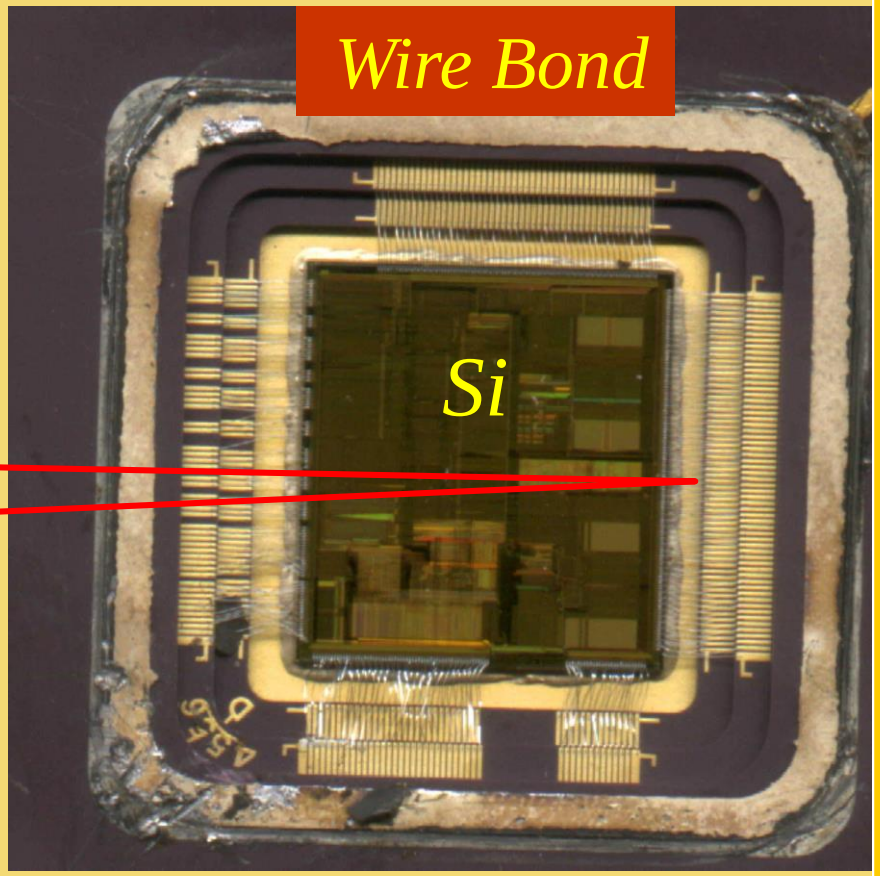


- System level



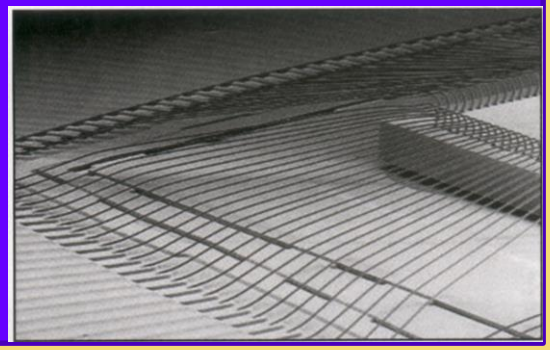
Multilayer Ceramic PGA (wire bonded)



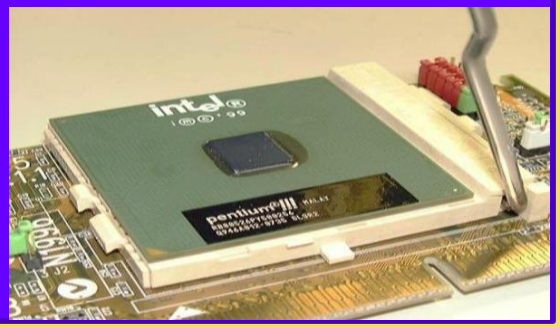


Interconnect – Die Level

- Wire Bond



- Flip Chip



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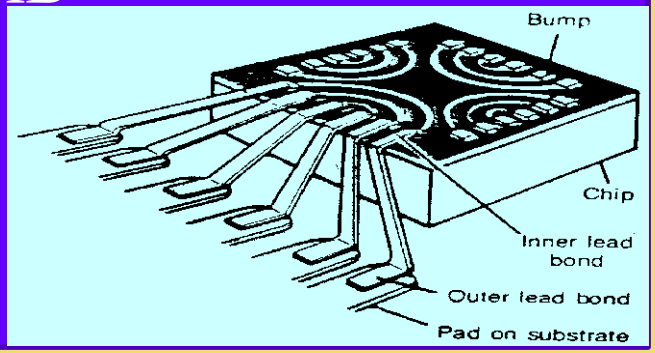
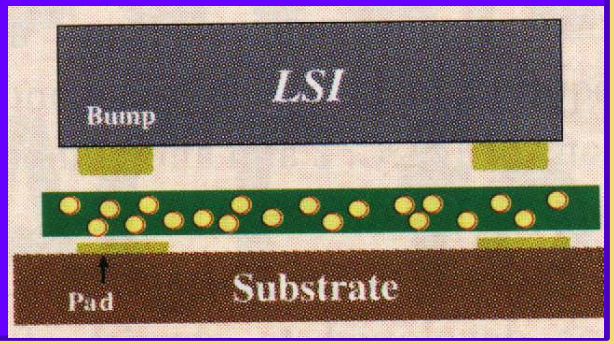


- ACF

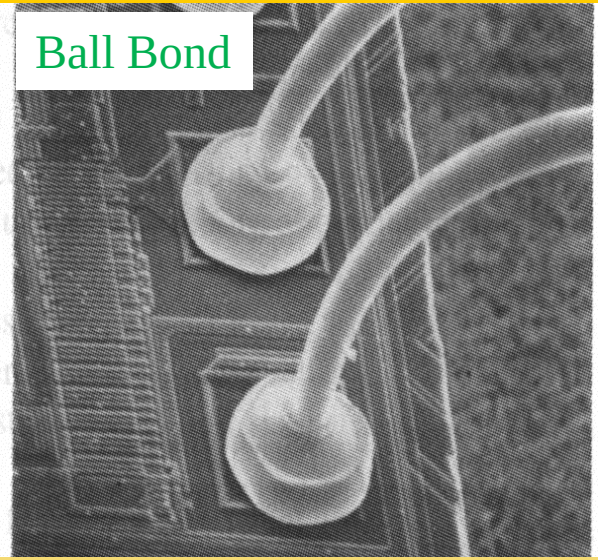


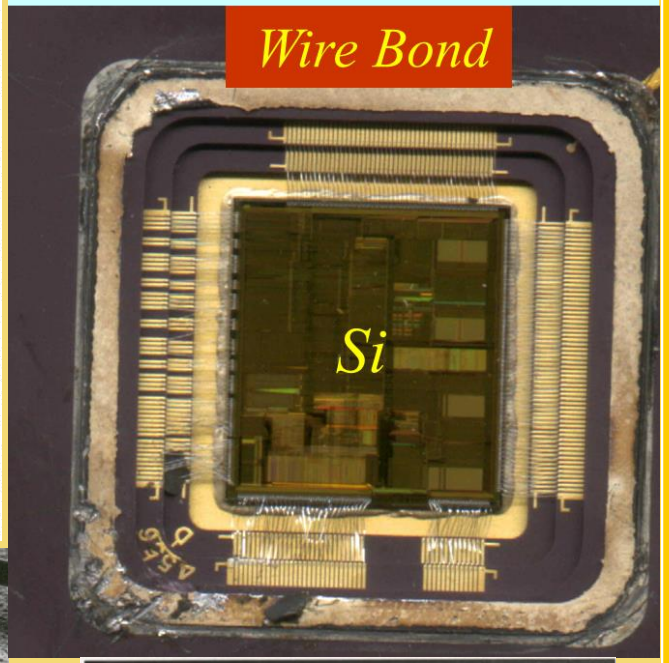
Die Level Interconnect – Wire Bond

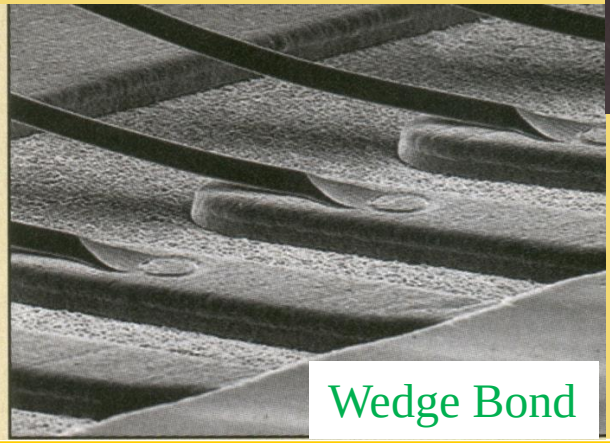
D. P. Seraphim et al., “Principles of Electronic Packaging”, McGraw-Hill, 1993

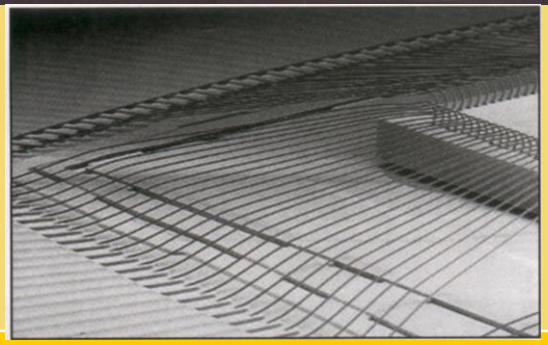
chip-terminal-to-wire interconnection

wire-to-chip carrier interconnection



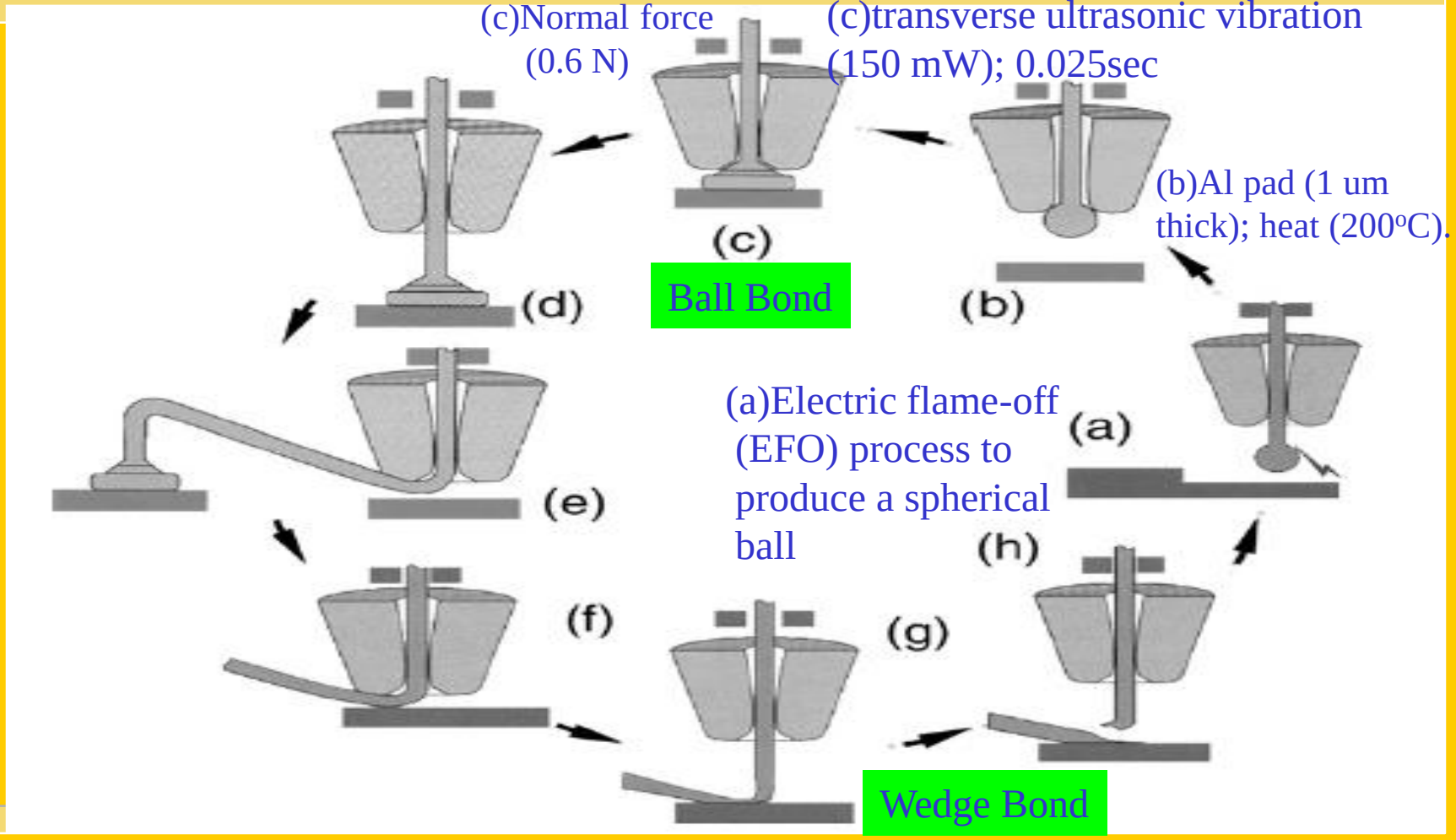






Wire Bonding Process

H. Xu/Scripta Materialia 61 (2009) 165–168
C.J. Hang / Microelectronic Engineering 85 (2008) 1815–1819, “Microstructural study of copper free air balls in thermosonic wire bonding”



Cu Wire Ball Bond

Ivy Qin,, Hui Xu, Horst Clauberg, Ray Cathcart, Viola L. Acoff, Bob Chylak, and Cuong Huynh,
2011 Electronic Components and Technology Conference, 1489

Terminal Metallization Materials for Wire Bonding

- On Si
  - Al, Cu doped Al
- On Lead (e.g., Cu alloy, Fe-Ni alloy) and Carrier
  - Pd-Ag
  - Au-Pd
  - Ni

Material Criteria for Bonding Wire

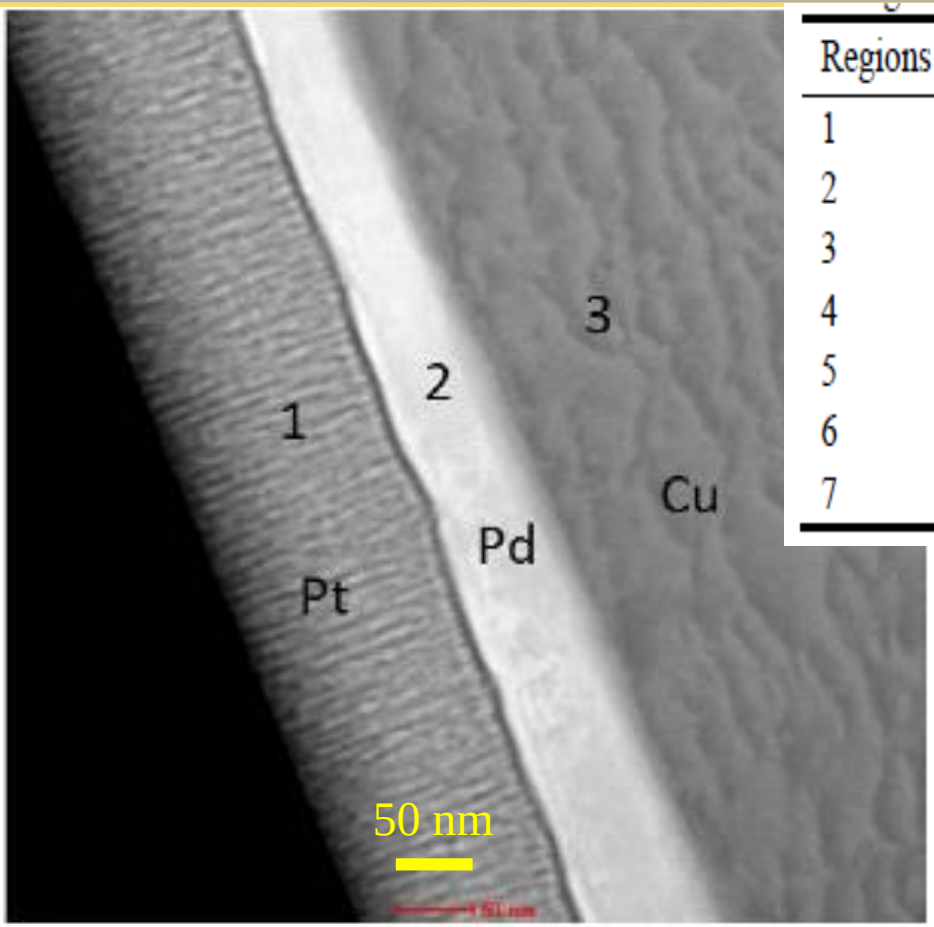
- drawability into fine wire
- strength for wire handling
- feasible with bonding techniques
- ductility for plastic deformation during bonding
- high electrical conductivity
- corrosion resistance

Wire Bonding Materials

- 0.8 mil ~ 0.6 mil (moving finer) diameter
- Au, Au-Be
  - Au-Be alloys: e.g.,1~2% or 30~100ppm Be to inhibit grain growth, increase yield
- Cu, Pd plated Cu
  - Pd plating to prevent Cu from oxidation
- Ag, Ag-Pd, Pd (100nm)plated Ag(2N)
  - 96~97% Ag + Pd to enhance mechanical strength and oxidation resistance.

Pd Plated Cu Wire

Ivy Qin,, Hui Xu, Horst Clauberg, Ray Cathcart, Viola L. Acoff, Bob Chylak, and Cuong Huynh, 2011 Electronic Components and Technology Conference, 1489

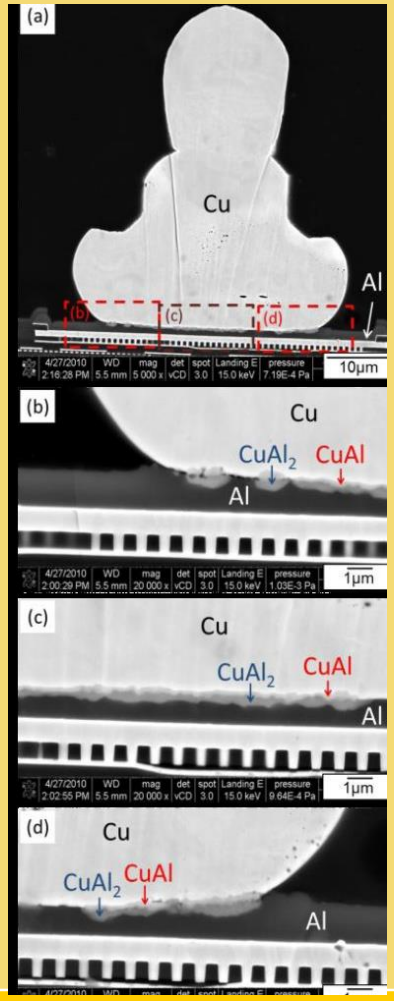


TEM showing a Pd layer of ~80 nm abutting Cu.

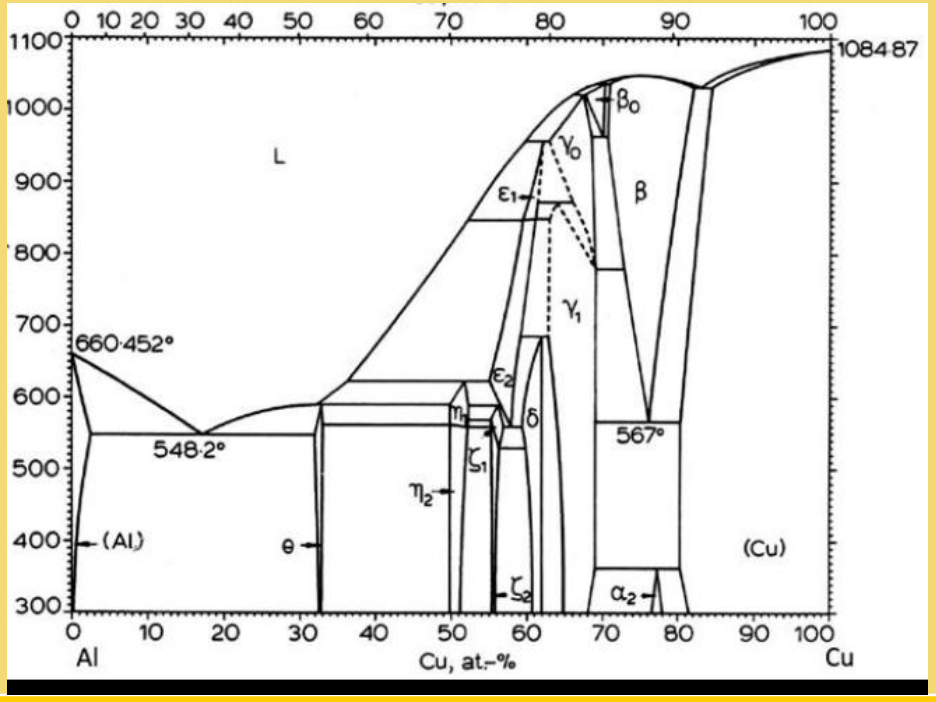
Regions	Pd K at.%	Cu K at.%	Pt K at.%
1	0.00	0.00	100.00
2	99.05	0.95	0.00
3	0.00	100.00	0.00
4	0.00	100.00	0.00
5	0.00	30.34	69.66
6	0.00	14.85	85.15
7	0.00	0.00	100.00

IMC formed in Cu Wire Bonding on Al

Y. H. Lu, Y. W. Wang, B. K. Appelt, Y. S. Lai, and C. R. Kao, 2011 Electronic Components and Technology Conference,1481



Secure Bonding Strength



Wire Bonding Interaction

- Ag-Al Inerconnection
  - Formation of $AgAl_2$
- Au-Al Interconnection
  - Formation of intermetallics (IMC):

    Au_5Al_2, Au_2Al, $AuAl_2$, $AuAl$, Au_4Al
- Cu-Al Interconnection
  - Formation of IMC:

    $CuAl$, Cu_2Al, Cu_9Al_4

Au and Cu Wire Bonding

S. Murali et al., Materials Research Bulletin 38 (2003) 637–646

- Electronegativity:

$X_{Au} > X_{Cu}$; Chemical Affinity for Al: Au > Cu

- Atomic size difference:
- Δr (Al-Au) < Δr (Al-Cu)

■ the larger size difference between Al and Cu
the lower electronegativity of Cu
➔ hinder Al solubility in Cu

Atomic properties of gold, copper, and aluminum elements [9,10]

Properties	Gold	Copper	Aluminum
Atomic radii (nm)	0.144	0.128	0.143
Electronegativity	3.1	2.2	1.5
Valence electron	1	1	3

Wire Material Comparison: Au vs. Cu

S. Murali et al., Materials Research Bulletin 38 (2003) 637–646

Enthalpy of formation of intermetallic compound:

(J.H. Westbrook, R.L. Fleischer, Intermetallic Compounds 1 (1994) 91–125, 227–275.)

$$\Delta H = -96.6Z(\chi_A - \chi_B)^2$$

ΔH (Al-Au) > ΔH (Al-Cu)

Z: number of valence bonds

X_A, X_B: electronegativity of elements A and B

Table 3

Heats of formation of aluminides in gold–aluminum and copper–aluminum systems [10]

Compounds	Heats of formation, $-\Delta H$ (kJ/g at.)	Compounds	Heats of formation, $-\Delta H$ (kJ/g at.)
AlAu (β)	38.7	AlCu (η^2)	20.0
Al_2Au (α)	42.1	Al_2Cu (θ)	13.4
$AlAu_2$ (γ)	34.9	$AlCu_2$ (γ)	23.0

Wire Material Comparison: Au vs. Cu

S. Murali et al., Materials Research Bulletin 38 (2003) 637–646

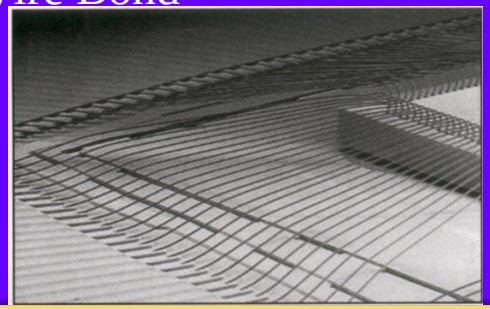
Table 1
EFO and bonding parameters of gold and copper 1 mil wires

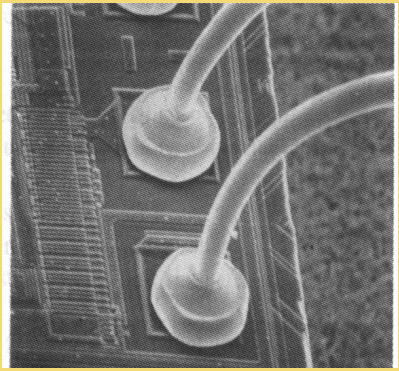
	Gold		Copper	
	Ball bonding	Stitch tail bonding	Ball bonding	Stitch tail bonding
Compressive force (gf)	35	50	25–46	45–70
Time (ms)	6	6	8–10	12–14
Ultrasonic power (mW)	79	208	113	350–399
Impact velocity (mm/s)	8–10	15–20	8–10	15–20

Cu wire bonding needs:
higher bonding power; longer bonding time

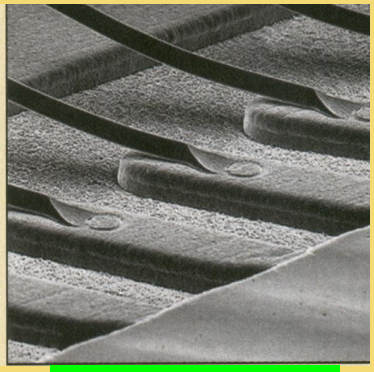
Interconnect – Die Level

- Wire Bond



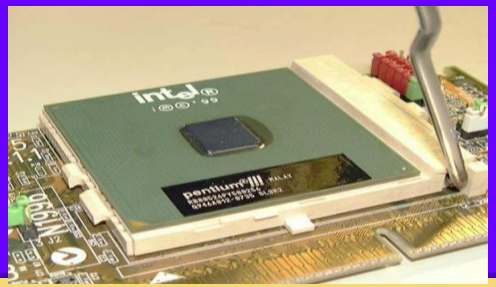


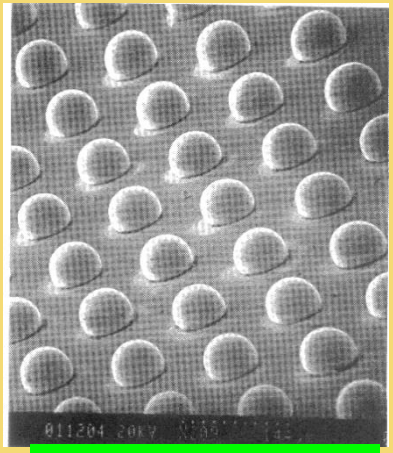
Ball Bond



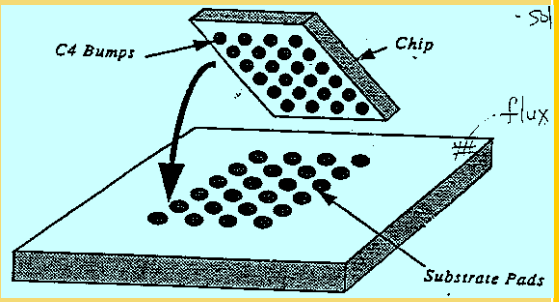
Wedge Bond

- Flip Chip



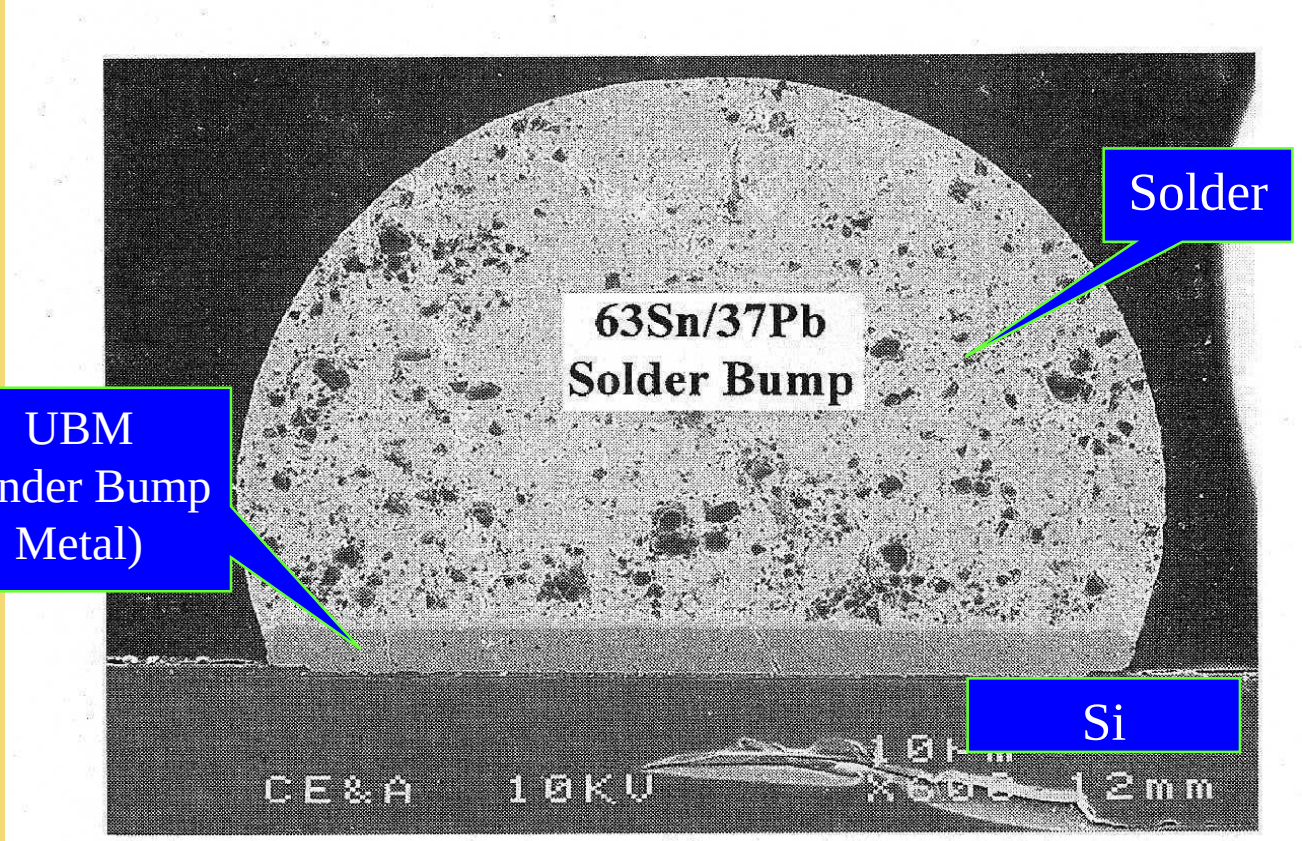


Bumping

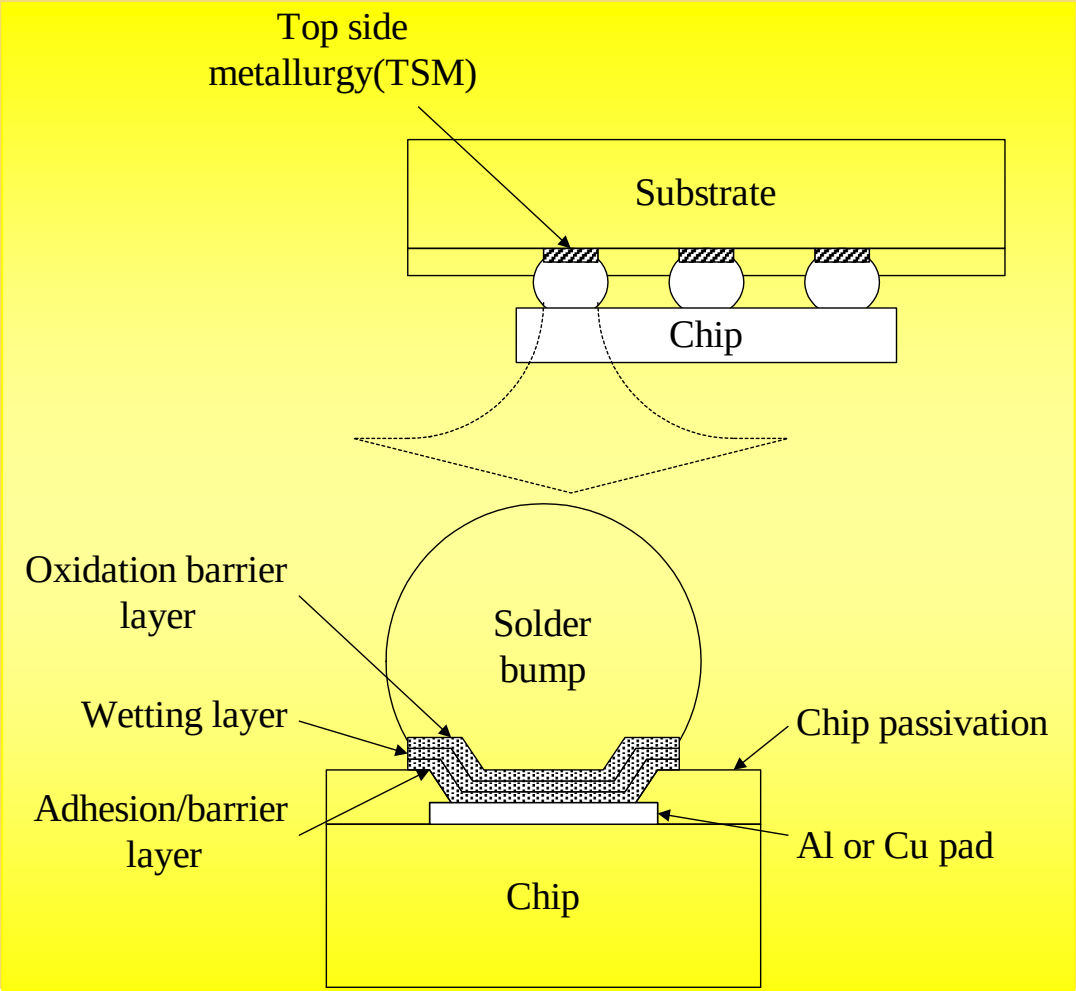


Bonding

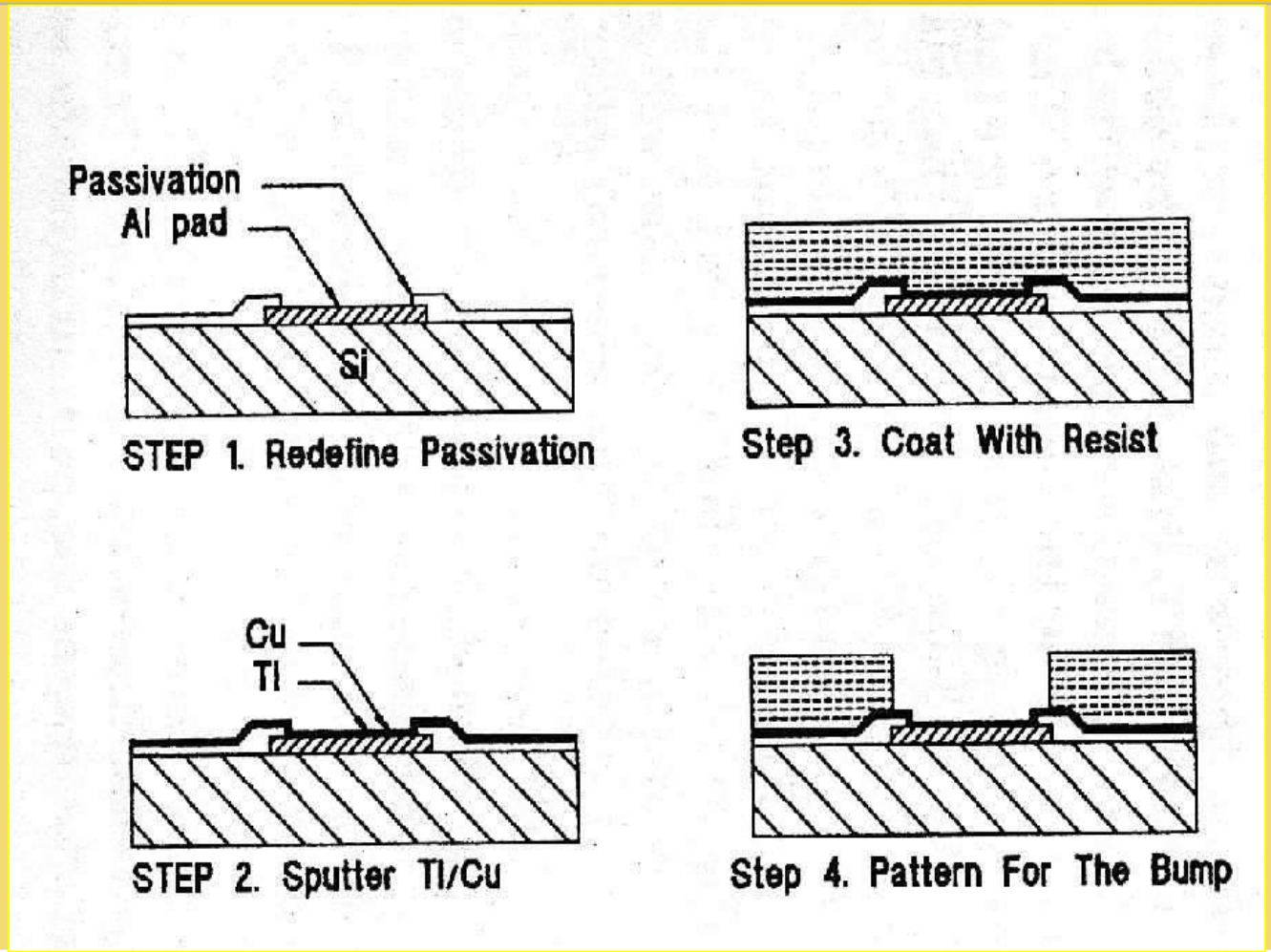
Solder Bump


63Sn/37Pb
Solder Bump
Solder
UBM
(Under Bump
Metal)
Si
CE&A 10KV

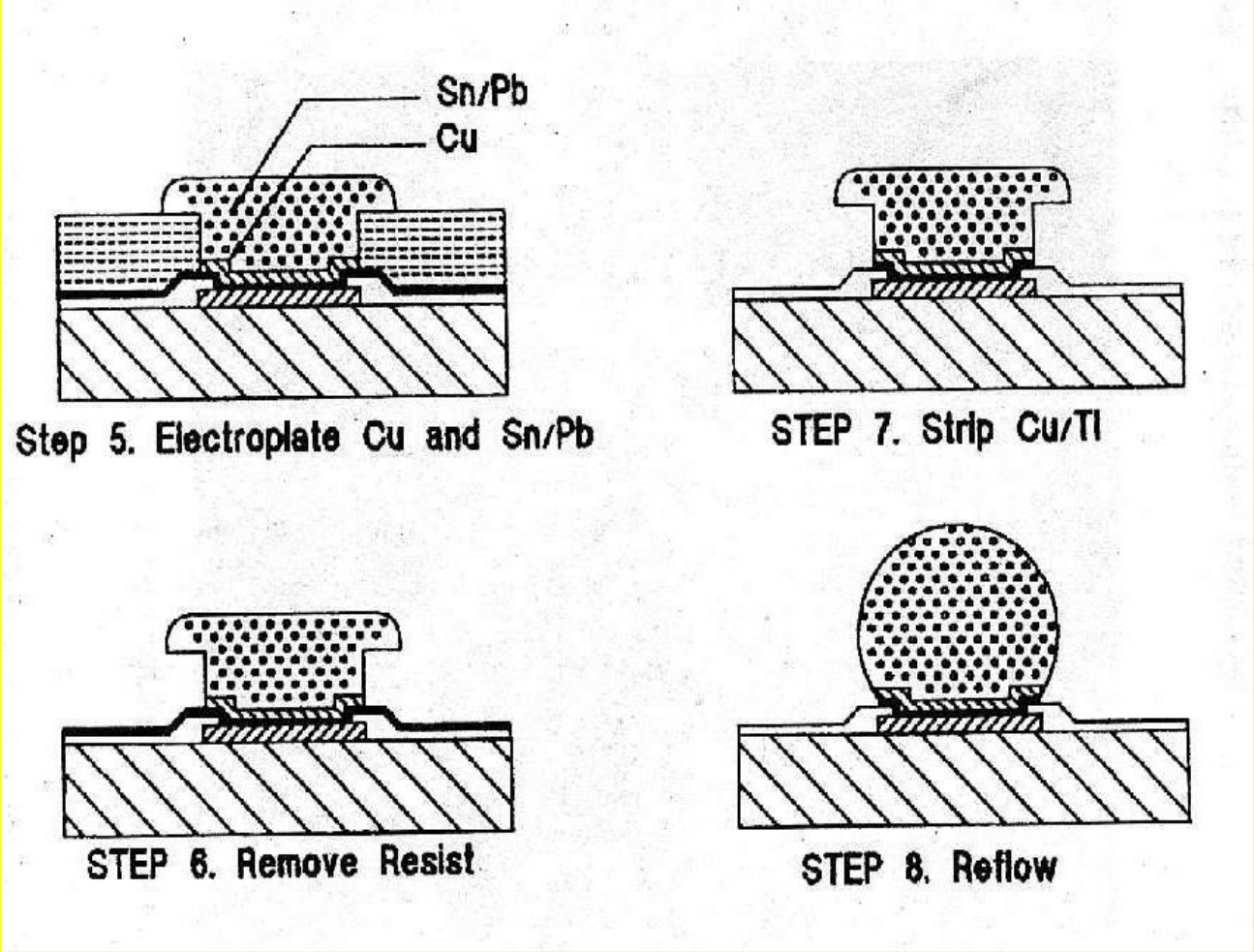
Flip Chip Solder Bump



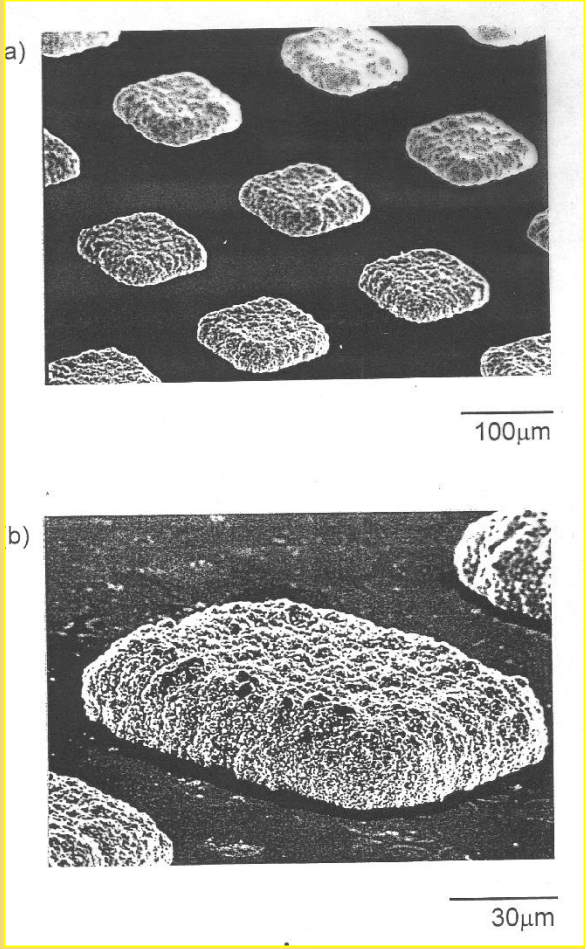
Bumping Process (1/2) – Ti/Cu UBM



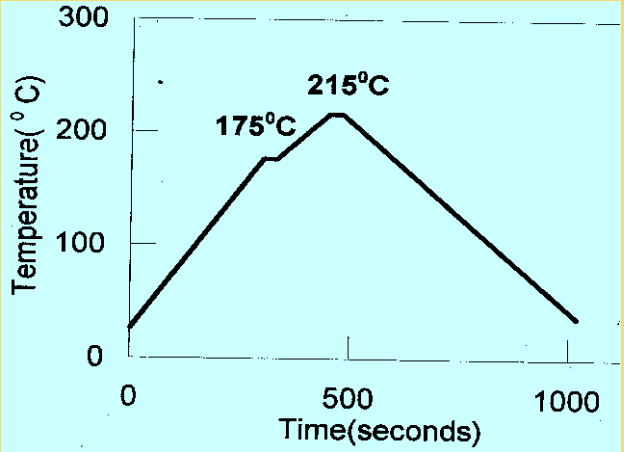
Bumping Process (2/2) – Ti/Cu UBM

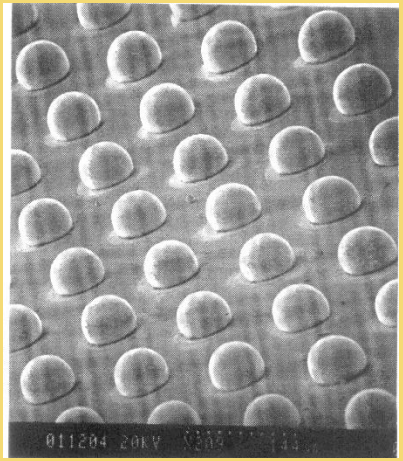


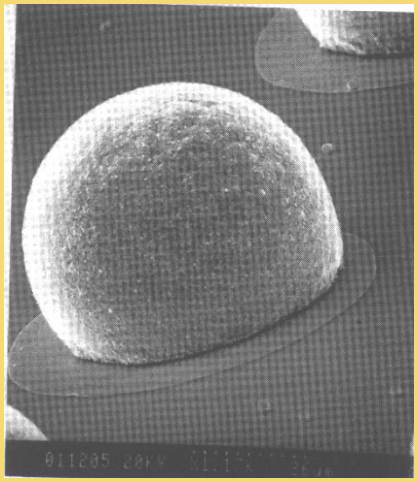
Electroplated Solder Bump



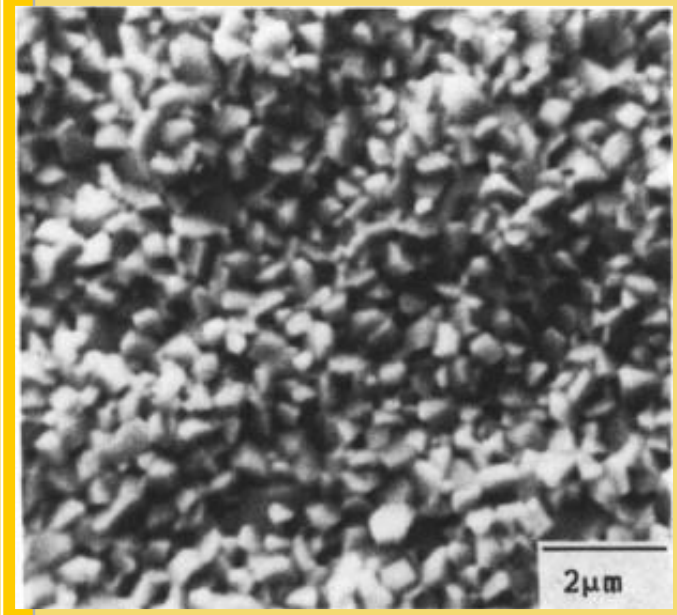
Reflow







IMC formed between Solder and Electroless Nickel Barrier Layer



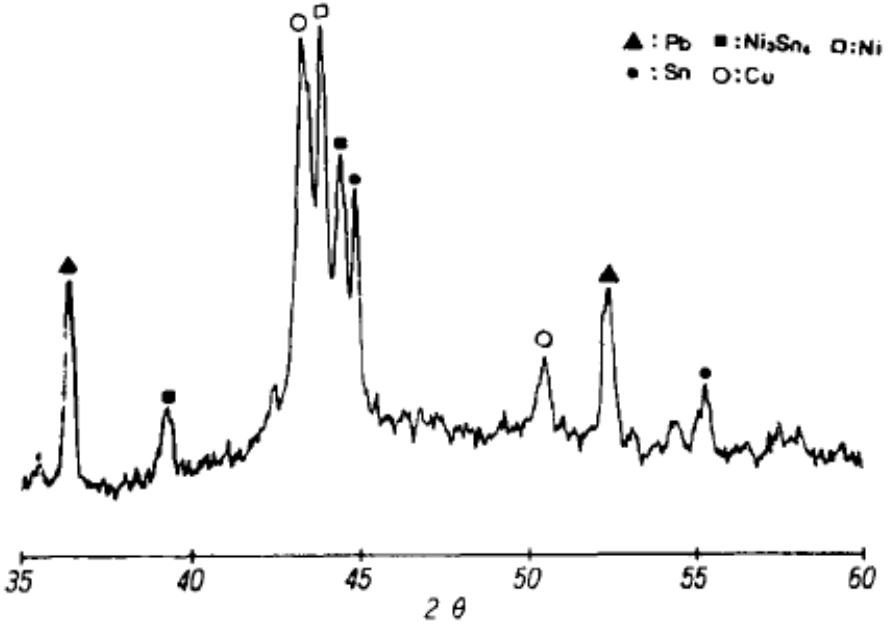
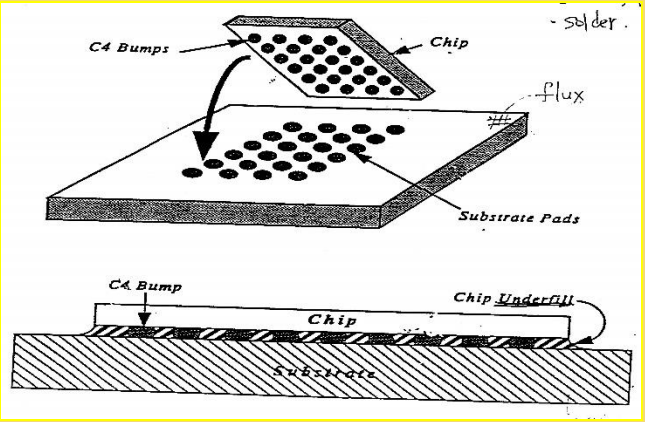


Fig. 7. X-Ray diffraction pattern of the compound layer formed in Al/Ni–Cu–P/Pb–Sn at 250 °C for 16 h, corresponding to Fig. 8.

C. Y. Lee and K. L. Lin, "The Interaction Kinetics and Compound Formation Between Electroless Ni-P and Solder," **Thin Solid Films**, 249, (1994) 201-206.

Flip Chip Bonding vs. Wire Bonding



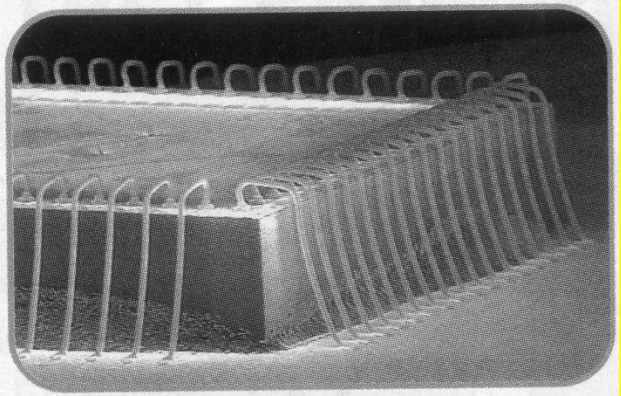
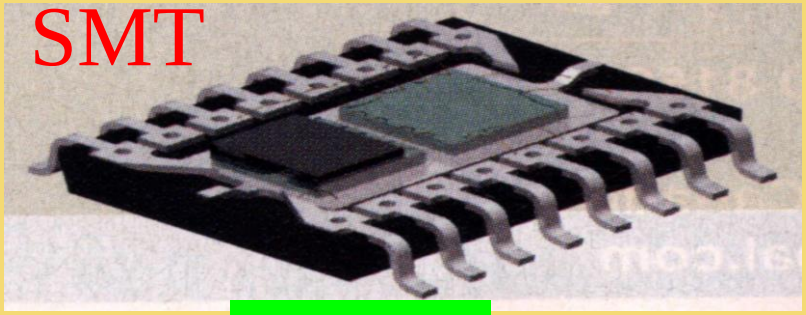


Figure 2. CSP loops created by a ball bonder. Special bends are formed that provide this shape with the second

- Flip Chip -
  - Bonding is performed at once, a gang bonding process
- Wire Bonding-
  - Bonding is performed one by one individually

Module Level Interconnect – Leaded and Leadless

SMT



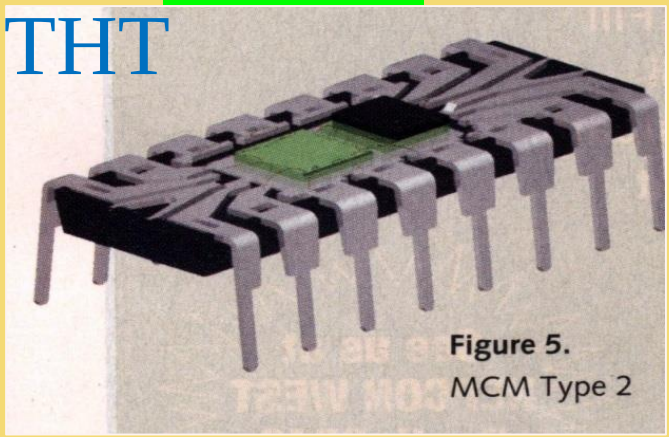
Surface Mount Technology

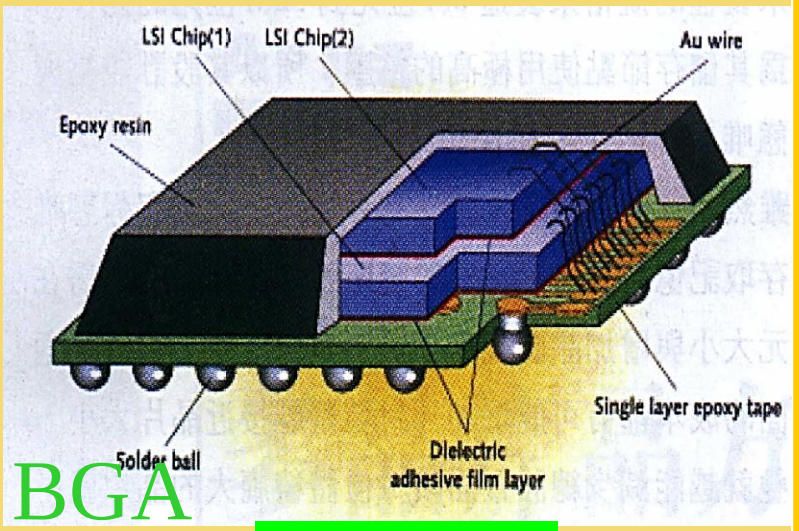
Through Hole Technology

Ball Grid Array

Leaded

THT

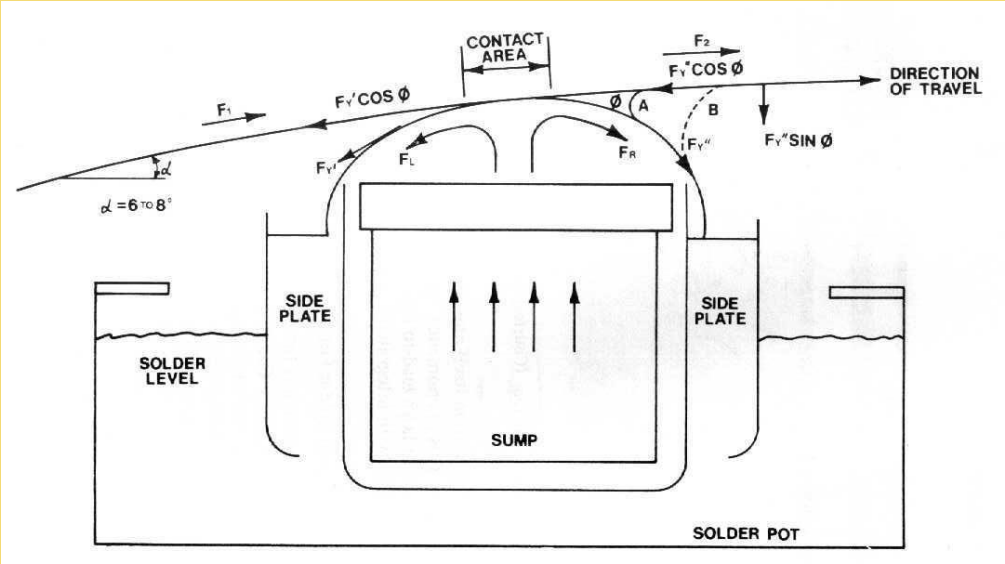


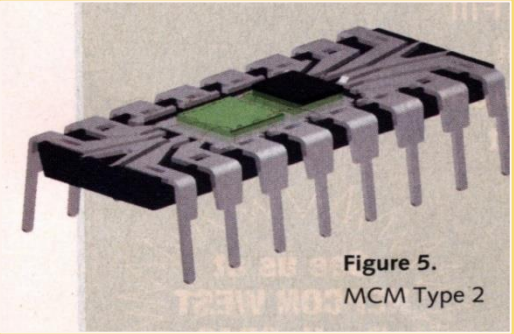


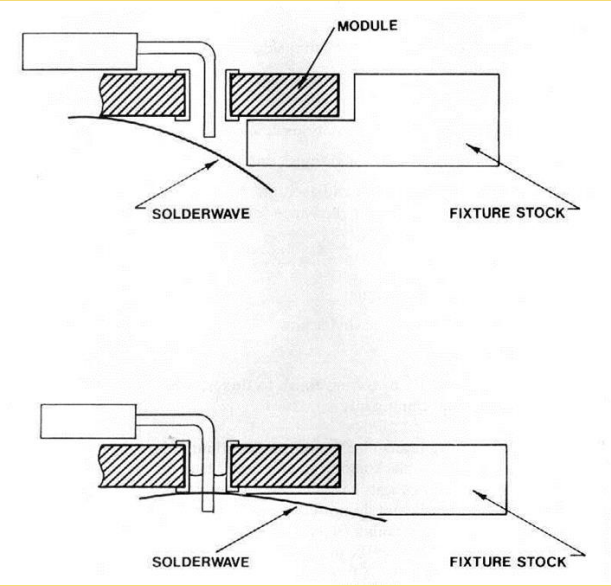
BGA

Leadless

THT – Wave Soldering

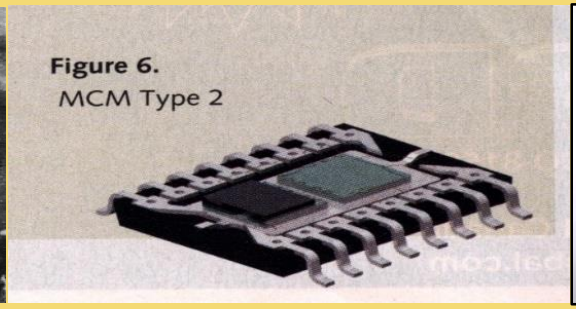


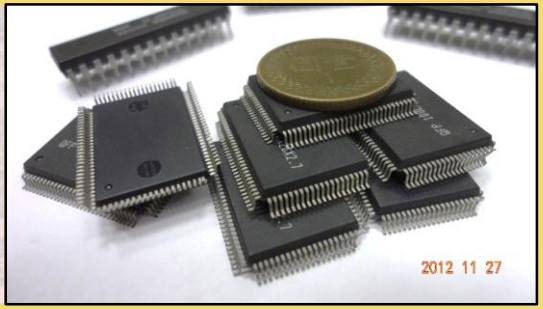




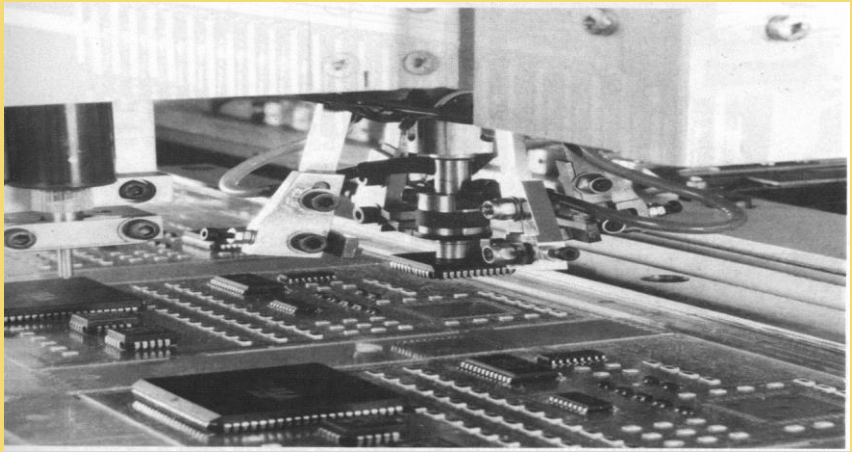
SMT Component - Pick and Place

R. J. K. Wassink, “Soldering in Electronics”, 2nd edn.





Pick and Place



Solder Paste

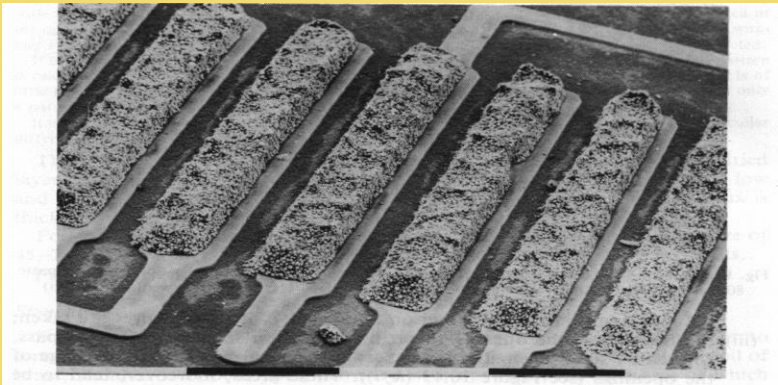
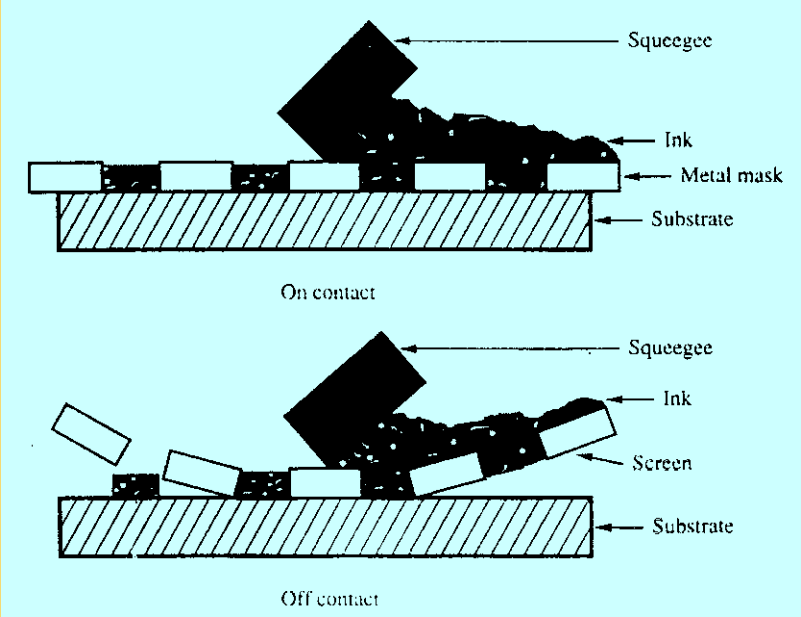
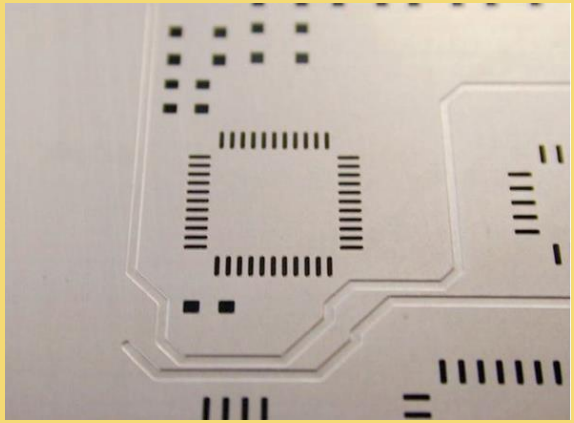


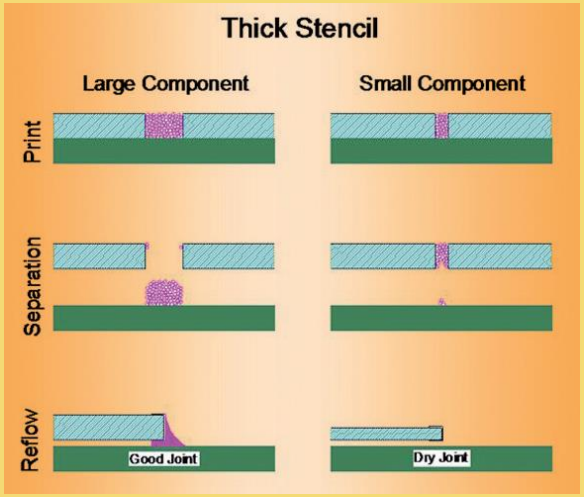
Fig. 10.11 Solder paste applied to solder lands of a VSO component with a pitch of 762 μm. The effect of the wires of the screen is still visible in the solder deposit. Note also the shift of the solder print with respect to the solder lands, due to tolerances of board and screen. The small amount of spilt paste (in the centre lower region) will, upon soldering, lead to a solder ball. (Courtesy of G. Teeuwen, Eindhoven)

Screen Printing of Solder Paste



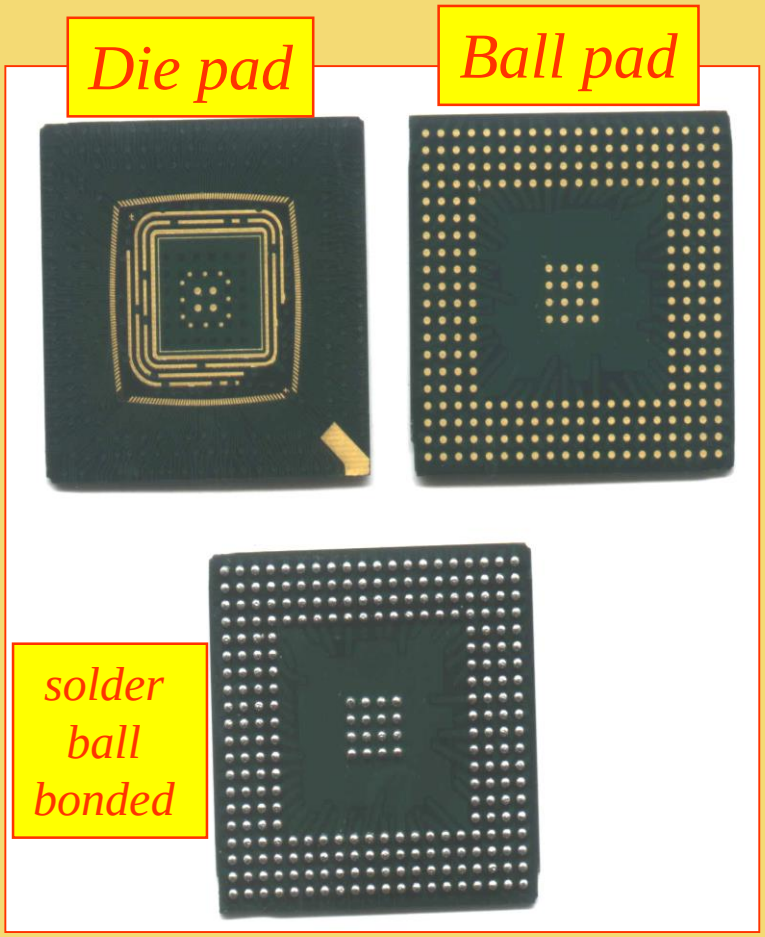
R. J. K. Wassink, "Soldering in Electronics", 2nd edn.





SMT Magazine • August 2011

BGA Substrate/Solder Ball



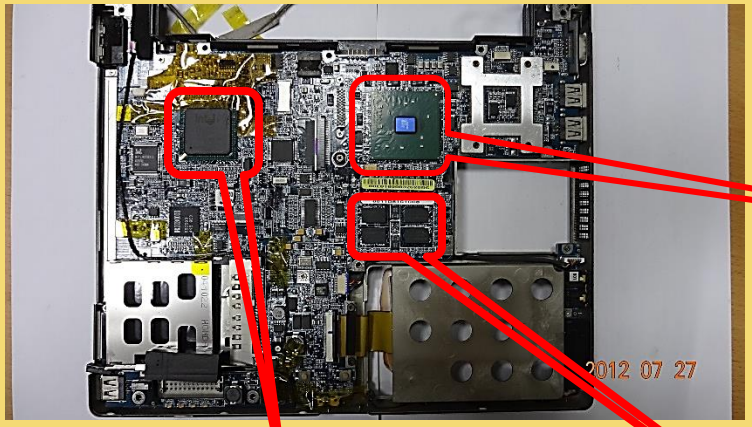
Ball size: 300 ~ 760 µm

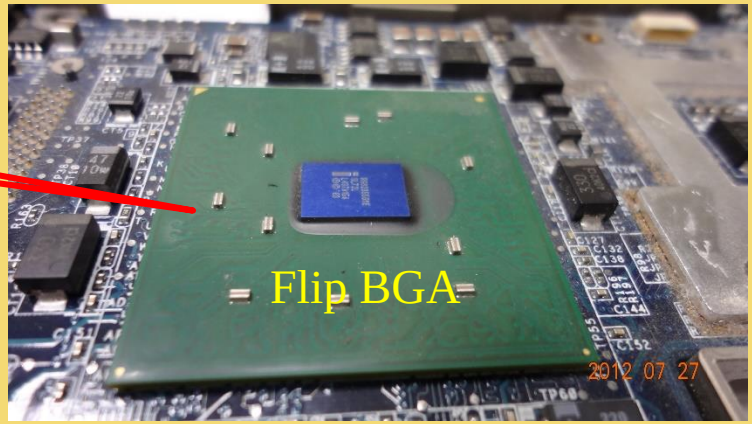
SMT Magazine • May 2011

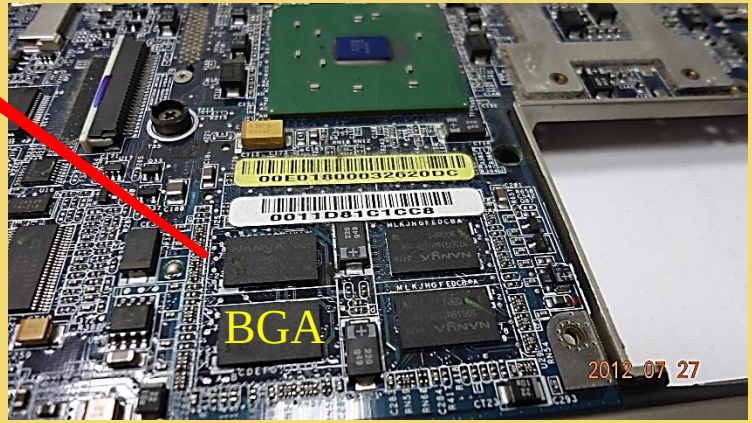
solder ball

Notebook –

packaged components





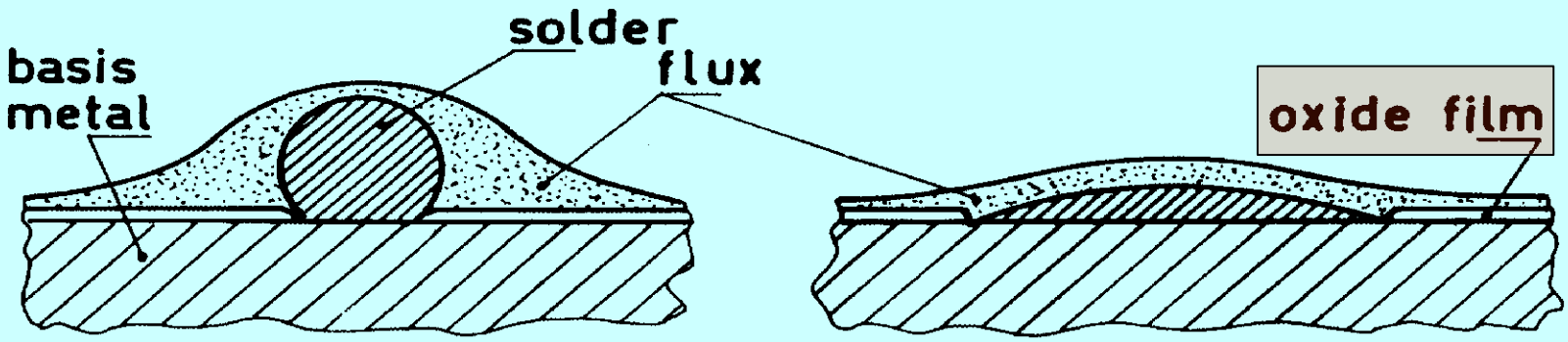


Solder Products (the form of solder) for Electronics Manufacturing

- Solder bump
- Solder preform
- Solder powder
- Solder paste
  - Solder powder + flux
- Solder ball
- Solder wire
- Solder ingot

Action of Flux and Soldering Occurrence

R. J. K. Wassink, "Soldering in Electronics" 2nd edn.



- Enhance wetting through:
  - Clean tarnish film on substrate (e.g., CuO)
  - Clean tarnish film on solder powder (e.g., SnO)
  - Lower surface tension of solder and substrate (air to flux atmosphere)

Sn-Pb Phase Diagram

Pb: (prohibited by WEEE, RoHS)

- Low price
- Enhance oxidation resistance
- Lower surface tension
  - 470 dyne/cm for 63Sn-37Pb at 230°C, 550 dyne/cm for Sn at 232°C
- Eutectic with Sn
- Toxic

Eutectic 183°C

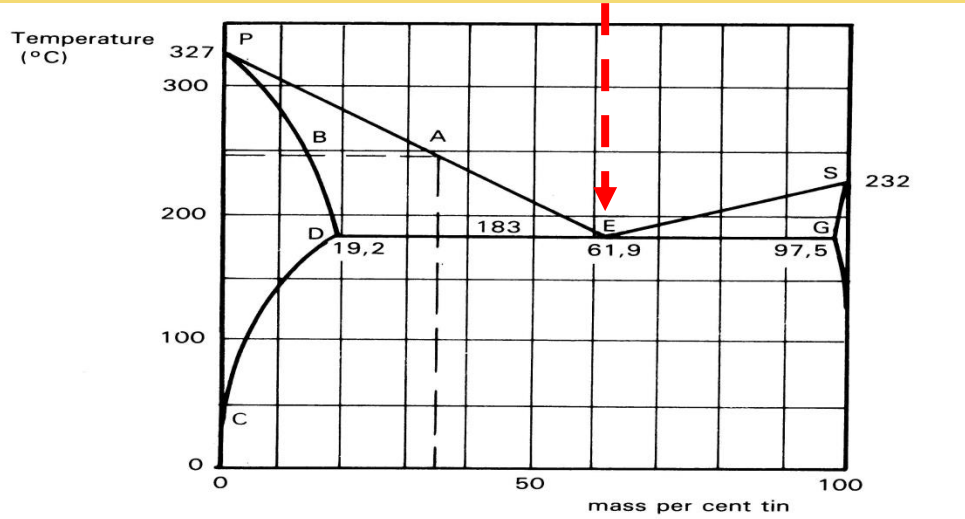


Fig. 4.2 Tin-lead phase diagram, showing the eutectic temperature of 183°C and the eutectic composition of about 62 mass % of tin.

Sn-Pb Phase Diagram

Sn-Ag Phase Diagram

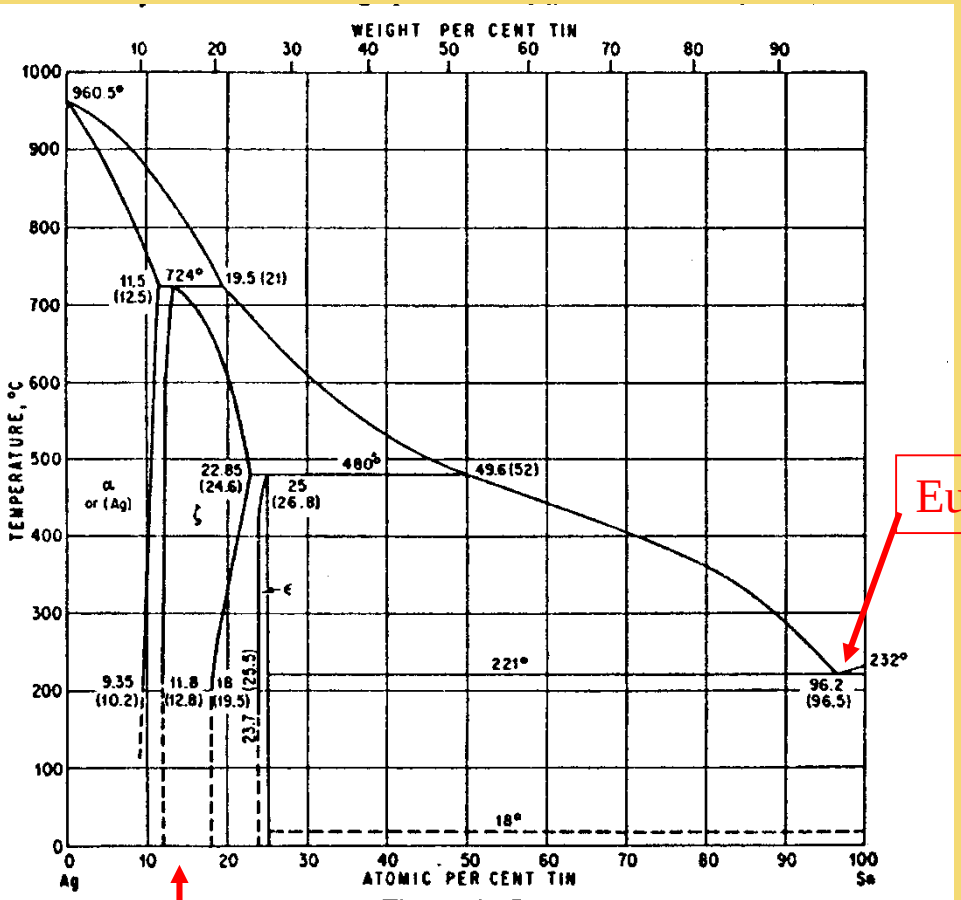


Fig. 33. Ag-Sn

Eutectic 221°C

Forms IMC at high Ag%

Sn-Cu Phase Diagram

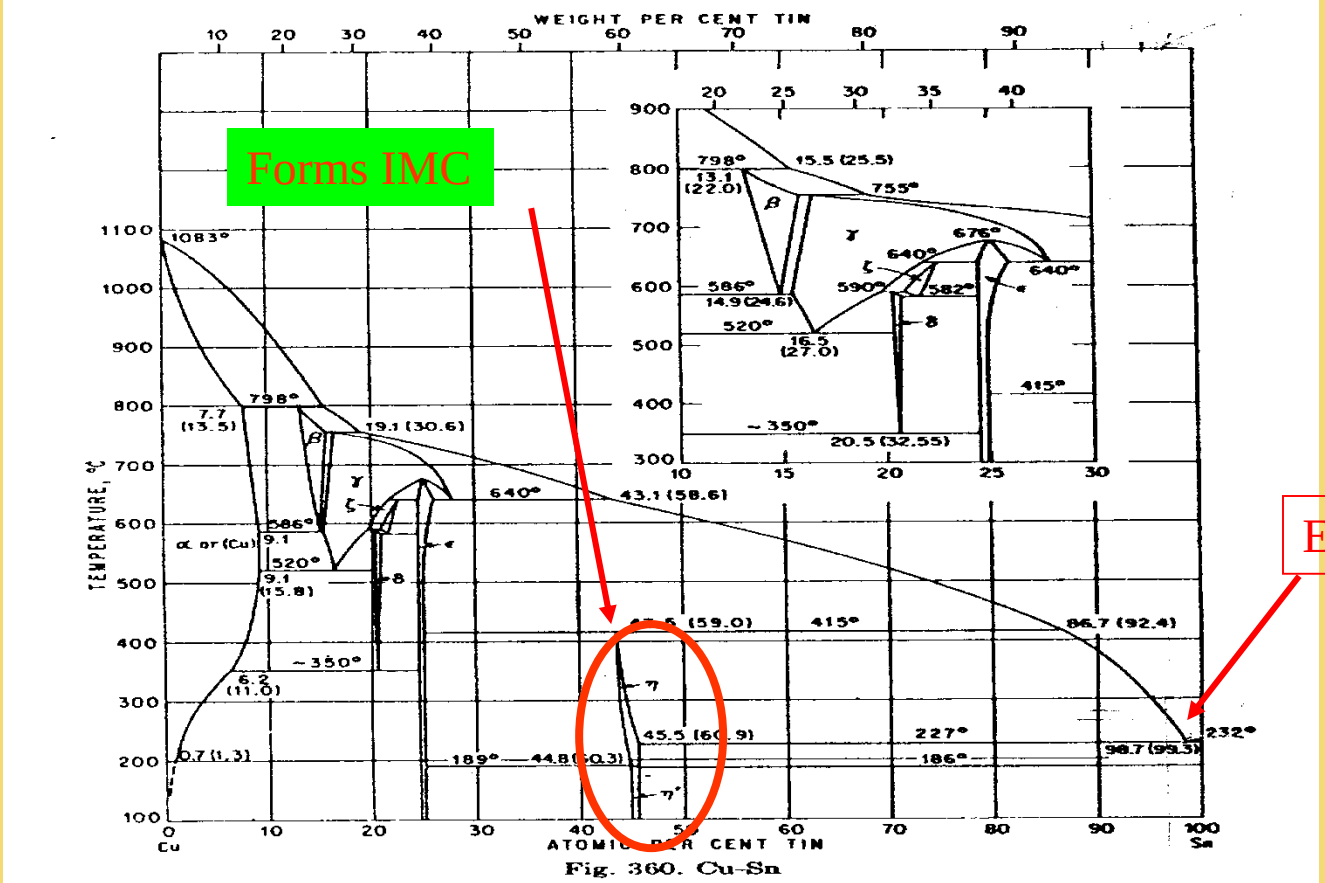


Fig. 360. Cu-Sn

Eutectic 227°C

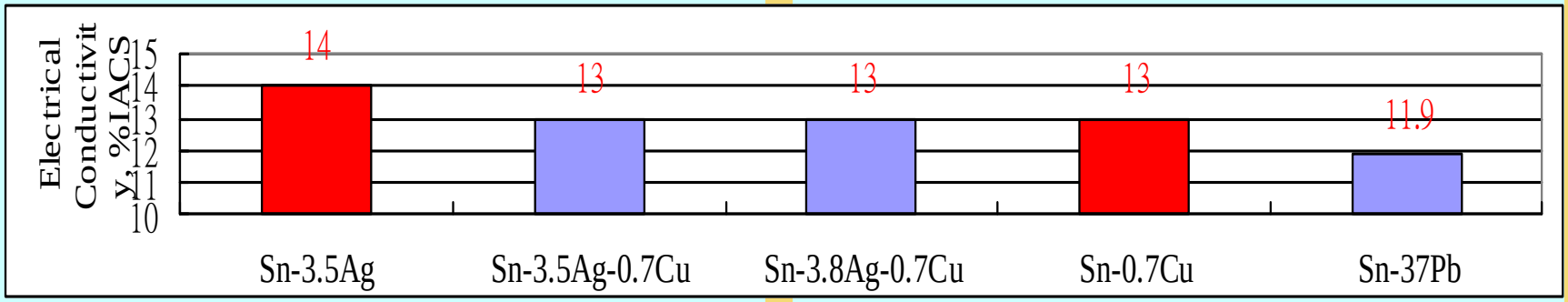
One of the major Pb-free solders: Sn-Ag-Cu

Eutectic Sn--Cu

- 99.3Sn-0.7Cu
- Eutectic temperature: 227°C

Eutectic Sn-Ag

- 96.5Sn-3.5Ag
- Eutectic temperature: 221°C



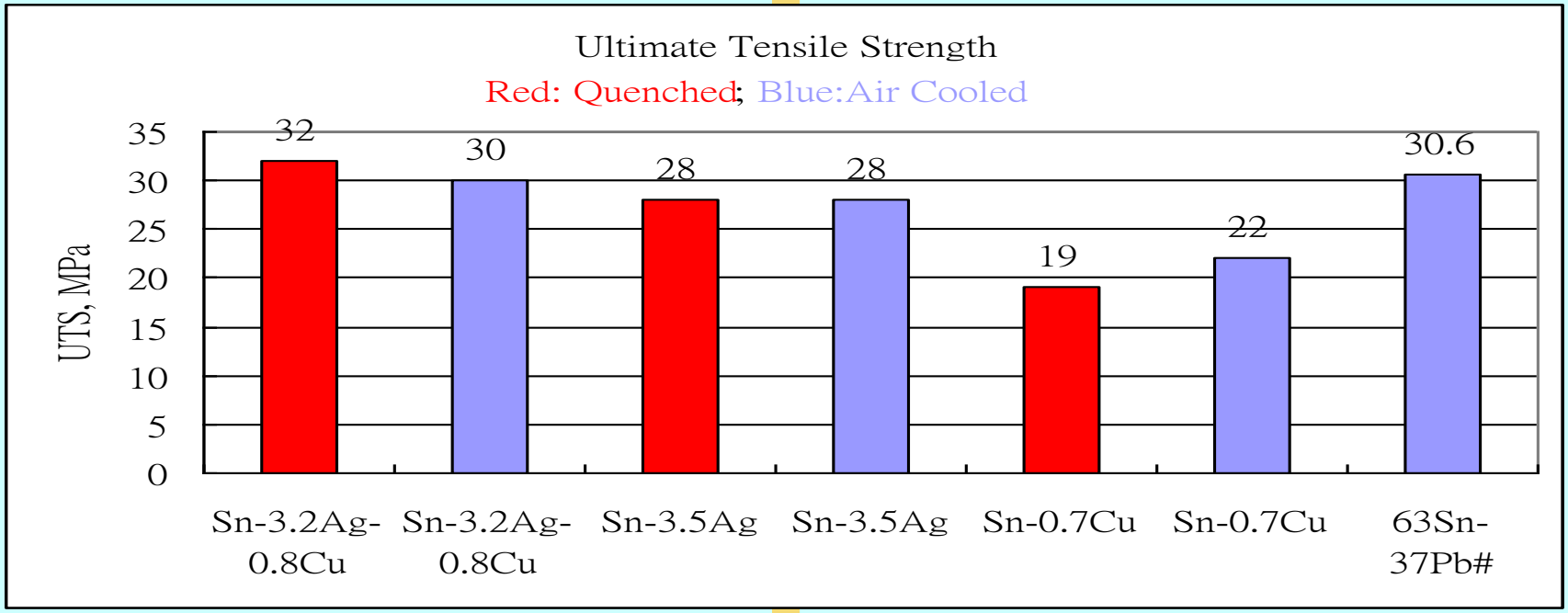
One of the major Pb-free solders: Sn-Ag-Cu

Eutectic Sn--Cu

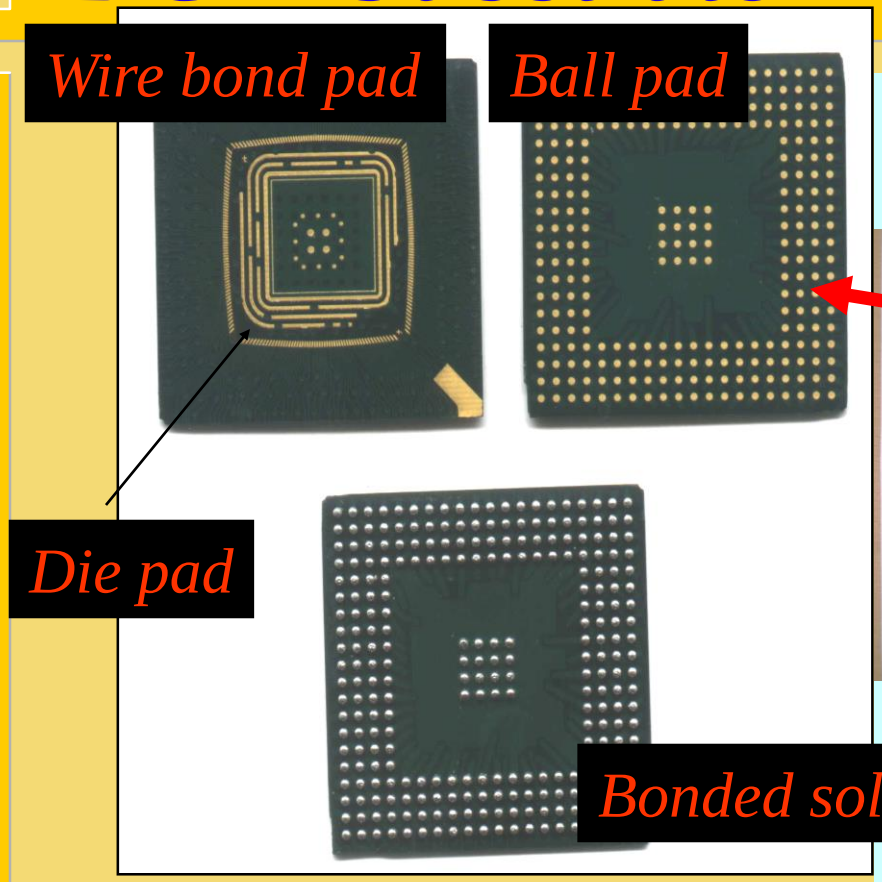
- 99.3Sn-0.7Cu
- Eutectic temperature: 227°C

Eutectic Sn-Ag

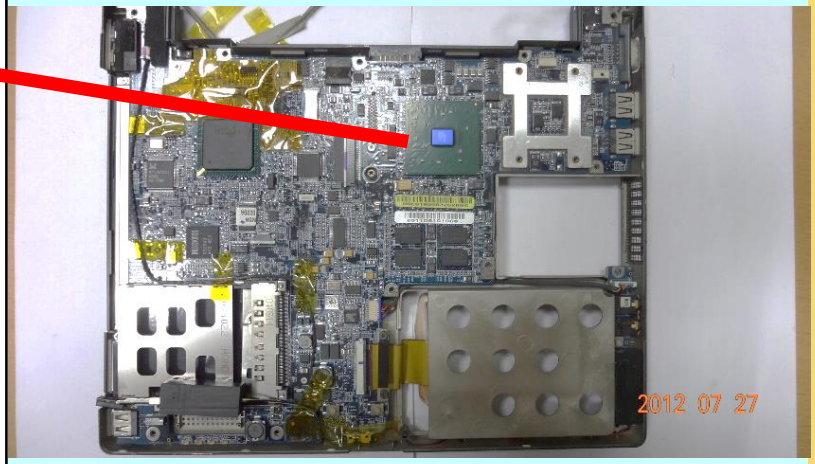
- 96.5Sn-3.5Ag
- Eutectic temperature: 221°C



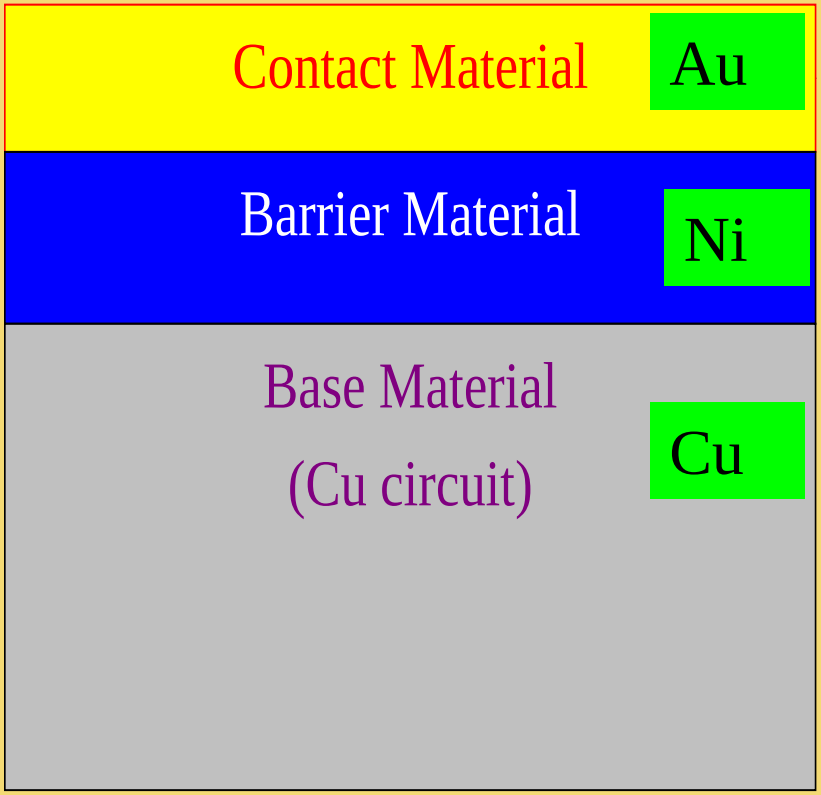
Substrate/Board Level Interconnects
BGA Substrate

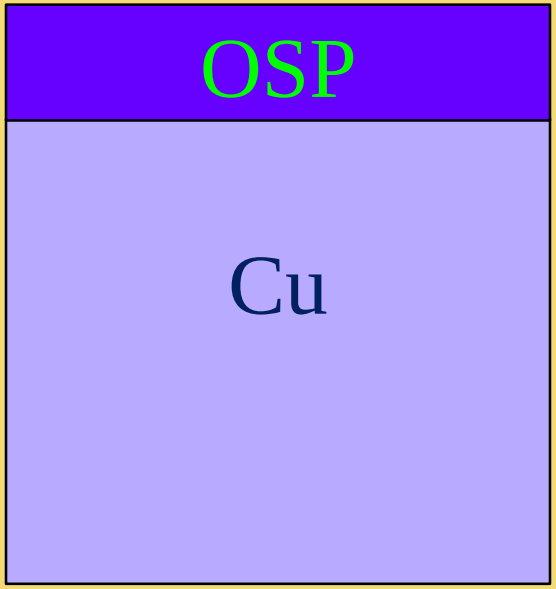


- Plastic substrate (BT)



Metallization on BGA Substrate

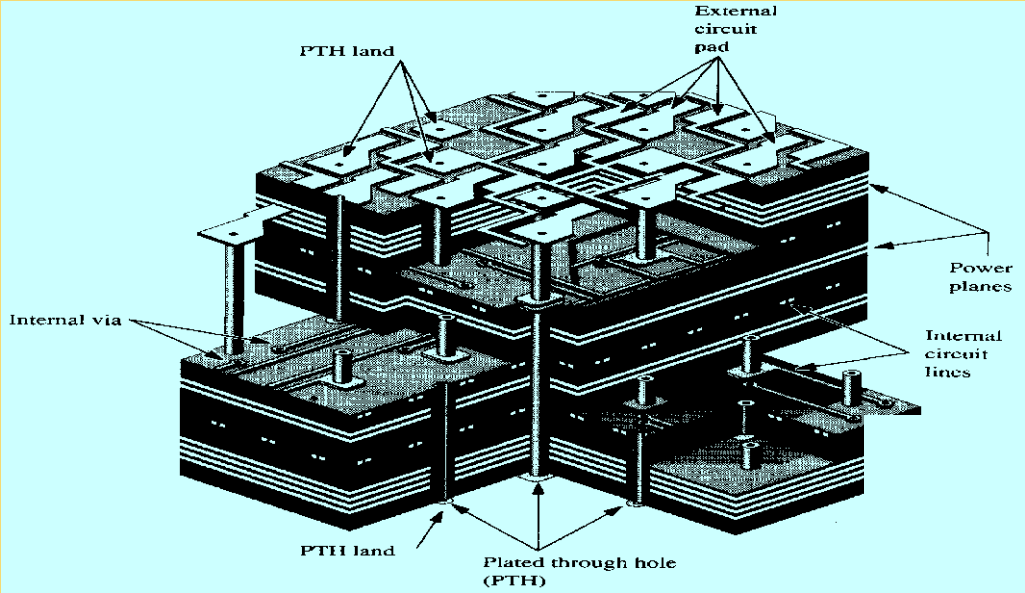


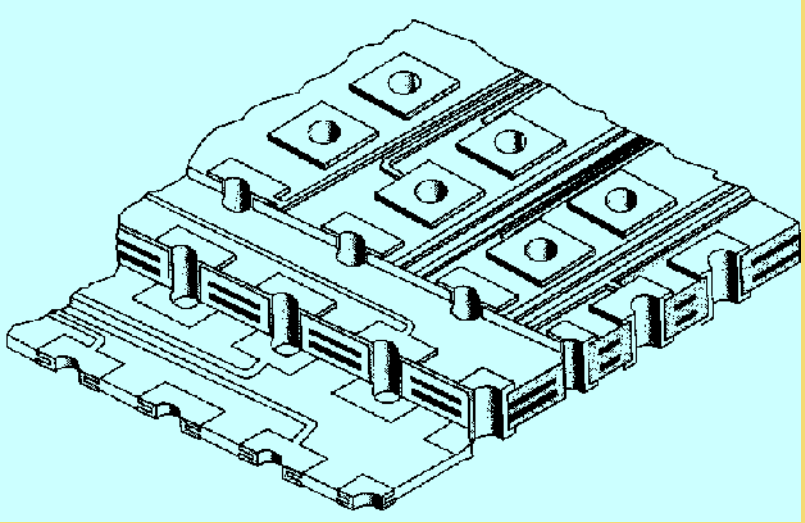


Organic solder preservative

3-D Sketch of PC Board

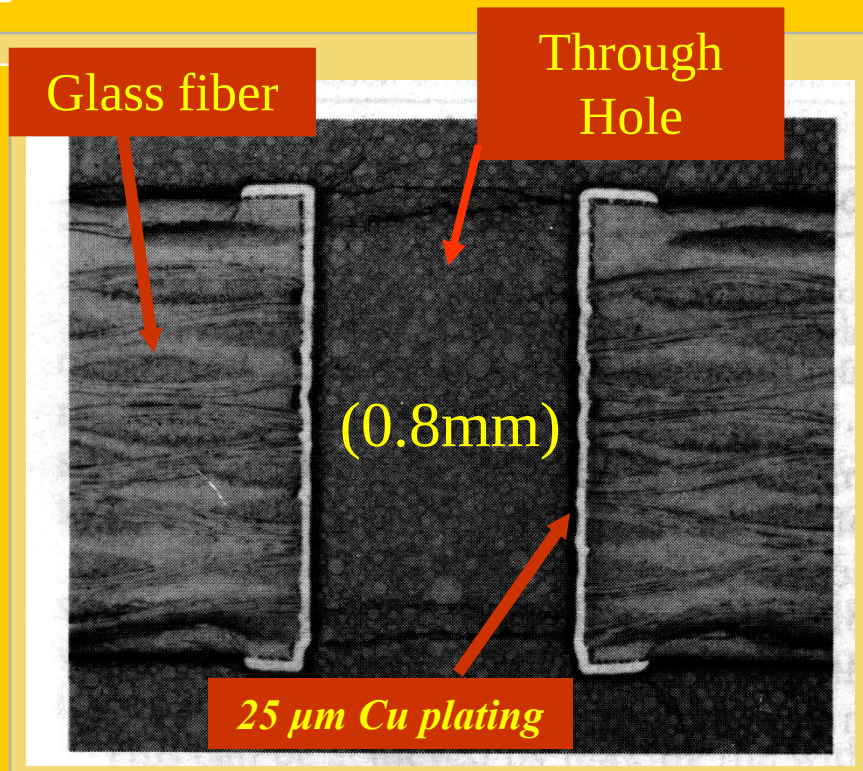
source: Principle of Electronic Packaging, C. Li





Plated Through Hole

Wassink, Soldering in Electronics



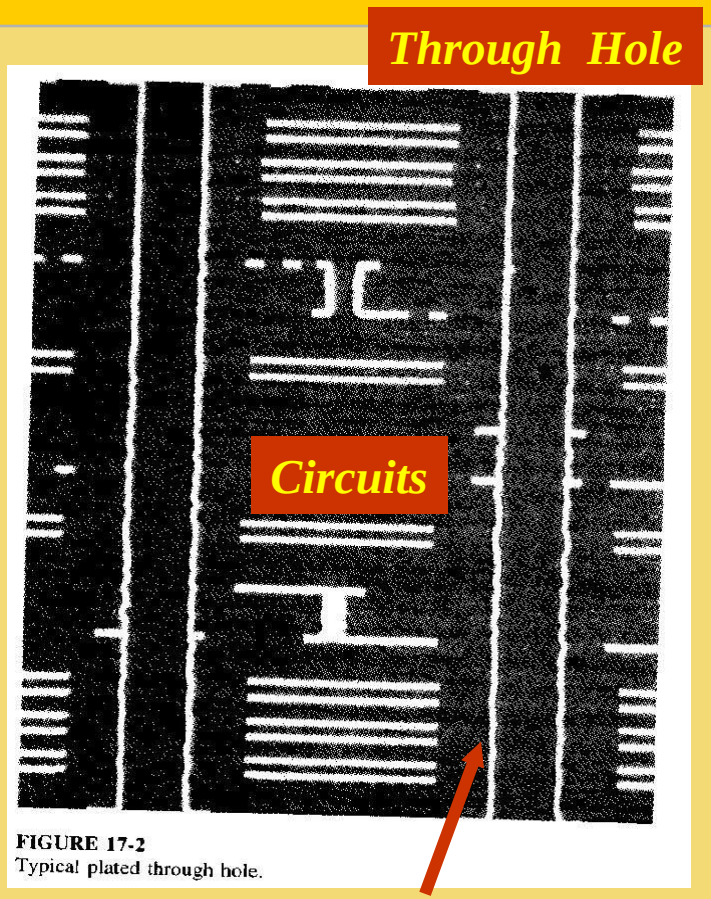


FIGURE 17-2
Typical plated through hole.

Through-Hole Activation (Electroless Cu Deposition) source: Principle of Electronic Packaging, C. Li

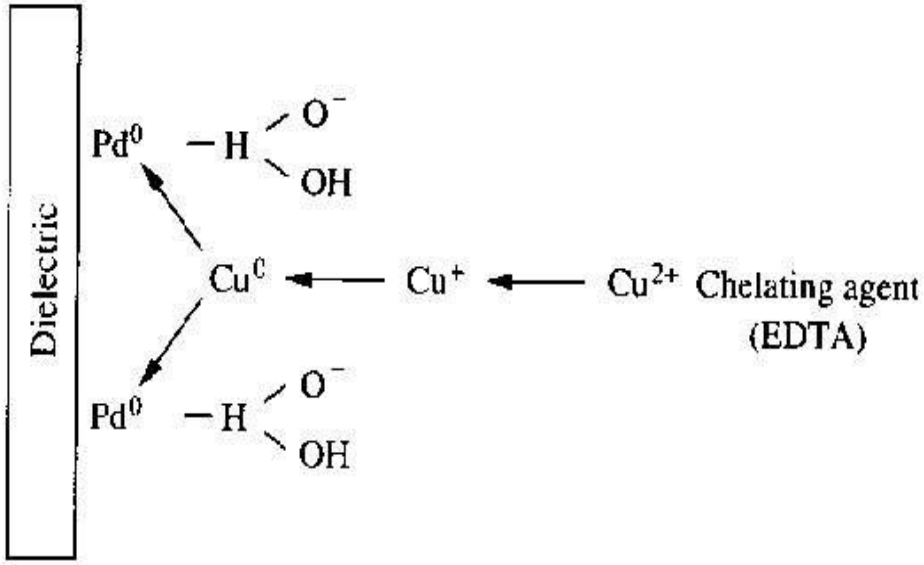


FIGURE 17-9
Reduction of Copper onto a catalyzed surface.

The electroless Cu provides the conducting base for electroplating.

Integration of Interconnects in Electronic Packaging

Integration of Interconnect Technology and Material – Stacked/3D IC Packaging

M. Kada and L.Smith, PanPacific Microelecronics Symposium Conference, Jan. 2000

Figure 6: Triple-chip Stacked CSP contribution to compact, light-weight cellular phones

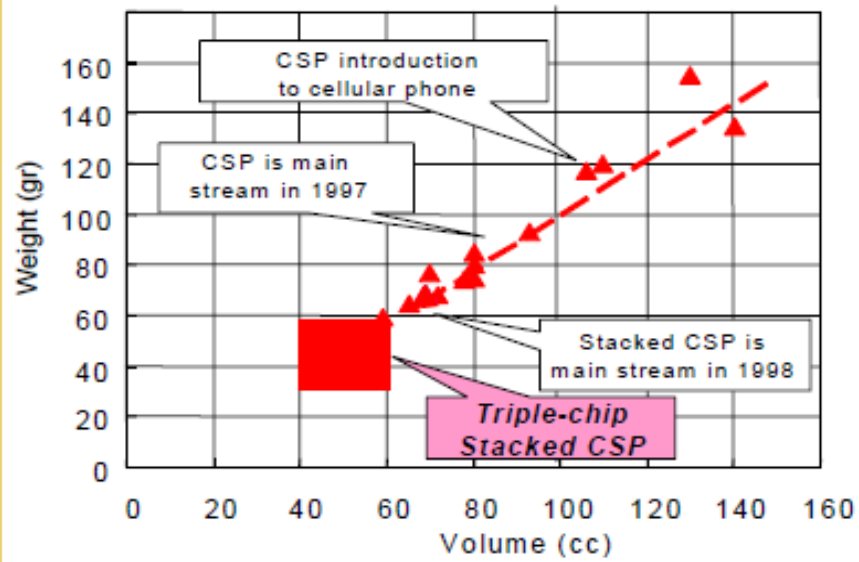


Figure 5: Triple-chip Stacked CSP Cross-section

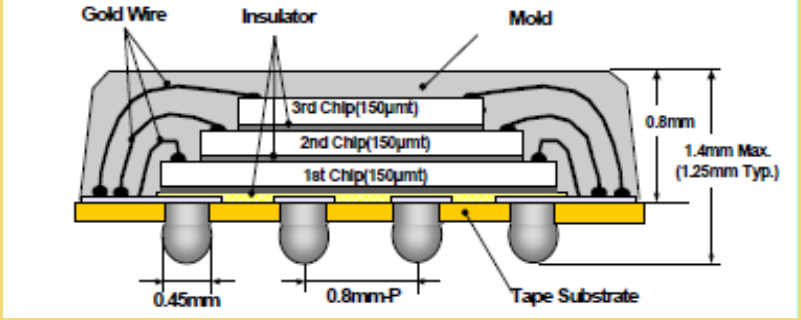
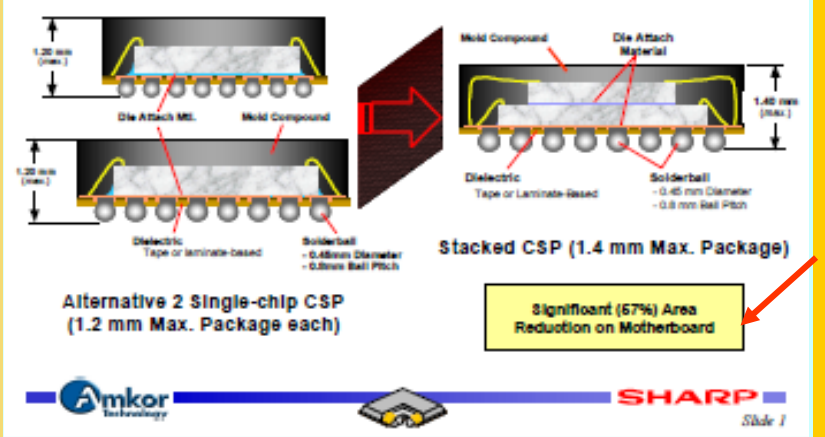
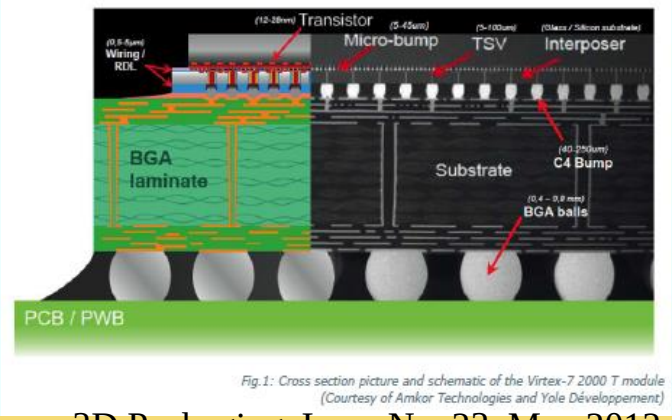


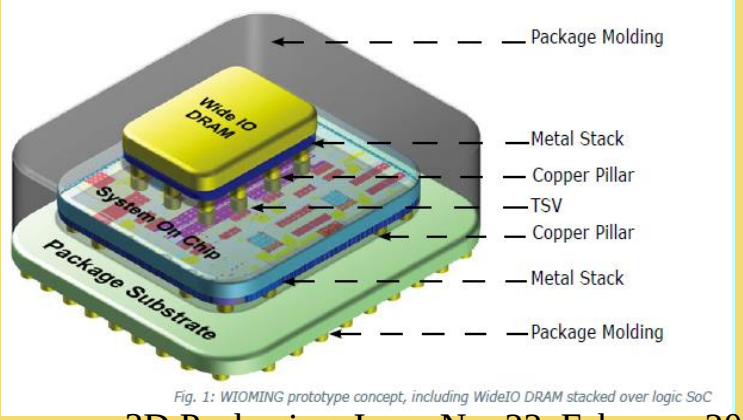
Figure 3: *Flash + SRAM Integrated into S-CSP*



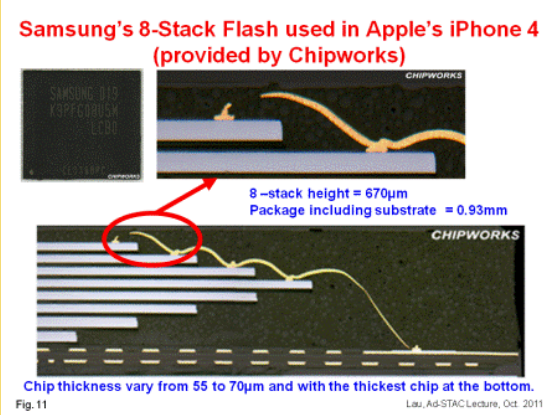
3D Packaging



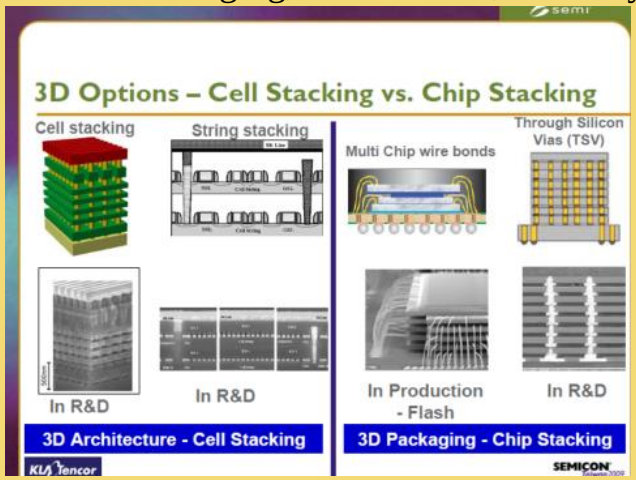
source: 3D Packaging, Issue No. 23, May 2012



source: 3D Packaging, Issue No. 22, February 2012



http://www.infoneedle.com/category/tags/wide-i/o?snc=20641



source: SEMICON Taiwan, 2009