3D Integration Technologies for Various Quantum Computing Devices

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INTRODUCTION

With the slowdown of transistor node scaling in the past decade, advanced three-dimensional (3D) integration technologies have been developed as an alternative approach for the continuity of Moore's law, specifically in reducing form factor, cost, power and increasing performance . By extending the conventionally two-dimensional layouts, assembly, and interconnections into the third dimension, 3D integration has progressively become the primary building block of advanced electronic devices. Depending on the interconnect hierarchy, 3D integration technologies can be classified into three categories: 3D System-in-Package (SiP, package or system level), 3D System-on-Chip (SoC, device level) and 3D monolithic integration (transistor level) [1].

On the other hand, quantum computing based on quantum mechanisms (i.e., superposition and entanglement) has been intensively investigated in the past two decades, in view of the superior potential in handling certain problems that are intractable for most advanced classical supercomputers. To realize quantum computing, various platforms with distinct physical implementations of quantum bit (qubit) are being developed simultaneously, including trapped ion, superconducting circuit, silicon spin, photon, topological qubits, etc. To date, the number of qubits that are fully connected is ~10 in most quantum computing devices. However, in the fault-tolerant quantum computing scheme, it is estimated that millions of physical qubits are required to build sufficient logical qubits (~1000) to run the useful quantum algorithms and demonstrate the quantum supremacy [2]. This yields significant challenges in scaling up the current devices to that broad blueprint. One of the possible solutions is to leverage the well-established CMOS fabrication process in semiconductor industry which builds billions of transistors in a fingernail-size chip. At the same time, 3D integration technologies can also be adopted to boost the scalability of qubits by extending to the third dimension either in a hybrid or monolithic manner. Similar to the classical electronics, the 3D integration in quantum devices can be also classified according to its hierarchy.

In the first part of this review, we summarize and classify the state-of-the-art 3D integration technologies that were employed in various quantum computing devices (trapped ion qubit, superconducting circuit qubit, silicon spin qubit, and photon qubit in silicon photonics), which are currently the most popular candidates due to their favorable manufacturability by leveraging the advanced semiconductor fabrication process. Subsequently in the remaining of this review, the advanced packaging and integration roadmap for ion trap in our group is presented, from substrate material evaluation to the through silicon via (TSV) integration, and finally to the cointegration of TSV, multilayer metallization and silicon photonics into ion trap.

TWO-LEVEL SYSTEM IMPLEMENTATION, GATE OPERATION, AND SCALABILITY BOTTLENECKS FOR DIFFERENT QUBITS

Trapped Ions Qubit

Trapped ions are dynamically confined and isolated from the environment by the RF electric field generated by the electrodes in an ion trap. Lasers with specific wavelengths are focused onto the ions for cooling, manipulation, and detection. The internal electronic states of the valence electron are encoded as qubit. We use optical qubit to illustrate the basic quantum operations. The rotation between states $|0\rangle$ and $|1\rangle$ can be simply performed by focusing a laser beam that resonant at the transition frequency. The shared motional mode in a string of ions can be used as a quantum bus to transfer information. Along with certain single qubit gate rotations, the entangled two qubit gate can thus be performed [3]. Currently, the most-widely used ion trap is surface electrode ion trap, where lithography-defined coplanar electrodes are used in place of the mechanically assembled rod electrodes [4]. Due to the compatibility with microfabrication techniques, surface ion trap with hundreds of electrodes has been demonstrated. However, to realize the actual large-scale ion trapping implementation, numerous challenges remain to be overcome. From the integration point of view, two respective challenges are overcrowding interconnection and on-chip integration of conventionally bulk components (e.g., voltage sources, mirrors, etc.).

With the development of ion trap geometry, certain electrodes located at the geometry center are inevitably surrounded by the peripheral electrodes, which cannot be accessed by bonding wires. Meanwhile, since wire bonds are laterally situated at the edges of a chip in a finite area, the increase of electrodes number will result in the interconnections overcrowding. To mitigate these issues, one needs to explore the third dimension of interconnections. Multilayer metallization (MM) and TSV were independently adopted in place of wire bonding to introduce additional degree of freedom for signal routing [5, 6]. However, both solutions feature some limitations (e.g., thick dielectric layer formation for MM, large diameter and pitch of TSV). Therefore, a combination of TSV and MM is foreseen in future ion trapping devices.

With the increasing number of trapped ions, the optical input and output interface for control and measurement of

individual ions from free-space optics is significantly compressed. Therefore, the integration of optical components becomes essential. At the beginning, bulk optics (e.g., fibers) were mounted into the traps in relatively brute-force approaches. Following that, for light collection, localized components like micromirrors and lenses were integrated and fabricated within ion trap to improve the coupling efficiency [7]. In addition, traps directly fabricated onto high-reflectivity or transparent substrates were also demonstrated [8]. However, these integrations were still limited by the customized fabrication process. Until year 2016, a waveguide and grating coupler integrated ion trap was demonstrated, where a SiN layer as core layer for photonics components is introduced underneath surface electrode and CMOS-compatible fabrication process is used [9]. Besides, it is necessary to highlight that the conventionally bulk passive and active electronic components (e.g., capacitors and digital-to-analog converters) were also on-chip integrated [10, 11].

Superconducting Circuit Qubit

At sufficiently low temperature ($kT \ll \hbar\omega$), the potential of a resonant circuit consists of a capacitor and inductor becomes quantized with a constant energy difference ($\hbar\omega$, harmonic oscillator). By introducing a Josephson Junction into the circuit, the energy difference turns into anharmonic, enabling specific state addressing and thus the encoding of qubit. We use the most popular transmon qubit as an example to demonstrate the quantum operations for superconducting qubit. The single qubit gate is predominately driven by coupling a microwave signal (5-10 GHz) via a coplanar waveguide line. For two qubit gate, two neighboring transmon qubits are normally coupled through a capacitor in between (capacitive coupling). In addition, the qubit transition frequency can be dynamically tuned by incorporating a dc superconducting quantum interference device (dc SQUID), which is essential for both single and two qubit gates implementation [12]. For superconducting circuit readout, dispersive readout is typically used by coupling the qubit to a transmission line resonator [13]. In summary, all components that are required to define, manipulate and readout superconducting qubits are macroscopic circuits, which can be patterned on the superconducting films with lithography-based techniques. This makes it inherently compatible with advanced CMOS process and thus promising for large-scale realization. However, some challenges are remained.

As differed from large array of classical bits in memory that can be parallel addressed using Word or Bit lines, every single superconducting qubit requires independent circuits designed for control, readout, and qubit-qubit coupling, resulting in huge footprint and interconnection overhead. Meanwhile, most of the circuit layouts are still in a 2D scheme, where interconnections for various signals can only access the qubits via chip perimeters. In the Sycamore processor demonstrated by Google in 2019, a rectangular array of 54 qubits took a surface area of ~10×10 mm^2 [14]. Therefore, to scale up the 2D scheme and maintain the qubit addressability, 3D integration technologies are essential.

Similar to the integration roadmap for ion trap qubit, superconducting multilayers were first introduced. However, the obtained coherence time is generally shorter as compared to the qubits with single layer structure. This is limited by the interlayer coupling as well as the disturbance from natural defeats in the interlayer amorphous materials. To mitigate this challenge, a 3D integrated superconducting qubit scheme was proposed in 2017 [15]. This scheme consists of three bonded chips that are individually fabricated. The top chip is the qubit chip which contains qubit circuits, and the bottom chip is for readout and interconnection. To bridge these two chips, an interposer chip that incorporates superconducting TSV is bump-bonded in between. With this

TABLE I
COMPARISON OF VARIOUS QUANTUM COMPUTING DEVICES

Qubit type	Temperature and vacuum	Control signal	Feature size	Pitch between qubits	Challenges to scale up	Commercialization
Ion Trap	Ambient and ultra-high vacuum^	Lasers, RF and DC voltage	~5 μm (gap width between electrodes)	~10 μm	a. flexible interconnection b. electrode and photonics fabrication node difference c. off-chip light alignment with ions	IonQ, Honeywell
Superconducting circuit	~10mK and high vacuum*	Microwave current, DC current, RF control[#]	~50 nm (Josephson Junction)	~1 mm	a. complex circuit layout b. cryo-electronics c. noise shielding and filtering d. entangle with neighboring qubits only	IBM, Google
Silicon spin	1K and high vacuum*	DC magnetic field, AC magnetic field, DC voltages, RF control[#]	~50 nm (gate electrode)	10-100 nm	a. multiple quantum dots placement and alignment b. complex electrodes layout c. cryo-electronics d. noise shielding and filtering	Intel
Photons	Ambient and atmosphere	Lasers, DC voltage, RF control[#]	200 nm (waveguide)	~200 μm	a. high efficiency single photon source and detector b. the integration and alignment with waveguide circuit	PsiQuantum, Xanadu

^Cryogenic apparatus in ion trapping test also benefits for anomalous heating reduction; * The high vacuum (down to 0.1 mbar) is required by the dilution refrigerator; [#]RF control is required for the pulsed operations within qubit lifetime. Table used with permission from [24].

scheme, the capability for complex interconnection routing is maintained in the bottom chip, while the qubit performance in the top chip will not be degraded.

Silicon Spin Qubit

Silicon spin qubits are encoded on the spin of electrons, that either bound to the embedded dopants or quantum dots (MOS and SiGe material systems are commonly used to define quantum dots). We use the simplest spin qubit defined by single electron as an example to demonstrate the quantum operations for silicon spin qubit. An in-plane large static magnetic field is required to create the Zeeman splitting. The single qubit gate is achieved using electron spin resonance (ESR) technique, in which an AC current is sent into a transmission line close to the qubit and thus generate a localized AC magnetic field resonant with spin transition frequency. The two qubit gate is implemented via the exchange interaction. For the qubit readout, a process known as spin-to-charge conversion is used, where the qubit electron is coupled to a single electron transistor (SET), and under specific conditions spin-up electron will tunnel to the electron reservoir and produce a detectable current pulse. We note that all these basic operations are controlled and enabled by appropriate voltages tunning on the corresponding gate electrodes located on top of qubits [16].

In terms of the compatibility with CMOS process, a silicon spin qubit geometry derived from the field effect transistor (compact two gate FET) was developed in 2016, where two top gates were respectively used to control two quantum dots that defined in the silicon channel (one qubit dot and one sensing dot in series). This work started from the standard CMOS process in transistor fabrication and adapted it to achieve the quantum functionality [17]. Similar to the superconducting circuit qubits, even in a huge array of millions of qubits, the independent control from multiple gate electrodes is anticipated to be indispensable for every single silicon spin qubit, posing significant challenges to the qubit architecture itself as well as the quantum-classical interface. To mitigate the first challenge, a 3D architecture was proposed in the qubit level, where the sensing dot was repositioned to the layer underneath the qubit dot and a tunnel barrier was introduced in between to transmit electron [18]. In terms of the interface overcrowding, a conceptual 3D integration architecture was also proposed for future quantum computer processor where the bottom layer and top layer of a silicon-on-insulator wafer were respectively used to accommodate qubits array and classical transistors for control [19].

Photon Qubit in Silicon Photonics

Photons are appealing to be used as qubits since they are almost free of decoherence. With that, the stringent environmental conditions (e.g., millikelvin temperature and ultra-high vacuum) as required by other qubit candidates can be eliminated, enabling photon qubits with high scalability. Besides, with the development of silicon photonics, photons can be routed by waveguides on a microfabricated chip, making the scale-up even more feasible. Though the single qubit rotation can be straightforwardly performed using waveplates and beam splitters, the two-qubit gate (i.e., Controlled NOT gate) implementation for photons become significantly more complex due to the large resource overhead required by the linear optics. Different from the abovementioned qubit candidates that have demonstrated single and two qubit gates but lack scalability, photon in waveguide circuits is naturally scalable thanks to the silicon photonics advancement. However, the challenge is to make it quantum, or more particularly, to achieve the entangled logic gate efficiently, which requires further theoretical and experimental innovations. Currently, one of the key requirements is to develop high efficiency single photon sources and single photon detectors, which are integratable to the sophisticated photonics circuit [20].

In 2016, a pick-and-place technique was developed for the integration of quantum dots single-photon source into ion trap. This technique allows for the precise alignment and high coupling efficiency between quantum dots and waveguide circuits [21]. Similarly, in 2015, a micrometer-scale flip chip method was demonstrated to transfer ten superconducting nanowire single photon detectors (SNSPDs) onto the same photonic circuits [22]. Based on separate fabrication and individual pre-selection of SNSPDs and photonic circuits, a 100% device yield was achieved. In addition to those single photon sources and detectors that integrated into the photonic circuits in an out-of-plane approach, novel 3D waveguide circuits can be built using the femtosecond laser direct-write technique by focusing the laser beams at different depth in the substrate [23].

We use Table I to compare and summarize the scalability requirements and bottlenecks of the abovementioned four qubit candidates. The current solutions using 3D integration technologies are classified based on the integration

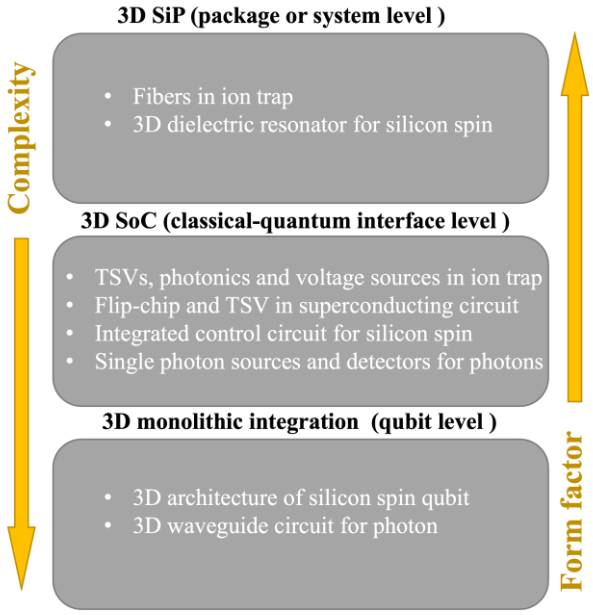

Fig. 1. The hierarchy of 3D integration technologies used in various quantum computing devices. Panel used with permission from [24].

hierarchy, as shown in Fig. 1. A more detailed description is given in [24].

3D Heterogeneous Integration RoadMap for Ion Trap

Substrate Material Evaluation

In our group, the integration roadmap of surface electrode ion trap starts from the material selection for the ion trap substrate (Fig. 2 (a-c)). The key requirements are low RF loss and high manufacturability. Silicon is always in the shortlist due to the CMOS compatible fabrication process. However, to mitigate the lossy issue of silicon, two possible solutions are proposed: the use of high resistivity silicon (>750 Ω · m) and the incorporation of grounding plane. Meanwhile, due to the development of glass fabrication technology in commercial foundries, glass has become a popular substrate especially for high frequency devices. Therefore, ion trap on glass substrate is also investigated. The electrical performances of traps on different substrates are compared in terms of leakage current, parasitic capacitance, on-chip RF loss and post-packaging resonance [25]. Ion trap on glass substrate demonstrates smaller capacitance (<1 pF) and lower RF loss (insertion loss of <0.05 dB at RF frequency of 50 MHz), as compared to the silicon counterparts. The ion trapping test on the glass trap is performed and up to four $^{88}Sr^{+}$ ions are successfully confined [26]. For single ion, the averaged lifetime is ~30 minutes.

TSV Integration

To simultaneously leverage the established fabrication technique of silicon and superior insulation property of glass, we further demonstrate a novel ion trap design with heterogenous integration of silicon and glass, acting respectively as ion trap and interposer substrate [6, 27]. The vertical connection between the silicon ion trap and the glass interposer is achieved by TSV (Fig. 2 (d, e)). We highlight all the fabrications of various traps are performed with the standard CMOS back end of line process on 12-inch wafer fabrication platform. Due to the integration of TSV, the original wire bonding pads on trap surface are eliminated. Consequently, the form factor of TSV integrated ion trap is reduced by more than 80%, minimizing the parasitic capacitance from ~30 pF to ~3 pF. Meanwhile, excellent ultra-high vacuum (10^{-11} mbar) compatibility of the packaged ensemble (trap, interposer and micro-bumps) is observed. In ion trapping test, the obtained heating rate (17 quanta/ms for an axial frequency of 300 kHz) and lifetime (~30 minutes) of TSV trap are comparable with traps of similar dimensions, indicating no additional decoherence source is introduced by the TSV integration.

Multi-module Integration

To move forward, the integration of other functional modules (silicon photonics and multilayer metallization) into TSV trap is proposed and the fabrication is ongoing. In silicon photonics module (Fig. 2(f)), waveguide and grating coupler are on-chip introduced in place of bulk optics to achieve localized light routing and emission [28]. Two different grating coupler designs which are correspondingly used for wavelengths of 1,092 ($^{88}Sr^{+}$ ion, repumping) and 422 nm (cooling and readout) are included. Based on the FDTD simulation result, the beam size of the light emitted from

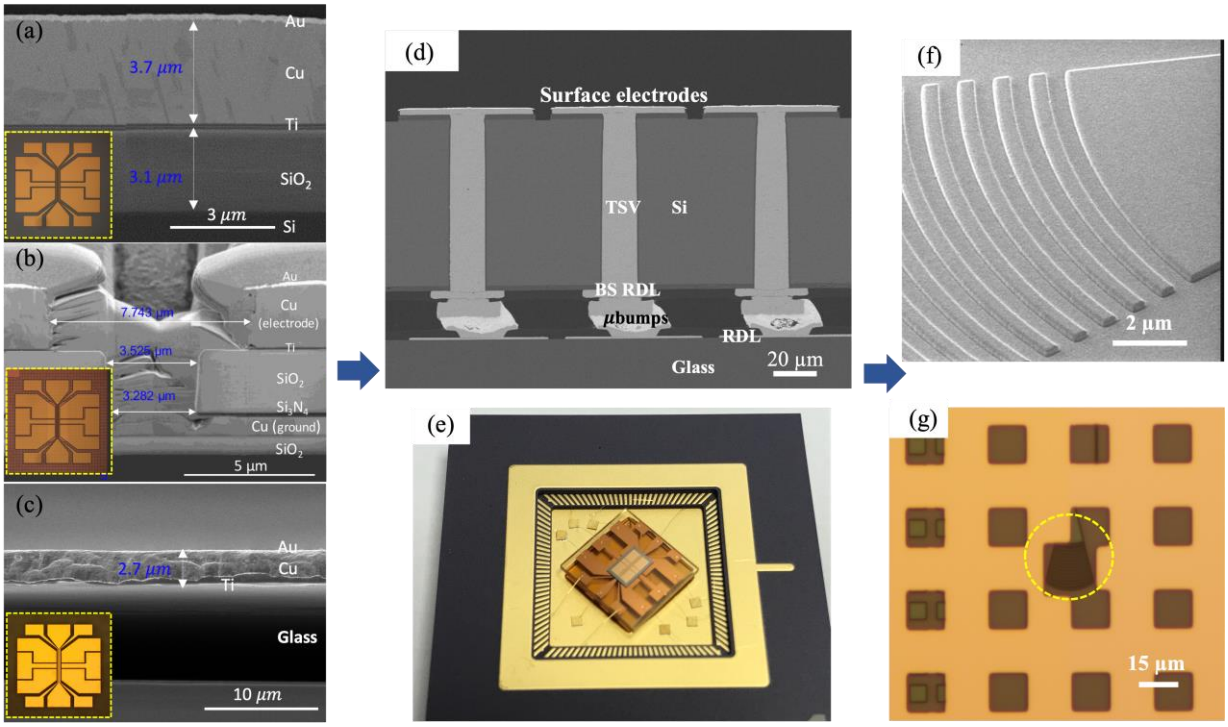

Fig. 2. (a-c) Cross-sectional SEM images of trap on HR silicon, trap on silicon with grounding plane and trap on glass. The insets are top-view optical images of corresponding traps. (d) Cross-sectional SEM image of TSV integrated ion trap chip on a glass interposer. (e) Assembled TSV trap in a CPGA. (f) Grating coupler designed for light of 1092 nm wavelength, which is located underneath grounding plane and surface electrode. (g) Grounding plane with specific windows on top of output grating coupler allowing light transmission. Panels used with respective permission from [25] for (a-c), [6] for (d), [27] for (e).

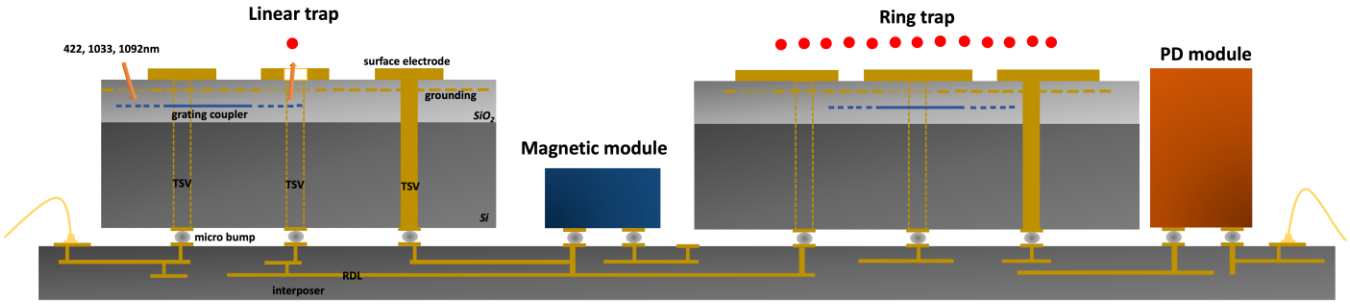

Fig. 3. Large-scale ion trap based quantum computing platform where multi-module integrated ion traps and other functional modules are co-located onto the same interposer in a reconfigurable approach.

output grating coupler is ~10 × 15 μm^2 at the nominated ion trapping height, which is compatible with inter-ion distance. In multilayer metallization module, as a first step, a grounding plane is incorporated into TSV trap to shield the silicon substrate from RF signal, in which specific windows are patterned onto the plane to accommodate TSV and allow the transmission of lights (Fig. 2 (g)) [29]. The power loss of TSV trap is further reduced due to the incorporation of grounding plane, maintaining the temperature increase of new trap <1 K (from finite element modelling). This paves the way for the normal operation of temperature-sensitive silicon photonics. The preliminary electrical testing results on the wafer frontside (before wafer thinning and backside processing) show that the capacitance and insertion loss of new trap are further reduced as compared to the TSV trap.

Based on the multi-module integrated ion trap, a large-scale ion trapping platform is proposed, as illustrated in Fig. 3. Different functional modules are co-located on the interposer and interconnected by the RDL in a reconfigurable approach. Linear trap is used for logic operation, whereas ring trap can be used as quantum 'memory' due to the superior capability to storage large number of ions.

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