

5G HVM Test Challenges – From RF to mmWave application

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Abstract— The rapid adoption of 5G mobile networking technology means that packaged ICs have new features and capabilities that present significant test challenges. IC package test requires quick adaptations to address these new test challenges. In this paper we discuss some of the key areas that need innovation to address these test challenges as volume of 5G IC's rapidly scale. This increases the demand for the development of low cost and scalable high-volume manufacturing test solutions. We discuss the challenges in OTA test, tooling and interconnects, and RF test instruments.

Keywords—5G, mmWave, package test, OTA, RF, Test Instruments, DFT, near field, modulation, sockets, interconnects

I. INTRODUCTION

As we shift into the new decade, the world is quickly becoming more connected and 5G proliferation is playing a key role. Many aspects and industries are embracing the value of 5G including automotive, health care, the cloud, and creating opportunities for smart homes and cities [1][2]. 5G enabled IC's are at the center of this evolving infrastructure.

With these opportunities, the new market brings many challenges for the IC test community. The devices all require wide bandwidth, high frequencies, and the need to functionally test Over the Air (OTA). And as the volume of these IC's expands exponentially, the need for reliable high volume manufacturing (HVM) test becomes a huge opportunity. Unfortunately, not many platforms can scale to HVM testability and volume requirements.

Until Design For Test (DFT) on silicon and other such methods have been proven out, OTA remains the most reliable.

II. STATE OF THE ART

Historically, most of the equipment and instrumentation to characterize the EM-field of the IC utilize horn antennas in large anechoic chambers the size of a room or a small building, and require hours/days of characterization time.

A few companies such as MVG [3][4] have developed tools for characterization in the near field, which starts to address the economies of scale needed for OTA, but further reduction in the physical size of the characterization tools are needed to scale for high volume test. Innovations to improve

characterization in the very near field are needed to enable this. [5]

Additionally, the instrumentation needed to process the information, like spectrum analyzers and power meters, are designed for rack setup/characterization and are not suitable for use in ATE (Automated Test Equipment).

A. Interconnects

i. DUT (Device Under Test) Interfaces

HVM test conditions require access to the 5G/RF ports that greatly differs from the end use system/platform. Often the access methods include direct connections to package pads or die bumps directly when in wafer format. These connection interfaces must be robust to last over HVM cycling in the factory environment. Direct observability of the electrical signals at these interfaces differ from the specification requirements that are meant for end-use applications. Therefore, great lengths of correlation activities are required to map the metrics observed at HVM test to final specifications to determine pass/fail criteria. In package test form factors, the OTA options become possible since the die and package antenna are integrated together. Conversely, at wafer test the opportunity to utilize OTA methods is much more restrictive based on the die geometries, testing cell infrastructure, and ability to inject high quality 5G signals through the interconnects and into the die. For this reason, testing methods typically do not directly translate between the two HVM steps for wafer and package testing, thereby requiring the need to develop multiple test programs and correlation activities.

ii. Socket Technologies for OTA applications

Socket (or test contactor) development for 5G applications adds complexity as compared to standard digital IC packages and RF packages that do not include antennas. It should be noted that since most of the 5G based products are direct soldered BGA packages to the end use system platforms, there is no significant effort at the major socket companies to create temporary socket solutions for 5G products. Some challenges that have been identified are:

- (i) the ability to provide substrate forces to the socket pins in a manner that does not impact antenna access,
- (ii) the mechanical stability of the socket when windows (or cutouts) are added for thermal cooling access (or additional antenna locations), and finally
- (iii) the electrical performance of the high-speed IOs and radiated RF/5G signals when in a socketed application.

The figures below show some examples of the solution space Intel has investigated for OTA applications.

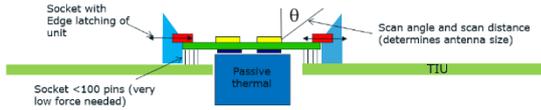


Figure 1: Example of IC package with top surface array antenna in test socket (contactor). Thermal solution access shown for controlling T_j rise.

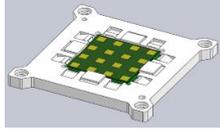


Figure 2: Top view of array antenna in an HVM test socket (contactor)

iii. Probe Heads - Die & Wafer Level Test

Wafer testing hardware includes additional interconnect layers that make it possible to interact with the die geometries in the sub 100um regime. The electrical performance through the additional interconnect layers and probing technology that touch the die pads directly require much care in design, material selection, and component selection. The ability to provide 40+ GHz to multiple locations of a dense die pad array results in specific design rules, testing methods, and co-optimization with die layout. Critical RF/5G bumps on the die must not be damaged during this process of probing as this could impact the die to substrate assembly yield.

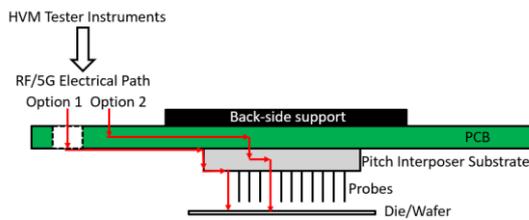


Figure 3: Wafer Test Application - RF/5G Interconnect Paths to DUT

iv. HVM Load board Complexity

Tester instruments provide a limited number of RF/5G resources that get mapped to the HVM test hardware interface. The DUT typically requires many more resources than the tester can provide. To address the need for more tester resources to service the DUT (or multiple DUTs), additional circuitry is required. Resource (or port) multipliers are made up of high frequency switches that can take a single RF/5G input and output N-ports directly to the DUT. Other components such as power splitters, filters, and amplifiers are useful to condition or multiplex the resources further. It is often difficult to find high density RF components for solder attach to the PCB. Minimizing the footprint of the multiplexing circuitry allows for closer proximity to the DUT as well as increasing the number of outputs that can be provided.

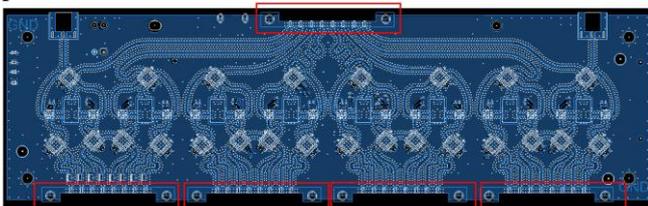


Figure 4: 5G/RF Resource/Port Multiplication: 8-to-32 resource switching

Another platform challenge is the ability to deliver 40+ GHz signal performance over long distances before reaching the DUT. PCB routing on the HVM load board must balance the losses, cross channel coupling, and break-in to the substrate or wafer. As the frequency continues to increase, PCB materials and design rules struggle to meet loss profile demands. Test instrumentation can increase the power to drive to the DUT, but it is not always the case for the DUT to drive harder to the test instrument RX. One manner of solving this issue is to incorporate coaxial cables onto the load board and deliver the signal as close to the DUT as possible. These coaxial cables provide a low loss and low coupling environment, but typically do not have the density to get the user all the way to the DUT. Much effort goes into working with custom RF cable/connector suppliers to develop high-density options for the coax to PCB transitions. Moving forward the RF/5G system architects must work with the connector companies to define suitable high-density and high-frequency solutions that can meet the HVM testing application needs.

Delivering wide bandwidth 5G signal resources to the DUT requires much care in filter selection. High quality factor filters are required to allow for frequency planning of the delivered resource. Multiple filter banks are required to meet the overall desired frequency span and bandwidth. Overlap in bands is required to make smooth transitions between banks. Additional filtering is also required to remove undesirable harmonics or external noise factors. Below (figure 5) is an example of a filter bank that provides continuous signal between 3-17 GHz.

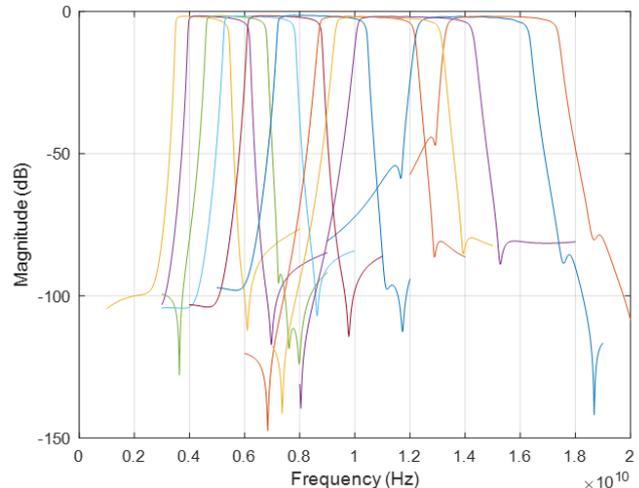


Figure 5: Passband and stopband response of multiple filters needed to meet wide bandwidth 5G applications.

B. Test Instruments

Traditional RF testing has relied on analog modulation (Figure 6) to generate an IQ pair at baseband (the signal is represented by an in-phase component $I(t)$ and a 90-degree lagging component $Q(t)$) that is mixed with a local oscillator signal (LO) and transmitted to the DUT for transmit (Tx) with the opposite done for RF signals received from the DUT (Rx). While this scheme has worked well for RF testing up until now, 5G IC testing exposes the limitation of the scheme due to its high BW, high frequencies, and sharply defined frequency bands [6]. Imperfections in the traditional RF testers like IQ gain, gain/phase imbalance, and LO leakage offset all severely impact the quality of the test. Inherently

this traditional analog modulation scheme is limited to about 1 GHz of real-time bandwidth. To be able to go beyond this BW limit while maintaining the same (or better) quality of test and the flexibility to adapt to many 5G use cases (including future cases), the package test community has to move to all digital RF signal generation and analysis (figure 7), where the IQ signal modulation and demodulation is implemented using digital signal processing techniques within a compute resource, like an FPGA or ASIC[7]. Digital IQ generation and analysis shifts the challenges into the digital space where typical computing trends and the heterogenous integration of FPGAs and ADCs/DACs onto a single package/substrate open the possibility of designing systems that have very high sample rates, are more tolerant of analog impairments, and are smaller and consume less power when compared with an analog implementation [8].

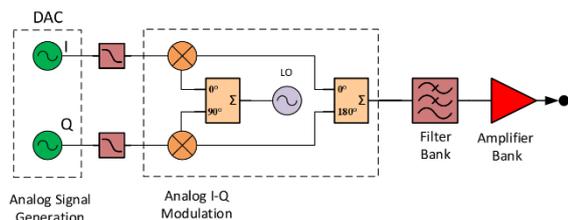


Figure 6: Analog IQ Signal generation with Baseband IQ mixed with LO before transmitting to DUT

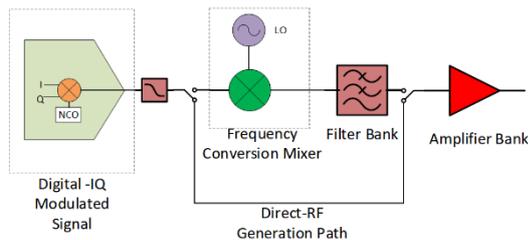


Figure 7: Digital IQ Signal generation with digital IQ can be transmitted to DUT or converted to other freq before transmitting

Despite its rapid adoption, the 3GPP 5G spec is still evolving with new capabilities being added regularly (rel-17 is release and rel-18 is already in the works), which drives the need to have system components that offer flexibility and adaptability. Many system components needed for 5G test instrument design, like filters, switches, and attenuators are provided in bulky form factors and are not packaged for 5G specific applications.

System component vendors should provide integrated solutions (not just components) that are targeted to match the frequency and bandwidth requirements of the 5G standards, yet have some flexibility to scale to future needs. An example will be a digitally selectable 5G specific filter bank(s) or packaging the LO with the frequency conversion on a single substrate to simplify the test instrument design and assembly.

III. CONCLUSIONS AND CALL TO ACTION

Exciting times are ahead in the world of 5G and there are many design and HVM test challenges that need optimization. Additionally the number of devices over the next 5-10 years will scale dramatically in volume. To enable volume test of these IC devices, there are several areas for the industry to focus.

First, test teams should be partnering with design teams to build DFT into the device and reduce reliance on high speed and RF instrumentation. Co-design of the Silicon and package can help optimize the IC to screen out defects

To get RF signaling to and from the tooling, the industry really lacks reliable high density RF interconnects. Most of the industry relies on large coax connectors and cables, which are quite bulky and cannot be easily serviced in a high volume setting. Therefore creating high density interconnects including blind-mate RF connectors will certainly help enable the test tooling to meet the future challenges. These connectors could also be expanded to the socket space where industry lacks high frequency connectors built for several hundred thousand actuation cycles.

In the materials space, specifically laminates, there is a need for PCB materials for mm-wave signals with low power loss which makes it critical for companies to not only model but characterize materials at 5G and mm-wave frequencies.

As we look at the components required for testing 5G ICs, many are discrete components which take up vital board space and create significant integration challenges for the test instruments. Integrating components like filters, amps, and muxes/switches into a single device certainly would help improve the density and potential losses from all the parts. Using digital techniques to simplify signal generation and analysis will also reduce the component count and complexity of test instruments.

Lastly, RF cal can be notoriously difficult and time consuming, so building in self-calibration into the instrumentation itself would help reduce reliance on the entire path.

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