Naming of New Technologies

The naming of new technologies can be difficult and often inaccurate. Over time, standards are developed and language becomes aligned.

The cost of leading-edge nodes, combined with the lack of scaling of significant design blocks (ex: analog) and die sizes reaching reticle size, is driving disaggregation (splitting up) of chip functions into their best price/performance nodes requiring new technologies to interconnect these functions.

We are voicing our support in naming these small IP blocks “chiplets”. It is not a perfect name but fits into our vernacular well and is gaining acceptance in our industry. Our definition of “chiplet”, and what it is not, follows.

We appreciate your inputs.

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Chiplet is not a package type, it is part of a packaging architecture. It is an integrated circuit block that has been specifically designed to communicate with other, similar chiplets, to form larger more complex ICs. Thus, in large and complex chip designs the design is subdivided into functional circuit blocks, often reusable IP blocks, called "chiplets", that are manufactured and recombined on high density interconnect.

Historically the need for multiple chips to deliver a specific function was driven by the reticle limit which dictated the maximum size of a chip possible to be fabricated. Designs that exceeded the reticle limit were split up into smaller dies to be manufacturable. As technology continued to enable increased integration, multiple dies were merged into single, more complex ICs. Thus, the origin of the term “system” on a chip or SoC.

More recently, economics has caused a reversal of that trend. As the industry moves to smaller process nodes, costs for yielding large dies increases. The desire to move to a chiplet-based design has been driven by the increasing cost of manufacturing devices on leading-edge process nodes. Compared to a 250 mm^2 die fabricated on a 45nm process, a 16nm process more than doubles the cost/mm^2 and a 7nm process further doubles that to 4x the cost per yielded mm^2. Moving to the 5 nm and even 3 nm nodes, is expected to make this even worse.

The chiplet solution can be used to ease the economics of manufacturing such chips, with large numbers of transistors, at state-of-the-art nodes. In chiplet-based design the chip is broken down, by function, into multiple smaller chiplets and only the chiplets that require the latest node are made in that node.

Some envision, that in time, the greater use of chiplets will drive the package to become the new SoC, and chiplets become the new "IP". However, for this to be viable across packaging companies, there must be standard/common communication interfaces between chiplets. There are several solutions today, but standards must be chosen.

Finally, the term chiplet SHOULD NOT be used to describe:

a) tiny chips,
b) a packaged die,
c) a package type,
d) or chips combined in a multichip module (MCM) or system in package (SiP) unless they meet the criteria given above.