Co-design and Co-analysis of 3D Integrated Electronics

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Abstract

In this paper, we present an overview of the electrical-thermal co-design and co-analysis of 3D ICs in heterogeneously integrated systems. We present the generalized framework for electrical-thermal co-design. The application of electrical-thermal co-design and co-analysis as applied to chiplets is addressed.

I. Introduction

As the semiconductor industry transitions to higher technology nodes, scaling and increasing demands for high speed have led to dramatic changes in the levels of integration of present-day integrated circuits (ICs). Historically, packaging technologies evolved around two-dimensional circuits. The need for heterogeneous integration has generated interest in 3D stacking and packaging strategies. These are facilitated by the inception of more advanced interconnection schemes such as through-silicon vias (TSV), micro-balls or direct bonding and interposers. Flip chip BGAs operating in the gigahertz range with high densities of I/Os help achieve higher levels of integration while reducing the dependence on Moore's law.

3D die stacking using TSVs, thinned silicon and fine-pitch silicon-silicon interconnections (SSIs) make use of a wide variety of technology structures, materials and processes. Interconnection schemes have also experienced dramatic changes with the demand for higher speeds. They have evolved from passive channels made of impedance-controlled traces on top or embedded in a dielectric to complex structures that involve analog and mixed-signal components performing equalization and clock/data recovery. To achieve required performance, planning in all three domains of integration is of paramount importance, hence the need for co-design.

The aim of co-design is to achieve design closure with a minimum number of iterations while meeting all requirements for performance and cost. The environment for performing the task must leverage from currently available technologies, namely computing power, algorithms, artificial intelligence and machine learning.

Traditional co-design practices address the *discontinuity* that exists between IC design and packaging with an objective that aims to streamline the process of assembling and optimizing the IC, package and printed circuit board (PCB) while applying constraints pertaining to the physical and logical interactions between these design domains. The broader co-design incorporates the heterogeneous nature of the technologies as well as the multi-physics properties of integrated systems.

A fundamental rethinking is needed in devising materials, synthesis, placement technologies and architectures in view of their relations to electrical and thermal performance requiring experts in several disciplines. This step should ideally be developed collectively, in a spirit of *co-design* and *co-analysis*, where each discipline engages the others and exchanges information between the various domains. The art of *co-design* is expected to broaden the range of possibilities for *a priori* knowledge of the path for optimal performance. It will minimize time-to-market, reduce design-related cost while providing better products for a multitude of applications.

Power consumption and signal integrity are currently the main roadblocks for the continued improved performance. In particular, heat dissipation and other thermal effects have moved to the forefront on the list of challenges. This article looks into the application of co-design methods for the electro-thermal analysis of chips.

II. Overview of the generalized framework for electro-thermal co-simulation/co-analysis

The typical electrical-thermal co-analysis flowchart for a Chip-Package-System is depicted in Fig. 1. Generally, the input for our analysis happens to be power-maps on chips. Temperature map from thermal analysis is used for material property adjustment in electrical design analysis. Power analysis results in normalized power map that are the inputs for the next set of thermal analysis. Increased temperature on chips can result in significantly altered properties of the electrical materials as compared to that at room temperature. For example, we see more than 40% increase in electrical resistivity due to temperature increase. This severely affects the electrical design parameters in functional prediction and leakage power dissipation, which is the main source for elevated temperature. Thus, we can clearly see the electrical-thermal correlation from the perspective of overall system performance and reliability [1-2].

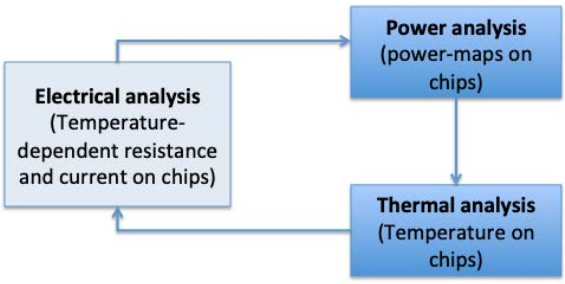

Fig. 1: Typical IC/Package/System co-analysis flow [3]

We now present an executive summary of some of the analytical methods and simulation techniques for electrical-thermal co-design of a range of 3D/2.5D packages and systems.

- Simulation time can exponentially increase in a 3D chip/package architecture due to large-scale geometrical heterogeneity involving complex materials and structures including stacking of chips using TSV, micro-bumps, interposer, package, and PCB. Volumetric meshing based on domain decomposition is an efficient approach that divides large-complex structures into many subdomains, which are smaller and thus efficient in analyzing 3D systems/interposers/packages and PCBs by capturing the IR drop and thermal gradients across the system [4].
- On the other hand, the average power handling capability in coupled interconnects is a critical design metric that requires accurate calculation of frequency- and temperature-dependent variables. In high-power radio-frequency (RF) circuits, thermal effects on interconnect performance are major design constraint. The effect of geometrical and physical parameters, such as metal line thickness, electrical conductivity, and chip/system temperature are quite critical [5].
- Thermal issues are quite important for TSVs and require deeper understanding on their equivalent circuit for efficient electrical-thermal co-analysis framework, as shown in Fig. 2 [6].

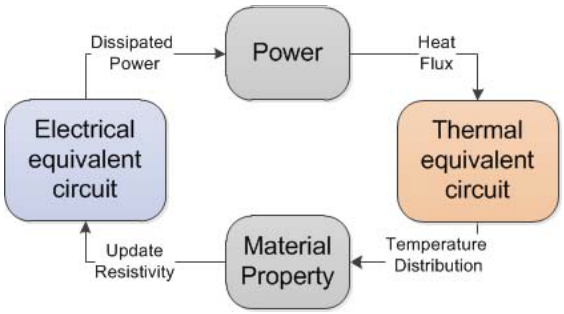

Fig. 2: Generalized electrical-thermal co-analysis framework for TSVs

- For the PCB design ecosystem, the demand for speed is constantly increasing with every technology upgrade. While *PCIe* speeds have doubled every generation from 8 Gbps (@ Gen 3.0) to 16 Gbps (@ Gen 4.0) to 32 Gbps (@ Gen 5.0), the channel loss budgets have not doubled. This has, in-turn, reduced the margin of error in high-speed designs, thereby putting a lot of pressure to consider all possible impairments that would impact high-speed PCBs. Thermal effects are inseparable aspects of interconnects due to Joule heating and/or environmental heating and are directly linked to temperature-dependent material properties in PCBs. Table 1 shows the typical measured values of dielectric constant and loss tangent with respect to temperature [2] for a mid-loss PCB material.

TABLE 1: MATERIAL PROPERTIES WITH RESPECT TO TEMPERATURE [8]

Temperature ^oC	Dielectric constant D_k	Loss tangent D_f	Resistivity $\Omega - m$
20	4.23	0.0124	1.72E-08
60	4.26	0.0146	2.00E-08
100	4.3	0.0173	2.27E-08

Novel technologies including glass/polymer/flex packages are seen to suffer from thermal effects largely due to the lower thermal conductivity of the substrates. An array of metal-based package vias are normally inserted that act as thermal structures or heat sinks. However, this technique can severely degrade the electrical performance due to proximity effects and coupling [7].

III. Co-design of chiplets

Chiplets are a key part of today's heterogeneous integration and reflected in the heterogeneous integration roadmap [8]. Chiplets in principle can provide the ability to integrate an independent but diverse set of functional units with an independent and diverse set of design teams and suppliers. In practice, the grand concept of chiplets becomes a serious challenge for implementing the efficient co-design and co-analysis methodology described in Sec. I and Sec. II as well as [9]. Once the heterogeneously integrated (HI) component is built, a test strategy is needed to support a robust product and the need for a standard to facilitate test capability is needed as presented in [10].

The chiplets may be assembled in many ways and there are many options to consider to conceive, design, and fabricate to produce the design [11]. In Sec. 1, we stated that the aim of co-design is to meet the performance and cost with a minimum set of iterations. A HI design depending on pulling together chiplets from multiple suppliers can easily end up with many iterations as designs become available or improved. Minimizing iterations is a challenge as well as defining the metrics for performance and cost as the design progresses. Until the standards are developed which includes test standards as in [10] and interface standards mentioned in [8] and [11] that means the supply chain needs to have IP providers, technology suppliers, foundries, and assembly houses that interoperate for the HI project in co-design.

Building on the analytical and simulation examples of Sec. II, we need to continue to develop the framework to get the desired *a priori* knowledge of the path for optimal design. For example, a key input is the power

maps that drive the electro-thermal analysis. However, standardized power maps are still a target being pursued between tool vendors or even tools from a single vendor, and standardizing power map input between chiplets will need some HI provider input on requirements to understand the input assumptions for power maps of digital cores, analog chiplets, and photonics devices, for example, that are needed for building the integrated component. This is an example of the need for fundamental rethinking mentioned earlier in that the IP provider needs to have some standards to position the design attributes, such as power maps, to be meaningful for the breadth of potential users and potential higher-product offerings for which the chiplets would be used.

It is important to note that the standards themselves are being discussed within the technical committees of the Electronic Packaging Society (EPS), however, since the details depend on many different disciplines within IEEE, it's likely the standards will have input from EPS, but not be owned by EPS. Just like heterogeneous integration, it will be necessary for the societies of IEEE to work together to develop and support the standards needed for the electronics industry.

IV. Summary

Current technology nodes provide both opportunity and limitations in capability and integration of electronic component. Heterogeneous integration to provide the ability to produce powerful and diverse systems and an efficient co-design methodology is under development and very much needed. The goal is to provide the tools and methodology to drive to design closure with a minimum number of iteration and maximum interoperability between the components or chiplets that make up the product.

The co-design addresses the chip – package – system integration which creates a challenge to handle the scale difference between silicon and TSVs and PCBs, the amount of data, and the diversity of design elements while leveraging the existing electrical and thermal tools to create a co-analysis of thermal-electrical interaction. The volumetric meshing, thermal requirements, and bandwidth increases challenge the capabilities available today. Meanwhile, the bandwidth is scaling with each generation which simultaneously drives trace and pin density and interconnect frequency with lowering electrical and thermal noise margins.

Chiplets are the physical instantiation of the heterogeneous integration and are a good way to view the co-design and co-analysis challenges. Although chiplets are individually designed and manufactured, they must be aware of the use conditions to give co-design a chance of meeting its aim of reducing the iterations to finished designs. Standards are a necessary path to achieve this desire and must embrace the full design cycle from concept to design closure to component testing to final product test and acceptance.

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