Chiplet Technology and Heterogeneous Integration

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Chiplets and heterogeneous integration are changing the design of modern electronic systems. Instead of only relying on process shrinks as the primary driver of product design and system performance, the heterogenous multi-chiplet architectures can potentially provide a much lower cost alternative to the latest design nodes. Packaging technology is poised to play a key role in the performance of the next generation systems. The chiplet-based design can be built on various materials such as silicon, glass, and organic laminate. The resulting single-package-based integration allows multiple silicon dies of various technology and complexity to be integrated efficiently using next-level interconnects, such as silicon interposers and bridges.

As the systems evolve from single monolithic devices to multi-chiplet architectures, the electrical analysis become more critical to guarantee the performance of such heterogenous systems. The second-level interconnects provide a low-impedance power delivery path between multiple independent power domains and short inter-die interconnects. The physical layer can either be parallel or serial interface trading power, latency and area or beachfront. Since these interconnects are short, the signal integrity may not initially pose a challenge. However, elevated transient currents of multiple dies and their unique clocking architecture make the supply noise, jitter, and latency the limiting factors in designing high-performance multi-die heterogenous systems.

In this paper, chiplet packaging technology as well as the design and analysis of the heterogeneous systems are reviewed.

I. Introduction

NEXT generation of electronic systems face multiple challenges to meet the demands for increased performance, lower power, higher bandwidth, smaller form factor, scalability and functionality owing to various applications in the era of Artificial Intelligence (AI), neuromorphic cognition, Internet-of-Things (IoT), wearable device, *5G* and autonomous computing. These challenges are more critical in low-power processors implemented in different technology process nodes supporting a wide range of data rates.

The current complex designs require adapting, as quickly as possible, to the most advanced process nodes, high-levels integration, and larger die sizes. However, due to Moore's law slowdown, the semiconductor industry can no longer scale as it runs through barriers to advance performance improvement. Thus, the normalized cost for incremental technology node advancement has recently been increasing on a faster pace as shown in Figure 1. The small geometries demand numerous complex process steps to manufacture the chips, leading to expensive mask-sets for lithography. For example, the cost-per-yielded die doubles from *16 nm* to *7 nm*.

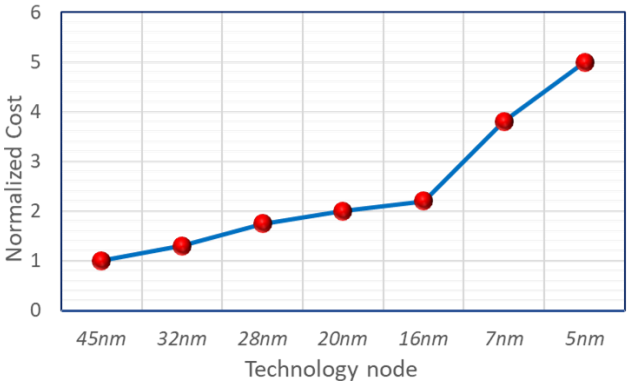

Figure 1: Trends of normalized cost per yielded die for 45nm to 5 nm; [Source: AMD].

Chiplet integration, as a solution to the yield issues in larger chips, facilitates splitting the design and implementing sub-systems into separate smaller dies. Assuming a simple yield model that defects scatter randomly across a wafer, and that a defect anywhere on the die renders it unusable, a large die is much more likely to contain a defect than a small die. For instance, a smaller die improves the yield per wafer for eight background random defects, as shown in Figure 2.

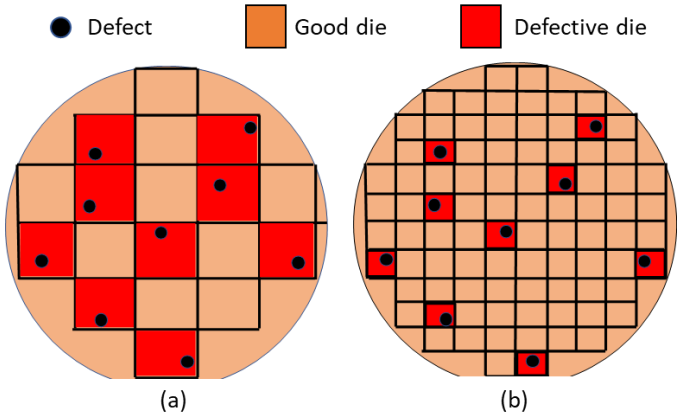

Figure 2: $\boldsymbol{Yield = \frac{Number\ of\ good\ dies}{Total\ number\ of\ dies}}$*; (a) Wafer with larger dies (yield = 50%) (b) wafers with smaller die (yield = 90.2%). Small dies produce higher yields.*

As a result, chiplet integration enables a large ASIC to be partitioned into multiple dies and then interconnected together within a package to build a heterogenous system. Figure 3 shows a conceptual view of a chiplet-based system integration. Even though High-Bandwidth Memory (HBM) is the first type of heterogenous integration that is being widely used, various dies from different process technologies can be integrated using dense parallel package interconnects to enable efficient communications between the chiplets.

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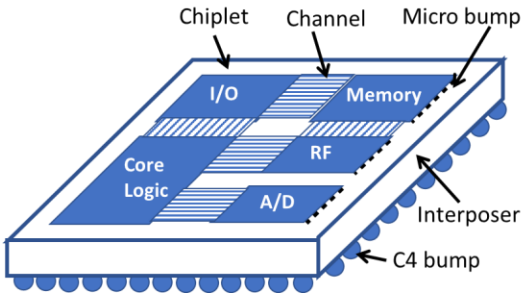

Figure 3: A conceptual heterogenous system using an interposer for chiplet integration.

II. Packaging Technology for Heterogeneous Integration

The physical implementation of die interconnect in chiplet-based heterogenous systems depend on the chip packaging technology. Although there are many packaging options, the three common implementations of heterogonous systems: organic substrate and silicon substrate with and without Through-Silicon Via (TSV), are reviewed [1]. The performance, cost, and maturity of the packaging technology affect the adoption of chaplets.

Organic and silicon interposer as well as Intel's Embedded Multi-die Interconnect Bridge (EMIB) or other similar silicon bridges are among the most popular interconnecting solutions often used to implement chip-to-chip communications [2]. These three approaches have slightly different tradeoffs in terms of the density of the embedded metal routings and power/ground layers, presence, or absence of TSV, and overall cost and performance. The three approaches are compared with respect to their channel loss, cost, coefficient of thermal expansion (CTE) matching, wiring density and infrastructure availability. of multi-chip packaging technology greatly affect the application of chiplets.

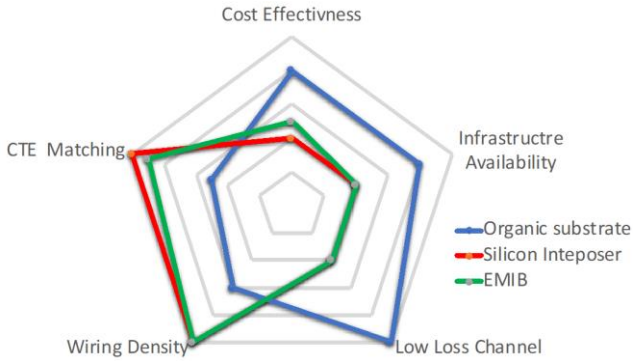

Figure 4: Spider plot comparing the importance of the five factors (channel loss, infrastructure, cost, CTE matching and wire density) for the adaptation of packaging technology for heterogenous integration.

The spider plot, shown in Figure 4, compares the organic interposers for packaging technology for chiplet integration. The silicon interposer and EMIB offer optimal CTE matching and inter-die wiring density, at a significant cost premium. The organic substrate solution provides attractive characteristics at the four corners of the pentagon. However, its wiring density is not competitive when compared to silicon interposer and EMIB.

Recognizing the key role of packaging in heterogonous integration, the IEEE Electronics Packaging Society (EPS) has been working on a heterogeneous integration roadmap to guide and accelerate the projected needs and opportunities for innovation [3].

A conceptual drawing of the cross-section of a heterogeneous system with organic or silicon interposer and EMIB, 2.5D/3D IC with ASIC/FPGA dies and HBM technology is illustrated in Figure 5. Most common implementations of 3D system-in-package are designed and manufactured with a large organic interposer (substrate) with fine-pitch and fine-line interconnections. Silicon interposer and EMIB are also used for high-end and high-performance systems.

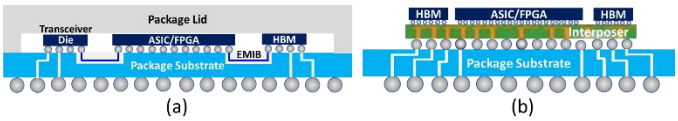

Figure 5: Heterogenous integration using (a) EMIB technology. and (b) organic or silicon interposer.

III. III. Signal and Power Integrity Of Chiplet Interconnect

The scale of interconnect dimensions achievable in a silicon interposer is finer than what is realizable in organic packages and the signal conductor loss in organic substrate is significantly less than that in silicon interconnect. The dimensions of interconnects used in silicon interposer or EMIB is similar to that of silicon metallization, thus the resistive loss and crosstalk between signal routings can be one of the dominant sources of noise and timing error when compared to organic packages. Thus, the interconnect in silicon interposer and silicon bridge need 3D analysis including the vertical paths such as vias, bumps and micro-vias.

A typical silicon interposer often uses one-sided 3 or 4 redistribution layers (RDL) and TSV as shown in Figure 6(a). Metal configuration of the three copper conductor layers with signal layer and power mesh are also shown in Figure 6(b). The diameter of the TSV is 10 μm and the insulation layer thickness is 0.5 μm. A typical implementation of the EMIB cross section is shown in Figure 6 (c). Common physical dimensions and material properties are shown in Table I

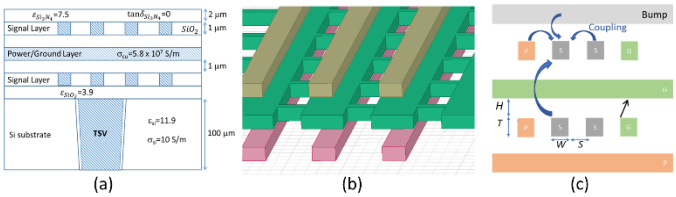

Figure 6: (a) A typical physical dimension and material property of silicon interposer, (b) the power/ground interposer design, and (c) cross-sectional view of signal routing.

A. Channel Analysis

Low latency chiplet interface requires hundreds of signal interconnects that are densely integrated in a small area in either organic or silicon interposer, resulting in several coupling

mechanisms. due to very congested micro-bumps placement, only a limited number of ground signals often provide the reference. This demands for analyzing the coupling effect between power and signal nets as the power-to-signal coupling can be a major source of noise and jitter in both silicon interposer and EMIB.

The insertion loss of the three implementations is shown in Figure 7 (a). The attenuation of the silicon interposer is higher due to the aggressive design rules as shown in Table 1. The DC loss is higher due to the smaller cross section of the silicon interposer traces. In most chiplet interconnect implementations, the two signals are surrounded by power and ground traces as shown in Figure 6 (c). As shown in Figure 7 (b), the crosstalk for the silicon interposer is minimized due to shielding, even though hatched ground and power planes are used, as shown in Figure 6(b).

Table 1: Cross-section and material properties of the three channels.

Interposer Type	*H (μm)*	*T (μm)*	*W (μm)*	*S (μm)*	ε_r	*tan (δ)*
Organic	10	10	7	7	4.6	0.02
EMIB	2	1	2	2	3.9	0.001
Silicon	1	1	1	1	3.9	0.001

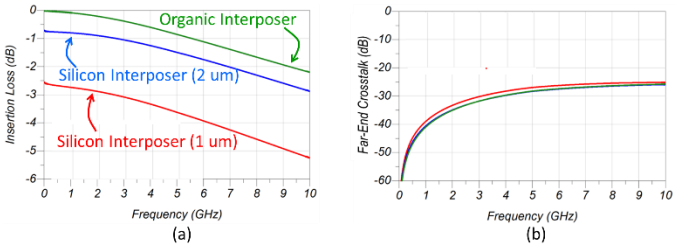

Figure 7: Channel characteristics of the organic, silicon interposer and EMIB: (a) insertion loss and (b) far-end crosstalk.

Since chiplet integration is a technique to enable sub-systems performing as in a monolithic chip, low power and low latency links using dense interconnects are essential. Depending on the packaging type, the density of the interconnects, the bandwidth, power and the latency requirements, there are a few interfaces currently used, as shown in Table 2. Almost all of these interfaces are parallel because the power requirement and latency of serial interfaces are generally higher due to the SerDes's inherent serialization and deserialization. However, the SerDes options should not be disregarded prior to analyzing the trade-offs for the application of interest.

Table 2: Common chip-to-chip interfaces.

Chiplet Interface	Intel AIB	Intel MDIO	BoW	TSMC LIPINCON	SerDes
Bandwidth per pin [Gb/s]	2	5.4	5-16	8	~112
Shoreline BW density[Gbps/mm]	504	1600	1280	536	
I/O Voltage swing [V]	0.7-0.9	0.5	0.7-0.9	0.3	1.2
PHY power efficiency [pJ/b]	0.85	0.5	0.7	0.56	1.6
Latency [ns]	3	3	< 3	14	>37

B. Power Distribution Network

Power distribution network *(PDN)* of heterogenous integrated systems can be significantly different from the traditional electronic systems as they include the interposer or *EMIB* power and ground routings that connect to the *PDN* of the rest of the system including PCB, package, and micro-bump routing, as shown in Figure 8. As a result of PDN connection to the interposer or silicon bridge, the *PDN* impedance of the dies with smaller on-chip decoupling capacitor can significantly be improved through charge sharing with the dies having large decoupling capacitor**.** Specially for TSV-less silicon connection such as EMIB, power connection among multiple dies can be made through the top package layer. For example, if there are power network connections between chiplet 1 and chiplet 2 through the interposer and/or package routings, when chiplet 1 has limited on-chip decoupling capacitor and chiplet 2 has a huge amount of decoupling capacitor, since the power supplies are shared, chiplet 1 can take advantage of the available capacitance provided by chiplet 2. This charge sharing often occurs in a multi-die system with HBM devices. Therefore, without the interposer or EMIB connection, PDN resonance peak looking from chiplet 1 may exceed *1.0 Ohm* while chiplet 2 *PDN* resonance peak is limited to only *0.1 Ohm*. The resulting PDN impedance profiles, with mitigated self-generated noise due to the power sharing scheme, are shown in Figure 9. However, proper tradeoffs must be made as the noise coupling may increase among the charge sharing silicon dies leading into elevated coupled power supply noises [4].

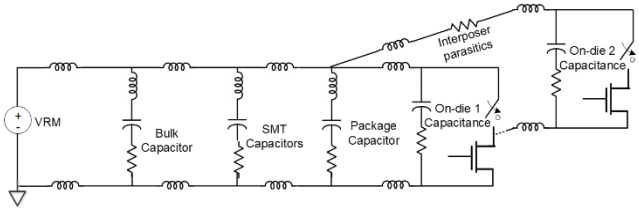

Figure 8: PDN model for a heterogonous integrated system including board, package, interposer, and parasitic and die decaps.

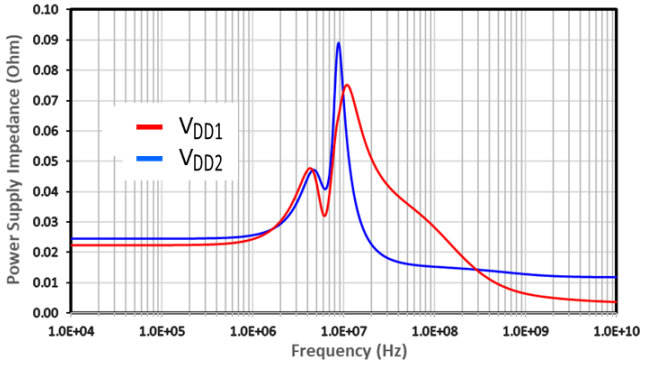

Figure 9: PDN impedance profiles for two chiplet supplies: V_{DD1} and V_{DD2}.

IV. Conclusions

Chiplet-based heterogenous integration has received widespread attention as a solution to break the slowdown of Moore's law. Packaging technology plays a key role in improving the performance of the next generation electronic systems. The three commonly used packaging technologies, organic interposer, silicon interposer, and EMIB are analyzed. Even though the signal integrity analysis of the die-to-die interconnect, for most applications, may not be complex, the jitter and power integrity require careful analysis to mitigate the impact of large current consumption and charge sharing among the many chiplets. Ultimately, developing an industry-wide chiplet ecosystem to accelerate adoption of heterogenous

integration is critical in successful implementation of the system.

V. References

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[2] R. Mahajan, *et al.*, "Embedded Multi-die Interconnect Bridge—A Localized, High-Density Multichip Packaging Interconnect," IEEE CPMT Oct. 2019

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