Flexible Hybrid Electronics with 3DIC

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Flexible Hybrid Electronics

In recent years, wearable devices, implantable devices, and the Internet of Things have become increasingly popular as such devices have become smaller and lighter, and the development of wireless communications has made it easier for device-to-device connections, thus diversifying the applications of electronic devices. Although conventional devices are limited by the shape of their internal printed circuit boards (PCBs), making them impossible to bend, lots of flexible devices based on organic semiconductors and thin film transistors (TFT) [1] using flexible substrates instead of rigid PCBs have been reported. However, there are several issues with conventional flexible devices using organic semiconductors. First, carrier mobility of organic semiconductors is lower than inorganic single-crystal semiconductors such as Si. Since carrier mobility is an important factor in determining the operation speed and power consumption of an IC, it is challenging to construct high-performance devices with organic semiconductors compared to those with inorganic single-crystal semiconductors. The second problem is the difficulty of manufacturing high-density wiring. The wiring width of typical printed electronics is several millimeters to several tens of micrometers, making it challenging to achieve highly integrated and high-performance flexible devices.

In these situations, the flexible hybrid electronics (FHE) has attracted much attention [2]. The FHE combines flexibility of polymeric substrates with single-crystal semiconductor devices' performance to create a new category of flexible electronics [3]. Generally, ultrathin chips are mounted on flexible substrates to enhance the flexibility of the rigid single crystalline semiconductors. Such ultrathin chips can be more flexible and follow curved profiles with a bending radius of 5 mm when 25-µm-thick chips are employed [4]. However, the ultrathin chips are sensitive to applied mechanical stresses, which would induce performance degradation and characteristic deviation by small bending radii.

Advanced Flexible Hybrid Electronics with 3DIC

An advanced concept of FHE is based on cutting-edge semiconductor packaging technology of fan-out wafer-level packaging (FOWLP) in which thin chips, not ultrathin chips, are embedded in a flexible substrate and connecting them with flexible high-density wiring fabricated by wafer-level processing called redistribution layers (RDL)[5]. As the thin chips are not bent, IC chips keep higher performance. Both flexible substrate and flexible wiring interconnecting the adjacent chips give high bendability to the advanced FHE. Another advantage is that advanced FHE suits "chiplet" design architectures well. In the chiplet architecture, instead of using a large application-specific integrated circuits (ASIC) chip, one can use multiple high-yielding, smaller-size chiplets connected by lithographically defined metal interconnects at fine pitches to allow for both higher mechanical flexibility and "on-chip"-like communication. The structural and characteristic comparisons among Si electronics, organic electronics, conventional FHE, and advanced FHE are summarized in Table 1.

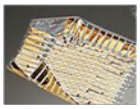
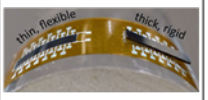
	Si electronics	Organic electronics	Conventional FHE	Advanced FHE
				
Material	Inorganic single crystalline semiconductor	Organic semiconductor	Inorganic & organic semiconductor	Inorganic single crystalline semiconductor
Interconnect	Photolithography	Printing	Printing	Photolithography
Integration	Sheet-level	Sheet-level	Sheet-level	Wafer-level
Performance	High	Low	High	High
Reliability	High	Low	Low	High
Flexibility	Low	Extremely high	Midium	High

Table 1 Comparison of various electronics technologies.

3DICs consist of thin chips stacked using microbumps and underfill or hybrid bonding. Therefore, it isn't easy to make 3DICs flexible while maintaining high performance. Therefore, Advanced FHE is the most suitable to realize flexible systems using 3DICs. Figure 1 shows a schematic illustration of 2D/3D IC chips embedded in a flexible substrate and connected by flexible high-density wiring. This advanced FHE technology with embedded 3DIC can push performance scaling beyond Moore's law limitations.

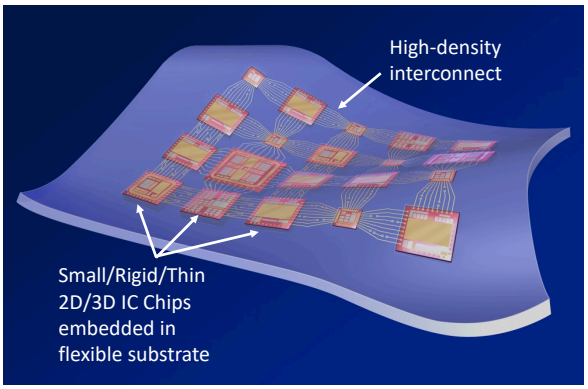


Fig. 1. Schematic illustration of advanced FHE with embedded 3DIC.

A fabrication process flow for advanced FHE is shown in Figure 2. First, Si or III-V (including passives, MEMS, and other) chips ranging in thickness from 50 to 400 µm and in size from hundreds of micrometers to several millimeters in a side, typically one mm^2, are placed in a face-down configuration onto the 1st Si carrier wafer on which a thermally removable adhesive layer is laminated. A Teflon ring makes a retaining dam to keep the liquid raw material or precursor of a polymeric flexible substrate inside the ring. This ring's height determines the total thickness of the advanced FHE. A biomedical-grade polydimethylsiloxane (PDMS) is typically employed as a flexible substrate. In the subsequent step, the raw material of PDMS is poured on the chips, then cured with the 2nd Si carrier wafers having another thermally removable adhesive layer that is stable at a higher temperature than the 1st adhesive. After compression molding with the two Si carrier wafers, the

thin/rigid/small chips are embedded in the PDMS. The following step is debonding the 1st Si carrier wafer at around 120°C to give the chips a planarized surface with various thicknesses on the 2nd Si carrier wafer without any mechanical thinning processes. Before the subsequent metallization processes, one or two dielectric layers as a stress buffer layer (SBL) are coated on the surface of the PDMS/chips, followed by contact etching and metallization using standard photolithography processes at the wafer level. Au or Cu wires are formed to interconnect the chips embedded in the PDMS. Finally, the 2nd Si carrier wafer is de-bonded at around 150°C to give advanced FHE. Figure 3 shows the advanced FHE with embedded 625 chips (25 by 25) on the human arm with a curvature radius of around 40 mm. The chip size and thickness are 1 mm^2 and 100 µm, respectively.

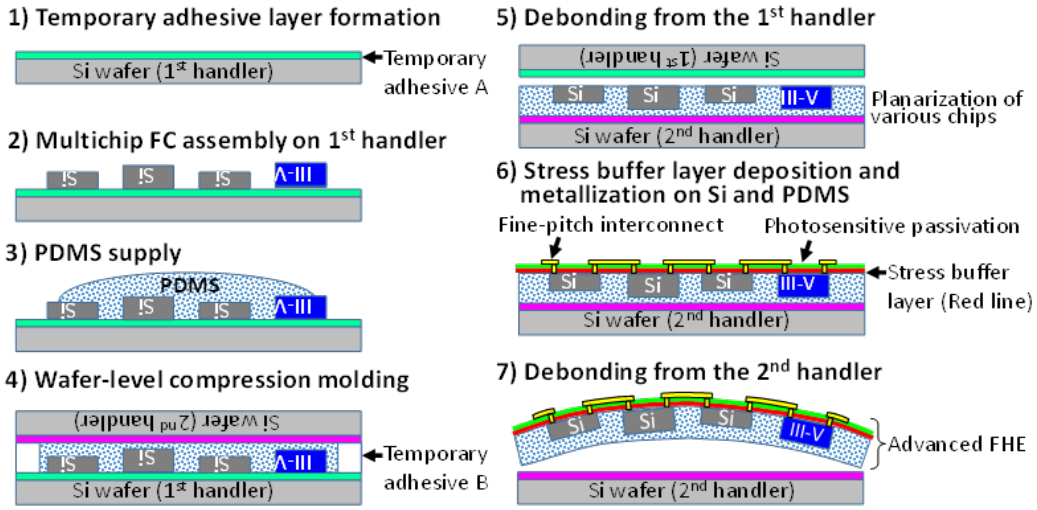


Fig. 2. Example of fabrication process flow for advanced FHE [6].

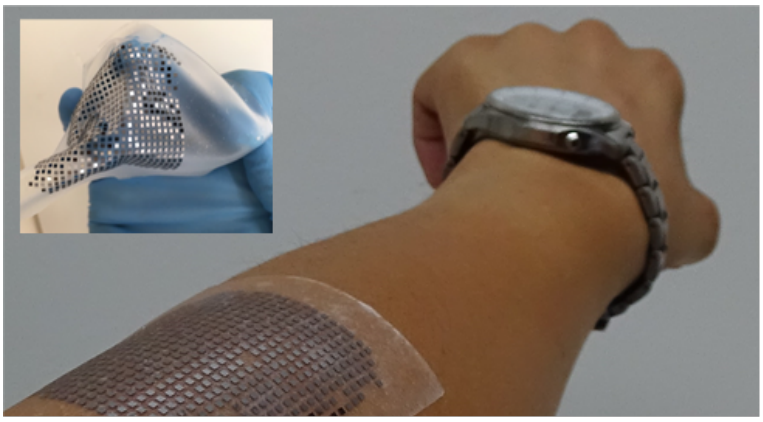


Fig. 3. Photographs of advanced FHE with 625 chips embedded in the flexible substrate.

Heterogeneous integration by 3D film stacking

Interposer technologies are widely applied i.e. in heterogeneous integration and chiplet architectures [7]. Typically, silicon or glass wafers are used as substrate materials and enable vertical electrical interconnections and lateral redistribution of the wiring. Beside these wafer type substrates also rigid organic interposers, e. g. high density printed circuit boards (PCB) are well known in heterogeneous

system integration. Further technological opportunities arise when flexible organic interposers are introduced.

High quality polymers like for instance Polyimide offer valuable advantages for chip embedding and 3D-stacking technologies: good electrical insulation, high thermal stability, high surface quality, low dielectric constant, CTE match to copper and easy manufacturability of vias for 3D interconnects, e. g. prepared by laser drilling. These material properties enable high performance and high density wiring systems as well as thermally supported chip bonding technologies. As an additional benefit the mechanical bendability of thin films or thin polymer layer stacks can help to overcome a main challenge in 3DIC systems i.e., bridging and levelling of height differences between different ICs or components within one functional system.

This section will briefly review some pioneering development work conducted by several research groups worldwide in the field of chip embedding in flexible organic materials.

At first it should be noted that there are a variety of integration concepts that are based on coating and chip placement techniques using Silicon wafers as temporary carrier substrates [8-12]. The targeted flexibility of the chip-packages appears only after delamination of the multi-layer setup from the carrier. As the manufacturing process is based on standard semiconductor processing technologies the boundary conditions of system size and cost per wafer area need to be respected.

An alternative approach to flexible organic interposers uses free-standing polymer films of a thickness of 25µm to 50 µm as base substrate for routing, die placement and embedding. In this case the processed substrate area is independent of the round wafer format. Films can either be placed on PCB boards as temporary carrier or roll-to-roll (R2R) processing technologies using Polyimide film rolls can be introduced. An interesting aspect in this context is the fact that high precision direct write lithography tools have become very fast and cost-effective over the past years. These new tools allow for the implementation of digital corrections during the patterning process and thereby can solve the problems arising from non-uniform shrinkage or expansion of polymer film substrates.

Fraunhofer EMFT has proposed an integration concept for manufacture of Thin-Chip-Foil-Packages that is compatible with roll-to-roll processing [13]. It is based on face-up placement of a thin die in a cavity of a PI film substrate, seamless embedding of the die in a polymer layer, via formation and patterning of copper interconnects by lithography and electro-plating processes, see Figure 4. A first demonstrator has been prepared proving the functionality of a 25 µm thin industrial micro-controller IC in a film package of less than 100 µm thickness. Initially these results were achieved by temporarily mounting the PI film onto a Si wafer carrier and standard wafer processing tools [14]. Now, this concept is intended to be adapted to roll-to-roll processing using doctor blade coating of a liquid polymer for embedding of IC devices. Vias for electrical interconnection then could be prepared by laser drilling and copper patterns by direct write R2R lithography. Further development work in this field would open the door to cost-effective manufacture of Chip-Foil-Packages by R2R.

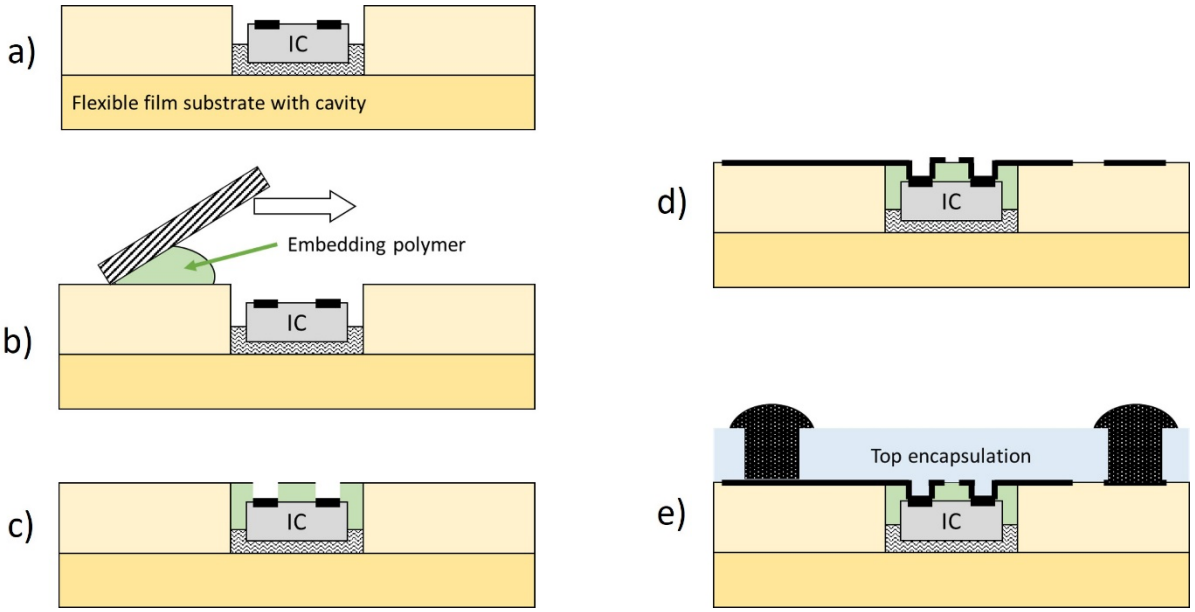


Fig. 4: Roll-to-roll compatible process flow for manufacture of “Chip-Foil-Packages“ by face-up embedding and direct interconnection by thin film wiring.

Outlook on 3D-Film Stacking

A technology of flexible hybrid 3DIC integration is envisaged by stacking of chip-film-laminates upon each other and thus creating a 3D-multi-layer-chip-assembly. In order to keep the final stack in a more or less plan-parallel configuration it is recommended either to ensure highly uniform thickness in each chip layer or to allow for some height compensation by embedded cavities. The latter concept is shown in Figure 5 [15].

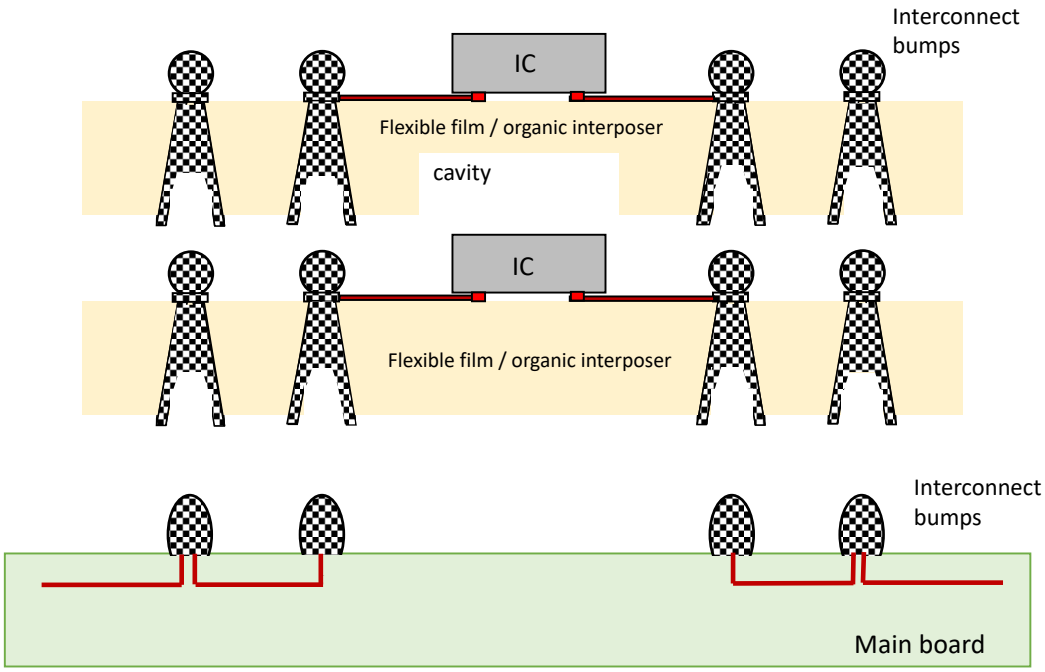


Figure 5: Concept for 3D stacking of chip-film-laminates (flexible hybrid 3DIC integration)

As a first estimation of the achievable 3D interconnect density the laser drilled vias might contribute by a diameter of 30 µm, thereby resulting in a via pitch of some 120 µm. A 10x10 via array thus could be arranged on an area of 1.2 mm x 1.2mm. This is obviously not in the range targeted for high performance computing systems like for instance 3D stacking of HBM (high bandwidth memory) devices. Nevertheless, as flexible film interposers can be produced at comparatively low cost (CMOS wafer technology is not required) such technological approach will offer advanced applications for Flexible Hybrid Electronics (FHE) such as standard memory devices stacked on micro-controller ICs. Applications can be envisaged for IoT (Internet of Things) sensor nodes that need to store and process data before transmitting the processed information (e.g. using AI algorithms for data extraction) to a host system. It is concluded that emerging technologies in processing of flexible film substrates also offer new perspectives for the realization of 3DIC.

Conclusion

In order to pay more attention to the described stacking concepts based on flexible organic substrates, the IEEE EPS Technical Committee 3D/TSV decided to broaden its objectives from Si-based 3DIC technologies to flexible hybrid 3DIC integration.

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