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Seminar

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Virtual Online

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"Heterogeneous Integration of Surface Ion Trap, Silicon Photonics and 3D-TSV for Quantum Computing"

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Abstract

The past decade has been exciting years for quantum computing. In 2016, IBM introduced the first superconductor-based quantum computer (IBM Q) entangling all 16 qubits with great versatility in nuclear magnetic resonance and cavity quantum electrodynamic applications. Meanwhile, Google reported quantum supremacy in the use of the Sycamore processor with 53 programmable superconducting qubits, taking 200 seconds to perform computing tasks which would take approximately 10,000 years in classical computers. To further improve the qubit performances (e.g. fidelity, coherent time) and scalability, ion qubits have been widely reported in quantum computing applications. MIT and ETH Zurich have reported the integration of on-chip photonics components into surface electrode (SE) ion traps. For the industrialization of ion trap quantum computing devices, Honeywell reported quantum charge coupled devices (QCCD) which trap, transport and address multiple ions simultaneously. However, these quantum computing devices require niche fabrication techniques which limits the universality of quantum computing technology. In this study, we developed a scalable multi-module platform integrating SE ion traps, silicon photonics components, and 3D through silicon via (TSV) interconnects using conventional CMOS technologies on a 12-inch substrate. The photonics components simplify the optical addressing setups in ion traps, providing significant miniaturization to quantum devices. Meanwhile, the TSV interconnects replace the conventional wire bonding connections with much lower parasitics, with improved ion trapping performances and scalability. In this talk, we discuss our work on surface ion traps (Sr^+) with respect to their RF and ion-trapping performance. The choices of glass

substrate, insertion of ground plane and 3D-TSV are included. In addition, design and performance of silicon photonic components, both active and passive, are also discussed. This talk ends with a vision of future quantum computing systems that are both CMOS compatible and scalable.

Biography

Chuan Seng Tan is a Professor of Electronic Engineering at the School of Electrical and Electronic Engineering at Nanyang Technological University, Singapore. He received his PhD from MIT in 2006. Currently, he is working on process technology of three-dimensional integrated circuits (3-D ICs), as well as engineered substrate (Si/Ge/Sn) for group-IV photonics. He has numerous publications (journal and conference) and IPs on 3-D technology and engineered substrates. Nine of his inventions have since been licensed to a spin-off company. He co-edited/co-authored five books on 3D packaging technology.

He is a senior member of IEEE and a recipient of the Exceptional Technical Achievement Award from the IEEE Electronics Packaging Society (EPS) in 2019. Beginning June 2019, he is a Distinguished Lecturer with IEEE-EPS. He is a Fellow of the International Microelectronics Assembly and Packaging Society (IMAPS) since 2019 and a recipient of the William D. Ashman - John A. Wagnon Technical Achievement Award in 2020.