Intel Agilex™ Direct Radio Frequency Multi Chip Package with Embedded Multi-Die Interconnect Bridge – The First State-of-The-Art Heterogeneous Integrated Multi-Chip Package

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Abstract - **Heterogeneous integration using Multi chip packaging has become a key technology enabler for meeting the high bandwidth demands of next generation compute architectures. Recent advances in packaging technologies, such as Intel's Embedded Multi-Die Interconnect Bridge (EMIB) packaging technology have enabled building complex compute architectures in a single package using multi-technology chiplet integration. These advances have provided designers with the flexibility to build systems in a single package using optimized and custom chiplets with unique functionalities and process technology of choice coupled with standardized low power, high bandwidth IO links. Intel's Advanced Interface Bus (AIB) is a die-to-die PHY level standard that enables a modular approach to system design with a library of chiplet intellectual property (IP) blocks. Combining Intel's FPGAs with AIB interfaces and EMIB packaging technology provides a unique opportunity to develop a new class of products for defense applications that meets the system requirements in a small form factor with greater flexibility, scalability, ease of use, and faster time to market.**

The U.S. Department of Defense has awarded Intel Federal LLC the second phase of its State-of-the-Art Heterogeneous Integrated Packaging (SHIP) program. The SHIP program enables the U.S. Government (USG) to access Intel's state-of-the-art semiconductor packaging capabilities and provides a path for the USG's industry partners to develop and modernize Department of Defense mission critical systems with state-of-the-art commercial electronic packaging technologies. One of the first prototypes to be developed and enabled through this program is an Agilex™ Direct Radio Frequency (RF) FPGA. The Agilex™ Direct RF FPGA integrates an Agilex™ FPGA with Direct RF Data Converters and SerDes chiplets into a single package with EMIB technology. This paper provides and overview of the SHIP program including the enablement of new RF based testing, quality, and reliability of overall EMIB technology and the first SHIP product. The paper also discusses the microelectronics quantifiable assurance (MQA) being evaluated as part of the SHIP program.

Index Terms — dense MCP, multi-chip package, high bandwidth packaging, heterogeneous integration, SHIP, Agilex™ Direct RF, AIB interface.

I. Introduction

We are living in an era where there is continually increasing performance demand for energy efficient computing and communication driven by applications such as AI, 5G, cloud computing, and autonomous driving. Heterogeneous integration (HI) enabled by the rapid development and proliferation of innovative advanced packaging technologies today provides a perfect solution to meet computing and communication demand and overcome the drawbacks in manufacturing [1-3].

Heterogenous integration is a key technology enabler that helps to integrate different components in a multi-chip package (MCP). This development provided options to assemble complex compute architectures in a single package with unique functionalities and process technology choices. These advances have allowed designers to build systems that the market demands. Heterogenous integration has emerged as a crucial enabler of current and future advances in computing and communications.

The major drivers for adopting this technology are:

1. Performance
   a. SWaP (Size, Weight, and Power). Increased performance while reducing power, critical for advanced Radar and Electronic Warfare (EW).
   b. Artificial Intelligence (AI) and "Big Data" Processing is enabled by High Bandwidth Memory when large amounts of memory can be successfully integrated with the package.

c. Very High Interconnect Density- Required for Direct RF sampling where sampling rates can reach 64 Gsps or higher.

2. Manufacturing cost and reliability
   a. Large die yields are lower when compared to a smaller die.
   b. Only some parts of the system require expensive leading-edge technology while other functions can be realized with less costly processes.
   c. Application Reuse – allows alternate markets and configurations to reuse some of the same silicon.
3. Security and Assurance – IP & Critical Program information (CPI) protection, enhanced resistance to cyber, data ex-fill, side-channel, and crypto attacks. Much greater visibility into the supply chain and assembly process. Including quantifiable data for material tracking, metrology, and process control. This significantly reduces risk.

Among those drivers, high interconnect bandwidth is vital to enable future applications. One primary design aspect for increased bandwidth using parallel IO is scaling interconnect density on the package by thus allowing high-density I/O and electrical interconnect paths between chiplets with minimal interface power/bit.

Intel invented EMIB technology to integrate the above features [4]. Intel has successfully enabled this packaging technology for chiplet applications. A silicon bridge was used to link multiple dies (Analog, memory, CPU, and ASIC chiplets alongside monolithic FPGA fabric) in a single package. Thus, EMIB based dense MCP technology has become a new packaging paradigm for localized high-density interconnects between two or more die on an organic package substrate, opening new opportunities for heterogeneous in-package integration. Intel's FPGA SIP technology is designed to deliver products that effectively mix functionality or process nodes within a single package.

To connect the chiplets or tiles and maintain communication, Intel created the Advanced Interface bus (AIB), a die-to-die PHY-level standard that enables a modular approach to system design with a library of chiplet intellectual property (IP) blocks [5]. This new interconnect scheme was revolutionary and enabled a high-speed, low latency, low power, and flexible method of interconnecting chiplets. The AIB specification is public, and its process and packaging technology are agnostic. Fig. 1 shows the chiplets connected to an FPGA connection using EMIB interconnect and the AIB protocol. Intel's Advanced packaging technologies are in full production and are used for a wide array of applications.

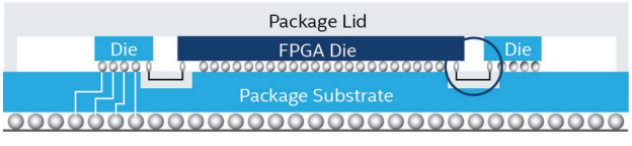

Fig. 1. Chiplet connections using EMIB/AIB

II. State of Art Hetergenous Integrated Package (SHIP)

The U.S. Department of Defense (DoD) awarded Intel Federal LLC through the second phase of its SHIP (State of the Art Heterogeneous Integrated Packaging) Program. Before SHIP [6] came into effect, DoD could not access State-of-the-Art microelectronics beyond commercially available off-the-shelf (COTS) products. SHIP is a crucial program in which both Intel and U.S. Government share a common priority to promote and advance U.S based state of the art semiconductor manufacturing. This has enabled the Department of Defense to access Intel's leading-edge advanced semiconductor packaging technologies & capabilities, including fab and assembly technologies, thereby protecting their intellectual property with a reliable partner like Intel. Intel SHIP MCPs changed the paradigm, and Intel's chiplet and packaging technology have enabled Defense Industrial Base (DIB) partners to design optimal systems for their end applications.

Primary benefits to the DoD:

- Allow post-foundry manufacturing personalization for Intellectual Property (IP) protection, permitting die to be sourced from multiple foundries.
- Allows DoD specialty chiplet integration to support enhanced performance and security.
- Lower cost and risk to integrate advanced technologies as they emerge, such as non-FLASH based non-volatile memory, non-silicon devices, neural networks, photonics etc.
- Shorter transition times, while offering configurability and enabling design re-use of SOTA microelectronics for DoD specific applications optimized to meet performance and/or security requirements. Allows early and privileged access through industry relationships.
- The package selection and its development together with IP design, manufacturing, validation, and software development utilize Intel's US based commercial design, assembly, test and manufacturing processes and methodologies. This provides quantifiable assurance for DoD products.

Fig. 2 shows Intel's first SHIP MCP product, codenamed MCP1 (Direct RF-series FPGA AGRW014). This device has an A-Tile wideband Data converter chiplet that provides four (4) Analog to Digital Converters (ADCs) and four (4) Digital to Analog Converters (DACs) operating up to 64 Gsps and enabling 32 GHz of instantaneous bandwidth. It also includes integrated programmable Digital Up Conversion (DUC) and Digital Down Conversion (DDC) blocks that allow customers to trade off channel count versus channel bandwidth. The Intel Agilex™ 014 FPGA fabricated on Intel 10nm provides 1.4M Logic Elements, 9020 18x19 multipliers, 190 Mb of embedded memory, and a quad-core 64-bit ARM® Cortex® -A53 processor subsystem for workload development. Intel FPGAs Tools enable the development of low latency, high throughput,

flexible, scalable, and secure designs. The F-Tile transceiver chiplet enables up to 16 high speed SerDes channels of 32 Gbps or up to 12 channels at 58 Gbps 4-Level Pulse Amplitude Modulation (PAM4) with dedicated IP blocks that support PCIe Gen4x16 or 10/25/50/100/200/400 Gb Ethernet.

Fig. 2. MCP1 (Codenamed MCP1, Direct RF-series FPGA AGRW014)

Intel worked with leading high-speed converter companies to develop high-performance RF ADC and DAC tiles compatible with EMIB packaging technology and AIB standards. Intel's Agilex™ FPGA Direct RF-series are state-of-the-art products that can perform Direct analog RF signal conversion for multiple analog channels at 64 Gsps over as many as eight channels. With Intel's EMIB and AIB, the Direct RF series provides the lowest possible latency and power consumption when converting between the analog and digital domains at these sample rates. Direct RF architectures deliver increased performance while eliminating many expensive analog components, which lowers the system-level cost. Platforms with long lifespans (as many as 30 to 50 years for some military applications) need solutions that fit within the existing size and power infrastructure constraints during the platform's entire lifespan. By eliminating large, expensive, power-hungry heterodyne stages, Direct RF solutions allow engineers to create systems that were once considered impossible to implement in the SWaP profile required for today's systems. Even a lower power solution is possible with Intel's complete logic continuum, substituting an Intel eASIC structured ASIC, or a custom ASIC for the Intel FPGA die in a packaged design. An example of this is shown in Fig. 3 which shows the replacement of an Agilex™ FPGA in our MCP2 (Direct RF-series FPGA AGRW027) configuration with a customer specific hardened eASIC structured ASIC for lower power applications.

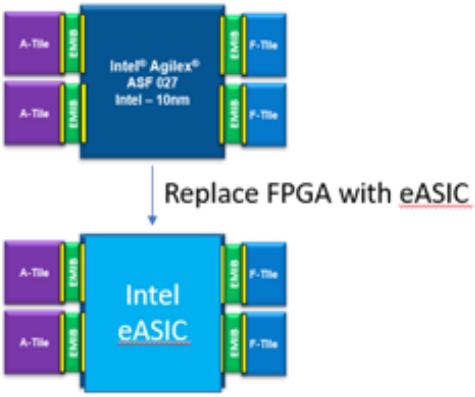

Fig.3. A custom ASIC for the Intel FPGA die in a packaged design

Intel's SHIP MCPs can provide 8x-10x savings in SWaP when compared to alternative solutions using discrete components. These innovative MCPs solve long standing challenges in monolithic integration for RF applications.

Heterogeneous integration is the best solution to handle complex requirements. Intel has developed a wide portfolio of chiplets to address the needs of the defense industrial base suppliers. This capability provides systems designers with a wide range of design options to cover various levels of flexibility and optimize cost, power, and performance. Additionally, MQA being developed by DoD and Intel provides guidance to enhance the IP protection and security of SHIP packages.

A. Details of the EMIB Package

Linear interconnect escape density or IO density (IO/mm/layer) is a key metric used to compare capability envelopes of different packaging technologies used to create the physical on-package link. Note that IO here refers to physical interconnects. IO/mm/layer is the number of wires escaping per millimeter of die edge for each layer of the package. EMIB is unique in that it is the only packaging technology that offers localized high-density wiring while the bulk of the package interconnects are still the same traditional organic package interconnects. The basic concept is that it uses thin pieces of silicon with multi-layer BEOL interconnects, embedded in organic substrates, to enable localized dense interconnects. A very thin silicon bridge is embedded within the top 2 layers of an organic package and connected to flip-chip pads on the package substrate through package vias.

EMIB bridge is connected to flip-chip pads on the package substrate using through-package vias in the top two layers. This ability to provide multiple localized interconnects, without using through-silicon vias (TSVs), is an inherent area and cost advantage of the EMIB technology compared with other dense MCP technologies. EMIB enables the integration of multiple dies, such that the total die area connected on the package is significantly greater than the reticle size and is not as limited by reticle limits. Aside from the high-density bridge regions, the rest of the die-to-package interconnects and the structure of the package substrate are unaffected by the presence of the bridges. Thus, unlike the silicon interposer, the electrical path is not adversely affected. In addition, the EMIB assembly process has one less step than the silicon interposer assembly process.

EMIB process is built upon the standard package construction flow, with the additional steps to create the EMIB cavities. The bridges are positioned in the cavities, held in place with an adhesive. The final dielectric and metal build-up layers are added followed by via drilling and plating. A bridge wafer is manufactured using a FAB back-end process. This wafer is first thinned and after thinning, the wafer is singulated into individual bridge dies which are ready for embedding. In parallel, the organic package follows a traditional build-up process until the final build-up layer. At this point, an extra step is introduced to create cavities for the bridge. The bridge is placed in the cavity, held in place with an adhesive and the final layers of buildup

dielectrics are applied followed by fine via formation in the bridge region and coarse via formation elsewhere. The package is now ready for chip-attach which is done using Thermal Compression Bonding followed by capillary underfill.

A number of enabling technologies were developed to realize the EMIB technology which is well on its way to technology certification and production qualification. Some of these enabling technologies are:

- A fab process for bridge silicon with multi-layer thick BEOL metals
- Bridge wafer thinning (below 75µm) that achieves tight total thickness variation (TTV)
- A unique substrate cavity formation process supporting multiple bridges.
- In the package substrate, a fine pitch bridge via formation process
- A process that allows for precise bump height control for mixed CD bumps
- An Epoxy Underfill process with void-free filling between fine and coarse pitch regions

An example of a fabricated bridge is shown in Fig. 4. This specific design implements the following:

- 55um bump pitch to the die above
- 2um line + 2um space, with 2um metal thickness
- 4um pitch, with 250 wires per mm "beachfront"
- 2um thick dielectric between each EMIB metal layer
- 4 metal layers on the EMIB bridge

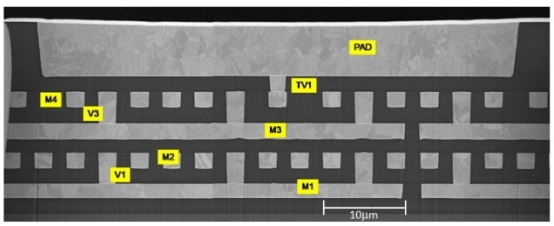

Fig 4. Bridge cross section showing 4 metal layers with 2um lines, spaces and vias. Layers M2 and M4 are used for signaling. M1 and M3 are grounds.

III. EMIB Package Quality and Reliability

EMIB process development has required significant innovations in the substrate dielectric thickness control, plating uniformity, and process metrologies to ensure a high-yielding assembly process at a fine bump pitch. Hence substrate manufacturing complexity has increased and, unlike the silicon interposer, EMIB package must accommodate a greater coefficient of thermal expansion (CTE) mismatch between the die and the package, which is like current organic packaging. Since the bridge itself is small and thin, it does not alter the thermomechanical state of stress of the package in a measurable way, and the package structure had been assessed to meet all reliability conditions that the traditional organic packages meet.

To validate the models and reliability estimations, A test package was created that represents the family of products in terms of package size, die size and layout, and interconnect structure as shown in Fig. 5. The test package has daisy chains routed between the die and the substrate through the first level interconnect and through the EMIB die to enable electrical detection of any thermomechanical related fail modes prior/ during/ after reliability stress. Enveloped test package layout is shared below.

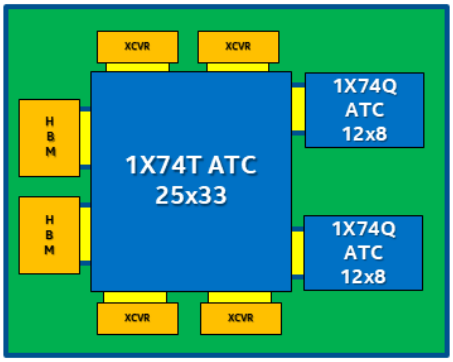

Fig 5. Test package for EMIB package quality and reliability validation

Test package had one compute test chip with 25x33mm die size and two IO test chips with 12x8mm die sizes, two transceivers and two High Bandwidth Memory packages connected with eight EMIB bridges, to envelop various product package designs.

The requirement was to demonstrate zero electrical failures with a minimum statistically driven sample size, subjecting the package to a range of stresses to simulate the life of product. The duration of accelerated stress and sample sizes were defined by industry standards, specifically JEDEC and MIL standards.

To test the reliability of the EMIB package design, JEDEC standard environmental stresses were utilized:

OEM Manufacturing: As the packages are designed for JEDEC Moisture Sensitivity Level 3, per JESD22-A111B standard, Level 3 Pre-conditioning stress is utilized to simulate OEM storage and SMT process

Humidity: Per JEDEC JESD22-A101D standard, Biased Highly Accelerated Stress Test (BHAST) at 110C + 85% RH condition with 3.3V applied voltage is used to assess impact of humid environments.

High Temperature Storage Life: To determine the effects of time and temperature for thermally activated failure mechanisms, per JESD-A103E standard, units are stressed under 150C steady-state temperature.

Fatigue Life: To determine the ability of package to withstand thermos-mechanical fatigue, per JESD22-A104F standard, temperature cycling -B (TCB) condition is utilized.

For statistically significant sample size per noise factors, 80 units per assembly lot and minimum of 3 assembly lots were required for each stress and after data availability, equivalent field DPM estimations were calculated for failure modes with known acceleration factors, even though no failures were observed in environmental reliability stresses.

To be able to determine the reliability of package beyond JEDEC defined standards, certain environmental stresses (such as TCB) are taken beyond the defined targets. Details of stress conditions, durations and sample sizes are listed in the Table 1.

TABLE 1. EXTENDED STRESS CONDITIONS

Test	Condition	Duration	Sample Size
Moisture Sensitivity Level3 (MSL3)	30C / 60% RH	9 days	240 units (3 lots)
Highly Accelerated Stress Test (HAST)	110C / 85%RH / 3.3V	275 hours	240 units (3 lots)
Temperature Cycling "B"	-55C to 125C	1500 cycles	240 units (3 lots)
High Temperature Storage Life	150C	1500 hours	240 units (3 lots)

The results from these stresses were shown in Table 2.

TABLE 2. EXTENDED STRESS CONDITIONS AND RESULTS

Test	Result	Equivalent DPM
Moisture Sensitivity Level3 (MSL3)	No failures	Not applicable
Highly Accelerated Stress Test (HAST)	No failures	0.1%
Temperature Cycling "B"	No failures	0.1%
High Temperature Storage Life	No failures	0.1%

Additionally, the reliability of the integrated package is validated on the MCP1 product through the environmental stresses. The product is powered up statically to the datasheet specs. for Biased Temperature and Humidity (THB) stress to test the robustness in humidity environments with stress conditions as 85°C, 85% RH and biased at V_{nom} for 1000 hours. TC'B, HTSL and unbiased HAST are the other stresses, as defined in the previous tables, the product is tested to. The parts are subjected through the MSL3 pre-conditioning before subjecting to the respective stresses. A minimum of 135 units are selected randomly from 3 lots for this stress. Before stress, after stress and at certain intermediate durations, the parts are subjected to parametric and functional electrical tests that check for any potential degradation. The results listed in the table below confirm that the product has performed well in the reliability stresses with no failures observed. The results from these stresses were shown in Table 3.

TABLE 3. MCP1 STRESS CONDITIONS AND RESULTS

Test	Cond.	Duration	Result
Unbiased HAST	110°C / 85%RH	264 hours	No failures
THB	85°C / 85%RH	1000 hours	No failures
TC"B"	-55°C to 125°C	1000 cycles	No failures
HTSL	150°C	1000 hours	No failures

IV. PACKAGE RF TESTING

In order to enable package RF Testing for the final SHIP EMIB package, an Automated HVM RF Test solution was developed at Intel as shown in Fig. 6. A semicustom tester solution was developed using an automatic test equipment (ATE) base tester used to provide Power, Thermal Management, and Automation. State-of-the-Art mmWave instrumentation was integrated into the tester, capable of calibrating and testing the individual RF ports. The Tester was integrated to an off-the- shelf Handler with Active Thermal Control. A load board with an elastomer-based contactor was developed to enable integration of the Tester to the Handler and DUT Testing. Direct RF Compliance Testing was enabled at interconnect speeds enabled by the EMIB Package Technology. Key RF current Tester capabilities are listed in Table 4:

TABLE 4. RF TEST CAPABILITIES

RF Test Capability	Specification
RF Testing Frequency Range	0-40GHz, Wide Band
Number of RF Ports	8 Receiver (ADC) 8 Transmitter (DAC)
Tcase Test Temperatures	-20 °C to 150 °C
Package Sizes	≤ 77x77mm
BGA Pitches	≥0.94mm

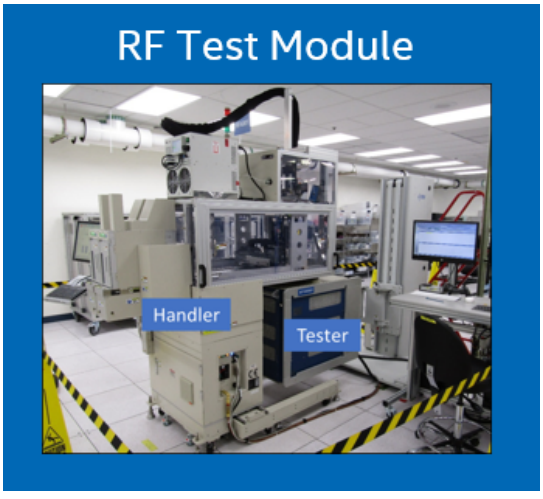

Fig 6. Test package for EMIB package quality and reliability validation

V. Microelectronics Quantifiable Assurance

To improve supply chain robustness and security the MQA analysis efforts have been kicked off for the SHIP program. MQA defines efforts to protect DoD intellectual property and to ensure national security, as relevant to microelectronics technologies. MQA provides guidance for managing microelectronics supply chain risks across the design, assembly, testing and failure analysis areas. The focus of MQA is to (a) understand key threats that relate to malicious modification or theft of design, process, or physical item; (b) perform detailed analysis of existing business process in the design, manufacturing, logistics, materials, and test areas; and (c) assess the existing mitigations and gaps to address potential threats. The MQA process supports IP protection and secure manufacturing of U.S based state of the art semiconductor packages. MQA leverages the use existing supply chain and materials, process, tools, and labs to develop high-performance heterogeneously integrated advanced packaging solutions.

VI. Conclusion

Heterogeneous integration is a key technology, enabling scaling in size, weight, and power advantages in next generation electronics. Under the SHIP program, Intel developed a high-performance RF MCP, codenamed MCP1, by integrating external companies RF ADC and DAC tiles with Intel Agilex™ device using the EMIB packaging technology and AIB standards. The integrated MCP provided up to 8x savings in SWaP when compared to alternative solutions using discrete components. The test package and the MCP1 product were subjected to environmental stresses to understand their reliability performance. The product and the test package with EMIB technology have exceeded the reliability criteria as defined in JEDEC for TC, HTSL and HAST stresses. DoD and Intel further their partnership to enhance IP protection and security of state-of-the-art U.S. based manufacturing of semiconductor packages through MQA.

VII. ACKNOWLEDGEMENT

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