Insights into the Design and Manufacturing of On-Chip Electrochemical Energy Storage Devices

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With the general trend of miniaturization of electronic devices especially for the Internet of Things (IoT) and implantable medical applications, there is a growing demand for reliable on-chip energy and power sources. Such tiny modules are expected to occupy no more than footprint-sized areas of a few square millimeters so that they can be easily integrated on semiconductor chips, while manufactured and packed using compatible approaches with current semiconductor processing. They are designed to provide power in the range of several μW to hundreds of mW and energy in the range of several hundreds of μWh to several mWh. Along with other emerging power sources such as miniaturized energy harvesters which cannot work alone, various miniaturized on-chip Electrochemical Energy Storage (EES) devices, such as micro-batteries and micro-supercapacitors, have been developed in the last two decades to store the generated energy and respond appropriately at peak power demand. One of the promising designs for on-chip EES devices is based on interdigitated three-dimensional (3D) microelectrode arrays, which in principle could decouple the energy and power scaling issues. The purpose of this summary article is to give a generic view of our recent works on designing and manufacturing on-chip miniaturized EES devices in particular 3D EES devices based on carbon microelectromechanical systems (C-MEMS) [1-6]. We also discuss some emerging opportunities in both materials and manufacturing for such applications.

Carbonaceous materials (including 1D and 2D nanomaterials), which have rich and tunable microstructures and surface chemistries depending on how the carbon is hybridized and assembled into 1D, 2D or 3D networks, are widely used as electrochemical active materials in EES devices. For the manufacturing of 3D carbon electrode arrays, one of the most promising and distinctive methods is the C-MEMS process, where photoresist can be patterned by photolithography and subsequently pyrolyzed into carbon at high temperatures in an oxygen-free environment. By changing the lithography conditions, pyrolysis temperatures and ramping rates, surface activation procedures, etc., we have demonstrated that C-MEMS can lead to 3D architectures with a wide variety of electrical, mechanical and electrochemical properties. The first prototype on-chip 3D C-MEMS micro-battery with interdigitated electrode array configuration is based on carbon micropillars array as one set of anode electrode, and electrochemically polymerized polypyrrole (PPy) micropillars array as another set of cathode electrode (Fig.1A). Both electrodes can be reversibly intercalated with lithium. An areal capacity of 10.6 μAh cm^{-2} was demonstrated for the functional full battery cell with relatively good stability and cyclic lifetime. Despite the limited battery performance, it was an important milestone as it demonstrated the first functional 3D on-chip micro-battery and how C-MEMS can be viewed as a very promising process for the emerging 3D on-chip EES technologies [2].

Following the first generation 3D micro-batteries, beyond developing high aspect ratio (> 50) electrode arrays, in the following couple of years our efforts were mainly focused on further increasing the surface areas and modifying carbon surface by activation of carbon surface and integrating high performance electrochemical active materials, such as: conductive polymer, 1D carbon nanotubes (CNTs) and 2D graphenes [3-7]. The goal was to develop on-chip electrochemical capacitors (ECs) or supercapacitors which are known for their exceptional power handling capabilities coupled with long cycle lives. ECs are typically subdivided into (i) electrochemical double layer capacitors (EDLCs), which store energy electrostatically at the electrode/electrolyte interface and the capacitance is governed by the thickness of the double layer, (ii) pseudo-capacitors, where the capacitance arises from the fast and reversible charge transfer between the electrode and the electrolyte, and (iii) hybrid capacitors, which essentially combines the two charge storage mechanisms. Lithium ion capacitor (LIC) is one of the examples pairing an EC

electrode with a Li-ion battery electrode. We have reported on the fabrication and characterization of various generations of on-chip micro-supercapacitors through C-MEMS technology [3-7]. On the one hand, the specific capacitance of as-prepared C-MEMS electrodes could be improved dramatically by electrochemical activation [3] and integration of CNTs (Fig.1B) and graphenes on the electrodes [5,6]. On the other hand, our approach can enhance the energy and power densities of micro-supercapacitors by employing a combination of a high surface area C-MEMS current collector and a pseudocapacitive material with high capacitance (such as: PPy and MnO_2) [4, 7]. In particular, graphene based on-chip micro-supercapacitors in 2D architecture show superior areal capacitance and excellent time constant [8]. The performance is typically hindered by the fact that graphene sheets tend to aggregate and restack not only during the processing phase but also because of the poor product quality from most commercial suppliers (the majority of commercially-available graphene products have high percentage of graphite microplates and less of graphene). The actual accessible surface area of graphene electrodes is in fact much lower than the theoretical one which can exceed 2600 $m2g^{-1}$. We demonstrated two effective strategies to avoid the aggregation and restacking issue encountered with graphene electrodes. Using CNTs as spacers between graphene sheets proved to help in preventing their restacking, but also adopting in-plane interdigital design helped increasing the accessibility of electrolyte ions to the capacitive material [8]. The micro-supercapacitors with interdigital microelectrodes (100 μm width and 50 μm spacing) were fabricated using Electrostatic Spray Deposition (ESD) and photolithography lift-off (Fig.1D). Cyclic voltammetry measurements showed that the specific capacitances of the devices based on rGO-CNT composites are 6.1 $mFcm^{-2}$ at $0.01Vs^{-1}$ and 2.8 $mFcm^{-2}$ at 50 Vs^{-1}, respectively. The resistive-capacitive time constant was as low as 4.8 ms, demonstrating exceptionally high rate capability and power handling performance. Another example of fabrication method is by using the concept of bipolar electrochemistry (BPE) to in-situ exfoliate sacrificial graphite substrate, and deposit and reduce graphene on an auxiliary electrode (Fig.1E) [9]. During the BPE, oxidation and reduction occur on both sides of the graphite placed wirelessly between two feeding electrodes in an electrochemical cell filled with DI water. Note that the BPE technique is also applicable for the exfoliation and deposition of other 2D materials and van der Waals heterostructures [10]. Using graphite, it was found that the deposition of GO took place on the positive feeding electrode with an areal capacitance of 0.404 mF cm^{-2} at a scan rate of 2 mV s^{-1}, whereas rGO was on the negative feeding electrode with areal capacitance of 1.932 mF cm^{-2}, at the same conditions [9]. The devices also showed high cycle stability and capacitance retention suitable for energy storage purposes. In terms of frequency domain response, the negative electrode-based rGO device outperforms the positive electrode-based GO device due to the vertically-aligned structure of rGO electrodes which is favorable for fast and effective electrical charge storage and ionic transport. At -45 deg. impedance phase angle, the cutoff frequencies were 1820 and 1157 Hz for the GO positive and rGO negative feeding electrode-based devices, respectively [9]. In addition, we verified, thanks to their low effective resistance, that both devices are suitable also for ac line filtering applications in a way comparable to commercial aluminum electrolytic capacitors. Furthermore, because the electrical response of most EDLCs is known to exhibit a distributed resistive-capacitive behavior which can be easily recognized from the deviation of the spectral impedance phase angle from the expected -90^{o} of an ideal capacitor as the frequency is increased, we have carried out quite a few research works on fractional-order capacitors (FOCs). The results indicate that 2D materials (graphene and phosphorene by BPE) based FOCs exhibit both tunable low frequency impedance phase angle and energy storage capabilities [9-11]. We also observed a memory effect in non-ideal capacitive devices via a non-local memory trace term that takes into account all prior history of the device in order to estimate its present state. This concept can be ”harvested” and used for electronic applications, and determining ageing effects and material degradation [12,13].

Although on-chip electrochemical capacitors could offer high power density and high-frequency response, the main drawback of these devices is the low energy density. Two of the promising strategies to overcome such a limitation include (1) asymmetric ECs realized by the combination of EDLC and pseudocapacitive electrodes [14], (2) LIC based on the combination of the redox storage and surface storage mechanisms. For example, various lithiation approaches were developed to enable lithiated carbon anode and activated

carbon cathode based LICs with promising electrochemical performance [15,16]. We have also demonstrated an aqueous on-chip LIC based on C-MEMS platform, where oxygen plasma-treated 3D carbon microelectrode arrays served as the capacitor-type anode while $LiFePO_4$ integrated on the 3D carbon microelectrode arrays served as the battery-type cathode with an areal density up to ~5.03 $\mu Whcm^{-2}$ (~5 times higher than the oxygen plasma-treated symmetric C-MEMS based EC) (Fig.1C) [17].

In terms of electrolyte type, composition and state, solid and semi-solid electrolytes are considered to be the most suitable for on-chip applications. In addition to developing high performance microelectrode arrays, we also developed novel patternable solid electrolytes based on semi-solid modified SU-8 photoresist mixing with lithium salt, which could be directly formed on electrodes to achieve solid-state miniaturized batteries and capacitors. The mSU-8 gel electrolyte shows high ionic conductivity (52 $\mu S\ cm^{-1}$), good electrochemical stability window of 0 to 5.3 V vs. Li, good mechanical rigidity, and the ability to photopattern with micron-scale resolution. We have achieved good elastic modulus which is nearly three orders of magnitude greater than comparable gel electrolytes (4.2 GPa) and good thermal stability for up to 250 ˚C. The half-cell galvanostatic testing has validated its use for on-chip EES applications [18].

In the last couple of years, another leading edge of manufacturing 3D carbon microelectrodes has been reported by DTU team based on combining lithography approach with additive manufacturing. The approach was reported in 2020 where well-defined freestanding complex 3D carbon microstructures based on stereolithography printing and pyrolysis were fabricated (Fig.1F) [19]. Following this work, another report was published by using hybrid microfabrication based on both photolithography and 3D printing, which opens up new carbon microfabrication possibilities for not only on-chip EES applications but also sensor devices, lab-on-chip applications and others. The precursor materials for carbon microfabrication are expanded from patternable photoresists to many commercially available resins and other polymers [20]. In addition to the 3D printing, direct laser pyrolysis in an inert environment using laser writer is another new carbon micro and nanofabrication trend [21]. Although there are issues related to resolution and uniformity, direct laser pyrolysis is surely revolutionary for writing carbon microelectrodes directly on flexible polymer substrates for wearable electronics applications.

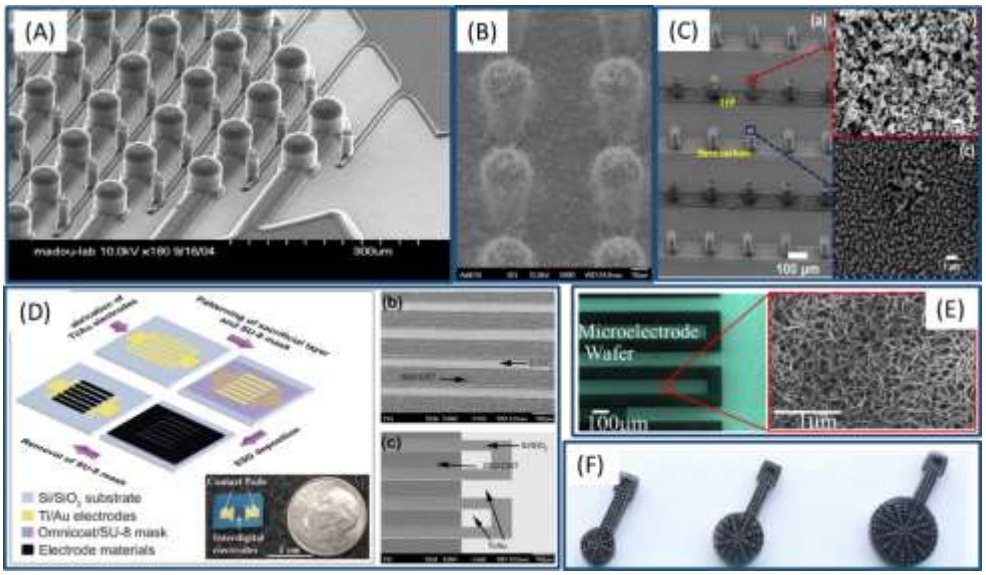

Fig 1. Efforts toward developing high performance carbon microelectrodes

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