TC-EDMS: Advances in high-performance electronic system analysis

The growth of data center computing power and the increase in the amount of data being transmitted within and between systems is driving interesting and innovative ways to design electronic systems. Building the systems with robust, predictable, and energy-efficient electrical performance is essential to designing and manufacturing complex systems that scale with the exponential increase in computing and networking operations.

A core interest of members of the IEEE EPS technical committee on EDMS (electrical design, modeling, and simulation) is developing the technology needed to produce these systems. Within EDMS, there are several activities that address the challenges being faced. This article gives an overview of the scope of activities and how EDMS plays a part in supporting the members and the broader community in their efforts.

There are three current activities in which EDMS plays an important role that illustrates the breadth of opportunities for the members to participate: conferences, roadmaps, and a benchmark offering. In October, the 29th EPEPS conference (Electrical Performance of Electronic Packaging and Systems) was held, the 2020 update of the HIR (heterogeneous integration roadmap) is being completed, and a benchmark subcommittee of EDMS has been working hard to make designs available for the community to use.

The quest for the ability to solve problems we couldn't address before pushes toward new system architecture and quantum is a visible example of that desire. There is much discussion about when quantum computers will have the capacity to start replacing classical computers, but the complexity of quantum computing is already having an impact on the work of the community. The impact includes the physical design of the various quantum devices, each innovative in their own way where a low-noise environment for long-term entanglement is needed and that leverages the electrical and thermal design expertise of our community. Quantum-safe security is required even in classical computers, not only in the algorithms, but also in the design of the hardware to prevent observation of signals in operation. Engineers interested in this area had an opportunity to learn more as Dr. Jim Held of Intel presented a keynote on quantum computing at EPEPS. Also, the HIR chapters are introducing quantum computing into their roadmaps including the chapter on high-performance systems.

The quantum computing may be forward looking, but there are plenty of challenges on classical systems. As the EDMS name articulates, the modeling and simulation is the core interest of our technical community. At the EPEPS conference, a keynote by Dan Dreps of IBM gave an excellent overview of the design of high-speed, large-bandwidth links and the role that modeling and simulation play in that design. Dr. Vaishnav Srinivas of Qualcomm gave an invited presentation on signal and power integrity from architecture definition to silicon implementation that was well-received. Focus on multi-level signaling such as PAM-4 and optical integration are two of the areas that stress the modeling and simulation tools and as a result are of topical interest to members of EDMS.

In addition to conference support and HIR support, EDMS is well along in creating a database of designs that can be used as a benchmark reference. The EDMS technical community has identified the need of advancing electrical tools and methodology and the benefit of having readily available designs to it is helpful to have some example design files that can be used as benchmarks for the community. We have a subcommittee co-chaired by Dr. Fei Guo of AMD and Prof. Ali Yilmaz of UT-Austin that is developing this database of benchmark designs that can be used by the community. Currently, there is a benchmark that has approved for use and should be available soon. Two more candidate designs are in development. This has been an active committee and expect that more benchmark designs will be needed to continue the development of the tools and methodologies needed for these ongoing challenges. It is our desire that these benchmarks can assist researchers and practitioners in their work.

Industry leading advances in numerical modeling methods are presented at the EDMS conferences. As a good example, the best conference and student papers at EPEPS this year were on uncertainty quantification [1] and nonlinear circuit blocks [2]. Machine learning algorithms are beginning to be applied to the analysis of these designs and are an important part of the EDMS conferences. These methods are applied to high-speed interfaces whether they be high-speed serial interfaces running PAM-4 signaling or wide package level traces for chiplets have an increasing complexity with restrictive requirements for crosstalk noise and power supply induced jitter.

In summary, the systems that our community designs are changing either in complexity such as chiplets, or in architecture such as quantum. The package centric nature and complex implementation with heterogeneous integration with its interaction of signal distribution, power distribution, thermal management, and EMI requires diligence in the development of the design, modeling, and simulation tools. The benchmarks provide a basis for the fundamentals of modeling and simulation that is needed for a robust modeling and simulation methodology. The advance of systems will be more complex than the benchmarks, but relevant benchmarks can guide the development of the desired analysis capability.

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[1] Z. He and Z. Zhang, "High-Dimensional Uncertainty Quantification via Active and Rank-Adaptive Tensor Regression," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2020, pp. 1-3, doi: 10.1109/EPEPS48591.2020.9231388.

[2] T. Bradde, S. Grivet-Talocia, G. C. Calafiore, A. V. Proskurnikov, Z. Mahmood and L. Daniel, "On Dissipativity Conditions for Linearized Models of Locally Active Circuit Blocks," 2020 IEEE

29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2020, pp. 1-3, doi: 10.1109/EPEPS48591.2020.9231316.