IEEE EPS High Density Substrates & Boards Technical Committee News

Yasumitsu Orii, High Density Substrates and Boards TC Chair

The High Density Substrates & Boards technical committee (TC-6) of the Electronics Packaging Society EPS is focusing on high-speed and high-density interconnect technologies, based on advanced material-, process-, structure-, and design-technologies. Application areas are ICTs, mobile electronics, automobiles/power electronics, and healthcare. High density substrates and boards are the key components placed in the center of the equipment and always need to be evolved correspondingly to the cutting edge technologies in electrical, optical, and thermal fields.

The current TC-6 committee organized in 2003, gathering the technical leaders with a variety of skills from several Japanese companies. Their activities started by summarizing state-of-the-art material technologies developed in Japan in those days.

The findings unveiled in ECTC2004 Special Session, entitled “High Density Build-up Printed Circuit Boards Technology”. The session won popularity and was raised to the annual event of CPMT Seminar (current EPS Seminar) in ECTC since then.

The TC-6 activities have gradually changed in the last two decades. In the early days, topics were mostly material-related, such as, how-to-use the new dielectrics, flexibles, and bumps; as shown in CPMT Seminar topics, “Advanced Flexible Printed Circuit Board Technologies” in 2005, “Bump and Bump-less Interconnection” in 2010, and “Nanotechnologies for Packaging” in 2009. These days the main topics are, however, shifted to the requirement for substrates from applications such as HPC, smartphone, and AI hardware; for example, “Systems, Devices, and PKG Tech for IoT & Hyper-Connected Society” in 2016, “HPC Packaging” in 2018, and “Roadmap of IC PKG Materials to Meet Next-Generation Smartphone Performance Requirement” in 2019. And then this year TC6 organized the hottest special session “Future Semiconductor Packages for AI hardware” at ECTC2020. This session attendance was 727 and the duration was 71.4min which is the 3rd longest time. The chairs are Yasumitsu Orii, NAGASE & CO., LTD. and Shigenori Aoki, LINTEC Corporation.

< Session Outline >

An overwhelming amount of data is generated daily, out of which 90% is unstructured. Such data cannot be easily stored in a traditional column-row database, therefore, it is not easily searchable and more difficult to analyze. Today, artificial intelligence (AI) has the ability to analyze unstructured data, however, it also requires a high amount of energy. AI is expected to become one of the biggest energy consumers on the planet. Brain-inspired devices and quantum devices are very attractive to support future AI due to its low power consumption. In this session, the speakers discussed the future semiconductor packages in the era of brain-inspired devices and quantum devices.

< Session Highlights >

Rama Divakaruni, IBM T. J. Watson Research, “Future of Innovation - IBM AI HW Center”

Today's bits computing is transforming to neurons computing and then to qubits era. Heterogeneous integration is extending fan-out WLP, interconnect bridge, 3D stacking, high density laminate, and photonics market addressing accelerator and memory interconnect bottleneck. The amount of compute used by the largest AI training is doubling every 3.5 months. The AI system could be unsustainable without materials, hardware, algorithms, and software innovation.

Hiroyuki Akinaga, AIST, "Brain-inspired ReRAM Devices for AI-edge Computing"

ReRAM (Resistive Random Access Memory) RAND (Resistive Analog Neuro Device) is one of the best candidates as an alternative to Moore's law. The target is AI devices in edge computing across AV&IT network, ubiquitous network, intelligent robots. ReRAM is NVM (Non-volatile memory) with a resistive change layer running in ~10ns and designed for multiply accumulate operation circuits with 4M synapses which is capable of 66.5 TOPS/W.

Subramanian S. Iyer, UCLA, "Why all this hype about Heterogeneous Integration?"

Compute challenges are larger chip size, memory capacity, access limitation, and increasing dark silicon. Heterogeneous Integration drives the key packaging technologies such as fine pitch direct Cu-Cu thermal compression bonding using formic acid vapor, Super CHIPS versatile communication protocol, photonics interconnects, and analog inference.

Takashi Hisada, IBM Research-Tokyo, "Heterogeneous Integration for IBM AI HW"

In memory crossbar array neuromorphic device with NVM is addressing von Neumann bottleneck. Lots of structures are proposed for AI accelerator and the bridge type of interconnect is attractive as a solution for high yield finer patterning. High density Chiplets increase the number of I/Os, die size, complexity, asymmetricity, and mechanical stress. Electrical thermal mechanical concurrent modeling is required for CPI(Chip Package Interaction).

Madhavan Swaminathan, Georgia Tech, "Intelligent Digital and RF Convergence for AI"

AI system of neuromorphic sensing, neuromorphic compute, and in-memory compute will address Moore's law slowdown because of the memory wall and heat wall. It features photonics interconnect achieving low energy consumption at <1.2pJ/bit while high data rate at 896Bb/s. Integrated power delivery is improved by complement GaN power FET and embedded high density inductor. Glass interposer in a panel is more cost effective than wafer based Si interposer.