The Test Roadmap Working Group is composed of 145 experts coming from 55 companies world-wide. This size of a team is appropriate given the complexity of the test in the Semiconductor industry. Not only do we have responsibility for determining good parts from bad, we also play a commanding role in tracking process parameters, product yields, and product reliability. Additionally, changes in test are nearly continuous as we strive to keep ahead of the latest industry challenges such as continuing Moore's law growth which is being compounded by heterogeneous integration techniques, 5G mobile phone components, photonic interfaces, and requirements for data sharing which conflict strongly with security and proprietary data concerns.

This year's Test Roadmap encompasses focused white papers on six key device testing technologies (logic, RF, Analog, Memory, Photonic, and Specialized Devices). It also includes discussions around device handlers and test interface products (probes, sockets). Finally, it explores trends in areas with the leading testing technologies such as DFT, 2.5D testing, Reliability Testing, Yield Learning, and Concurrent & Adaptive Testing techniques. Altogether the 2017 Test Working Group roadmap include 15 white papers and 14 detailed tables of data.

With the possible exception of challenges in the photonic probing area, the Test roadmap does not highlight any significant technical roadblocks. The industry knows how to do what it needs to do for devices which are expected over the next five to ten years. That's not to say that we don't have significant non-technical challenges.

As the device complexities continue to rise, test times and test development efforts will scale in a non-linear fashion. While it would be great if 50% more circuity just meant 50% more test time and effort but this is simply not the case. Fault observability and test controllability are complicated by more levels of circuitry. Exasperating this situation, the more circuitry we put into smaller and smaller areas the more noise paths which are created.

The industry is working hard to confront these challenges by deploying higher levels of pattern compression, creative simultaneous testing techniques for similar logic blocks, and it is actively embracing built-in-self-test (BIST).

Certainly, the biggest test challenges on the horizon are for super-wide bandwidth interfaces planned for RF and photonic devices moving forward. The world's push more and more conductivity demands that test gear up to handle many more interfaces running at much faster data rates. This is our challenge which we have chosen to accept. The Test Roadmap shows that this won't be easy but it is doable.

Call to Participate: New volunteers to the Test Technology Working Group are always welcome. Contact Dave.Armstrong@Advantest.com for more information.