

Title: Nanopackaging for AI and power delivery

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Time: 11AM EST (8AM PST)

Speakers: Dr. Siddharth Ravichandran and Prof. Kuan-Neng Chen

Moderator: Dr. Srikrishna Sitaraman

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Abstract:

The proliferation of artificial intelligence (AI) applications has increased the demand for compute performance and memory capacity. This is happening at a time when the semiconductor industry is facing challenges associated with the slowing down of Moore's Law. Chiplet integration using nanopackaging is being viewed as a critical enabling technology for supporting AI applications. Such highly integrated systems require a multitude of materials to support electrical, mechanical, thermal, and chemical properties. In addition, these materials need to be compatible with packaging processes to ensure compatibility with low-cost manufacturing solutions. The interplay between the various engineering domains makes the selection of nanoscale materials, their processability, and compatibility extremely complex. In the first part of the talk, we investigate the future in terms of the requirements posed by materials for advanced packaging and review the past and present work in nanomaterials and nanopackaging techniques to enable this trend. As the most significant current 3D integration key technology, bumpless Cu-based hybrid bonding has become the main solution to meet the requirement of high speed and density. The second part of the talk will discuss the current status and technology trend of hybrid bonding, as well as challenges and solutions to low-temperature hybrid bonding.