Special Session for ECTC2022
Organized by
TC6 High Density Substrates & Boards

January 30, 2022
Yasumitsu Orii, TC6 Chair
Topics: Interconnect Technologies for Chiplets

For 50 years, the number of transistors that could be squeezed onto a piece of silicon had increased on a predictable schedule known as Moore’s law. However, the Moore’s law is reaching to the end. The new approach comes with “chiplets” which is something like high-tech Lego blocks. Instead of carving new processors from silicon as single chips, semiconductor companies assemble them from multiple smaller pieces of silicon—known as chiplets. We will discuss the several interconnect technologies for Chiplets such as Silicon Bridge, Advanced Interposer, Fan-out wafer-level packaging, and optical interconnection. We will have 6 panelists and each panelist will prepare a short set of slides to present within 10-15 minutes, followed by panel discussion.

Organized by High Density Substrate and Board (TC6)

Chair: Yasumitsu Orii (NAGASE)
Co-Chair: Shigenori Aoki (LINTEC)

< Panelists >
• Ravi Mahajan, INTEL, “HI Interconnects for today and tomorrow”
• Akihiro Horibe, IBM Research Tokyo, “Direct Bonded Heterogenous Integration DBHi Si Bridge”
• Yu-Hua Chen, Unimicron, “The Challenges of Advanced Substrate for Heterogenous Integration”
• Shin-Puu Jeng, TSMC, “Heterogeneous integration approaches in foundry”
• Yu-Po Wang, SPIL, “Trend and Solution for Memory Integrated Advanced Packages”
• Hideyuki Nasu, Furukawa Electric “High-Density Optical Transceivers and Pluggable Electrical Interfaces for Co-Packaged Optics”