IEEE ELECTRONICS PACKAGING SOCIETY Newsletter

IEEE

JULY 2018
VOL. 40 NO. 2
ISSN 1077-2999

Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Avram Bar-Cohen, PhD, Principal Engineering Fellow, Raytheon—Space and Airborne Systems, Arlington, VA

Dear Colleagues, friends, and members of the Electronic Packaging community:

I am just back from San Diego and still basking in the glow of our most successful ECTC Conference ever. This Conference, as the electronic packaging community we serve, has grown enormously in size and in impact since its inception in 1950 in Washington DC as the "Symposium of Improved Quality Electronic Components." The success of that Symposium resulted in a second symposium in 1952 and annual meetings for the subsequent 66 years; since 1962 with joint sponsorship by IEEE and EIA, and solely under our auspices for the past 7 years. The approximately 1750 participants in this year's ECTC, along with nearly 400 in the co-located thermal-packaging ITHERM Conference, constituted the largest gathering of Packaging professionals in the history of our Society, totaling almost 2500 attendees. The two Conferences also provided us all with the opportunity to meet and help recognize, through the EPS, ECTC, and ITHERM awards, some of the incredible engineers and scientists who have made Packaging what it is today.

I would like to take this opportunity to thank the ECTC Executive and Program Committees, the ITHERM Executive and Program Committees, the Board of Governors and members of the EPS Society, who along with the ECTC, ITHERM, and EPS staff, have made this the premier annual event of the electronic packaging community. We are fortunate to have so many of you actively engaged in these two Conferences and we are indebted to the large, highly-skilled, and enthusiastic team that keeps finding new ways to enhance and better integrate these Conferences.

The ECTC/ITHERM attendees and the nearly 3000 additional participants in our flagship Asia-Pacific Conference (EPTC), our flagship European Conference (ESTC), and the other EPS sponsored and co-sponsored Conferences, as well as the 10's of thousands who regularly download EPS papers thru Xplore, have helped to establish the broad, international footprint of this Electronics Packaging Society. Together we are heirs to a rich history of leading and giving witness to successive revolutions in component and packaging technology.

There has never been a time in our history when Packaging Science and Technology was more prominent or better positioned for future impact on our community. As we well know, the current wave of expansion and change in the electronics industry has identified electronic packaging as a cutting-edge value creator and product differentiator. With growing frequency, packaging is driving change in the microelectronic industry, building on innovations in 2.5D and 3D packaging, compound semiconductor materials, and heterogeneous integration to lay the groundwork for the approaching inflection in IoT technology, a new 5G generation of telecommunication hardware, and the introduction of new computational modalities, from quantum to neuromorphic computing.

As you have heard—or read—me say before, I believe that our new name—the Electronics Packaging Society—and the changed dynamics of the electronic industry provide us with a unique opportunity to:

- Take ownership of, i.e. Brand, Packaging and Interconnection across all scales and applications;
- Drive industry recognition for the strategic value of packaging, and
- Become the premier source—within IEEE and the broader community—of packaging and integration knowledge and expertise.

But we cannot succeed in realizing this EPS Vision without your engagement and commitment. As members of IEEE and

(continued on page 9)

NEWSLETTER SUBMISSION DEADLINES

1 December 2018 for Winter issue 2019

15 June 2019 for Summer issue 2019

Submit all material to d.manning@ieee.org

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Sr. Past Pres.:	Jean Trewhella	jean.trewhella@GLOBAL FOUNDRIES.com
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Members At Large

2018 Term End: Regions 1-6, 7, 9—Philip Garrou, Eric Perfecto; Region 8—Karlheinz Bock; Region 10—C. Robert Kao, Andrew Tay, Suresh Subramanyam

2019 Term End: Regions 1-6, 7, 9—Li Li, David McCann, Kitty Pearsall, Subramanian S. Iyer; Region 8—Thomas Brunschwiler, Gilles Poupon

2020 Term End: Regions 1-6, 7, 9—Alan Huffman, Sam Karikalan, Xuejun Fan, Jeff Suhling; Region 8—Grace O'Malley; Region 10—Yoichi Taira

Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:
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Power & Energy:
Patrick McCluskey

RF & Thz Technologies:
Manos Tentzeris

Green Electronics:
Nils F. Nissen

Photonics—Communication, Sensing, Lighting:
Gnyaneshwar Ramakrishna,

3D/TSV:
Paul Franzon

Reliability:
Richard Rao

Program Directors

Membership Programs: Jeffrey C. Suhling, jsuhling@auburn.edu

Chapter Programs: Kitty Pearsall, kitty.pearsall@gmail.com

Awards Programs: Eric Perfecto, eric.perfecto@globalfoundries.com

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Region 8 Programs: Toni Mattila, toni.mattila@investinfinland.fi

Region 10 Programs: Yasumitsu Orii, yasumitsu.orii@nagase.co.jp

Standing Committee Chairs

Fellows Evaluation: CP Wong, cp.wong@ieee.org

Long Range / Strategic Planning: Jie Xue, jixue@cisco.com

Nominations: Jean Trewhella Jean.Trewhella@ globalfoundries.com

Distinguished Lecturers

Program Director: Beth Keser, beth.keser@intel.com

Lecturers: Mudasir Ahmad, Muhannad Bakir, Ph.D., Avram Bar-Cohen, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., Moises Cases, William T. Chen, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., R. Wayne Johnson, Ph.D., Beth Keser, Ph.D., John H. Lau, Ph.D., Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., Ravi Mahajan, PhD., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Michael Pecht, Ph.D., Eric D. Perfecto, Karl J. Puttlitz, Ph.D., Dongkai Shangguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

IEEE Electronics Packaging Society Newsletter is published quarterly by the Electronics Packaging Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US $1.00 per member per year is included in Society fee for each member of the Electronics Packaging Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE EPS Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. For circulation information call IEEE Customer Service 800-701-4333, or FAX 908-981-9667.

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SFI Logo

The Next Phase of Innovation: Heterogeneous Integration

We are entering the era of digital economy and myriad connectivity. Look around you: the migration of data to the cloud, presence of smart devices everywhere and the emergence of autonomous vehicles are all great examples.

Recently, artificial intelligence and big data analytics have been undergirding the technical advances in every market. At this inflexion point, though, with the plateauing of semiconductor scaling and the explosive expansion of electronic products into global society, continued technological progress will require a new phase of electronics innovations.

Heterogeneous integration is rapidly becoming the key technology for the next decade, and will initiate a new era of technological and scientific advances. Heterogeneous integration refers to the integration of separately-manufactured components into a higher-level assembly that, in total, provides enhanced functionality and improved operating characteristics.

Packaging, for both systems and devices, will be the vanguard to this enormous advance. As a result, heterogeneous integration has become the highest strategic initiative of the IEEE Electronics Packaging Society (EPS), from conferences, publications, education, technology, and industry outreach.

Heterogeneous Integration Roadmap (HIR), initiated by EPS is now sponsored by three IEEE Societies together with ASME EPPD and SEMI, is at the forefront of this strategic initiative. Our vision is to colloaborate with organizations with likeminded vision and open governance.

The mission of the Heterogeneous Integration Roadmap is to provide guidance to the profession, industry, academia and government on key technical challenges with sufficient lead time to prevent them from becoming roadblocks to continued progress in electronics. That progress is essential to the future growth of the industry, and to the realization of technology's promise of continued positive impact on mankind.

We would like to invite the readers to access the Heterogeneous Integration Roadmap page in the EPS Website under Technology under the link: http://eps.ieee.org/technology/heterogeneous-integration-roadmap.html

The readers will find information on

- *Background*
- *Mission*
- *Purpose*
- *Committee*
- *Global Advisory Council*
- *Scope*
- Technical Working Groups
- Global Events

We had a very successful 1st Heterogeneous Integration Roadmap (HIR) Symposium in Santa Clara sponsored by the EPS Santa Clara Chapter. This was followed by HIR Workshop at ECTC-ITHERM Conferences in San Diego May 29th. This month in July we shall have work session at SEMICON West in San Francisco. These face to face work sessions together with weekly conference calls is designed to bring us to publication of the 1st edition of the Heterogeneous Integration Roadmap in September, We believe that with the rapid and disrutive changes in our industry, annual revision will be in order. This will be our goal.

Contributor: William Chen
IEEE Fellow

2018 IEEE Electronics Packaging Society Award Recipients

William T. Chen
An IEEE Fellow, ASE Fellow and senior technical advisor with ASE Group, Inc., Sunnyvale, CA

2018 IEEE Electronics Packaging Award
For contributions to electronic packaging from research and development through industrialization, and for his leadership in strategic roadmapping efforts.

Note: "Please read a Q&A with Bill Chen later in the newsletter"
IEEE grade to award winners:

- Douglas Yu: IEEE Fellow
- Pradeep Lall: IEEE Fellow
- Muhannad Bakir: IEEE Senior Member
- Kuan-Neng Chen: IEEE Fellow
- Katsuyuki Sakuma: IEEE Senior Member
- Jean Trewhella: IEEE Senior Member
- Annette Teng: IEEE Senior Member
- Gilles Poupon: IEEE Senior Member
- Yoshitaka Fukuoka: IEEE Fellow

Douglas Yu, IEEE Fellow
Taiwan Semiconductor Manufacturing Company, Taiwan

2018 IEEE CPMT Electronics Manufacturing Technology Award
For contributions to the development and high-volume manufacturing of Interposers and Wafer-Level Fan-Out Packaging.

Pradeep Lall, IEEE Fellow
Auburn University, USA

2018 IEEE CPMT Outstanding Sustained Technical Contribution Award
For outstanding sustained contributions to the design, reliability and prognostics for harsh environment electronics systems.

Muhannad Bakir, IEEE Senior Member
Georgia Institute of Technology, USA

Kuan-Neng Chen, IEEE Fellow
National Chiao Tung University, Taiwan

Katsuyuki Sakuma, IEEE Senior Member
IBM T.J. Watson Research Center, USA

2018 IEEE EPS Exceptional Technical Achievement Award
For contributions to 2.5D and 3D IC heterogeneous integration, with focus on interconnect technologies.

Jean Trewhella, IEEE Senior Member
GLOBALFOUNDRIES, USA

2018 IEEE EPS David Feldman Outstanding Contribution Award
For 20 years of leadership consistently driving change, collaboration, and engagement in EPS and ECTC, including driving our society name change, sponsoring the Heterogeneous Integration Roadmap, and establishing the ECTC Student Reception.

Annette Teng, IEEE Senior Member
Promex Industries Inc., USA

2018 IEEE EPS Regional Contributions Award—Region 1-6, 7 & 9 (Americas)
For sustained contributions to the Santa Clara Valley Chapter and continued support of Chapter activities.

Gilles Poupon, IEEE Senior Member
CEA-LETI, France

2018 IEEE EPS Regional Contributions Award—Region 8 (Europe, Middle East, Africa)
For outstanding and sustained contributions and leadership in regional activities such as organization of international conferences and workshops, active volunteering in technical committees, and leading the EPS French chapter to one of the most active chapters in the region.

Yoshitaka Fukuoka, IEEE Fellow
Worldwide Electronic Integrated Substrate Technology Inc., Japan

2018 IEEE EPS Regional Contributions Award—Region 10 (Asia and Pacific)
For contributions to establish an International Japanese conference on electronic packaging and to provide the latest packaging technology information in Japan to the world.

Congratulations to IEEE EPS Senior Members

New IEEE EPS Senior Members
The members listed below were elevated to the grade of Senior Member between December 2017 and April 2018.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: https://www.ieee.org/membership/senior/application/index.html

Ian Harvey Arellano, Republic of Philippines Section
Hidetaka Hayashi, Tokyo Section
Randy Crutchfield, Phoenix Section
Shaowu Huang, Santa Clara Valley Section

ECTC 2018 Travel Award Winners

Congratulations to the winners of the 2018 ECTC travel award. The award is intended to assist students to attend ECTC.

- **Luca Del Carro**, ETH Zurich
- **Normand-Pierre Goodhue**, Université de Sherbrooke
- **Siva Chandra Jangam**, University of California, Los Angeles
- **Chenhui Li**, Eindhoven University of Technology
- **Tong-Hong Lin**, Georgia Institute of Technology
- **Nivesh Mangal**, Ghent University
- **Saikat Mondal**, Michigan State University
- **Bo Song**, Georgia Institute of Technology

Congratulations to the ECTC Volunteer Award Recipients

The EPS/ECTC Volunteer Award is given to those individuals who contribute to the success of the ECTC by volunteering in one of the conference committees, year after year. Here are the 2018 EPS/ECTC Volunteer Award winners:

Rozalia Beica	10 Years
Karlheinz Bock	10 Years
Zhaoqing Chen	10 Years
Vijay Khanna	10 Years

James Lu	10 Years
Mikel Miller	10 Years
Shichun Qu	10 Years
Sandeep Sane	10 Years

Matthew Yao	10 Years
Tieyu Zheng	10 Years
Thomas Reynolds	25 Years

EPS Major Awards Nomination Period Starts on September 15

For the first time all the EPS Major Award nominations will require line submission. The nomination period to input all the required documents runs from September 15 to January 21. The Electronics Packaging Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and EP Society.

Outstanding Sustained Technical Contributions Award
To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Must have been a member of the IEEE and EP Society for the past three (3) years (2016-2018), and renewed for 2019.

Electronics Manufacturing Technology Award
To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. Work in the management of EPS Conferences or its BoG may be contributory but it is not a requirement for the award.

Eligibility: No need to be a member of IEEE and EP Society.

David Feldman Outstanding Contribution Award
To recognize outstanding contributions to the fields encompassed by the EP Society through executive or managerial directions.

Prize: $2,500 and Certificate

Basis for Judging: Contributions to the organizations or enterprises connected with the field; contributions to EPS Chapter or Board of Governors activities; contributions to the fields encompassed by the EP Society.

Eligibility: Recipient must have been a member of IEEE and EPS for the past five (5) years (2014-2018), and renewed for 2019.

Exceptional Technical Achievement Award
To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the EP Society.

Prize: $2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in EPS's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for the past three (3) years (2016–2018), and renewed for 2019. There are no requirements for service to the IEEE or EP Society.

Outstanding Young Engineer Award
To recognize outstanding contributions to the fields encompassed by the EP Society through invention, technical development, publications, or new product implementation.

Prize: $1,500 and Certificate

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the EPS Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of

employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Must have been a member of the IEEE and EPS (member grade or above) for the past three (3) years (2016–2018), and renewed for 2019, and must be 35 years of age, or younger, on December 31, 2018.

Guidelines for Nominators:

- A recipient of any EPS Major Award will be eligible for nomination for another EPS Major Award *after two award cycles have passed*. (i.e., Recipient of XX Award in 2016 becomes eligible for nomination for YY Award in 2019). For lists of past awardees, see http://eps.ieee.org/awards.html
- Past recipients of an award are not eligible to receive that same award. For lists of past awardees, see http://eps.ieee.org/awards.html
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- An individual may submit only one endorsement per award but may submit endorsement for more than one award.
- It is the responsibility of the nominator to ensure quality documentation to assist the Awards Committee in evaluating the candidate.
- Outstanding Sustained Technical Contribution Award is designed for the "practitioner", while the Electronics Manufacturing Technology Award intended for "Corporate Leadership".
- Complimentary material, such as candidate›s picture, CV, list of publications and/or patents should be submitted separate from the award nomination.
- Self-nominations **will not** be considered.
- All nominations must be **online**. Nominations questions can be send to Society Awards Program director:

Eric Perfecto
GLOBALFOUNDRIES
2070 Route 52 MS: 6C1
Hopewell Junction, NY 12533
eric.perfecto@globalfoundries.com
ph: 845-894-4400

Winners will be notified by 9 April 2019, and the awards will be presented at the 69th Electronic Components and Technology Conference (ECTC), May 28–31, 2019 at the The Cosmopolitan of Las Vegas, Las Vegas, NV (USA).

Functional Teams—Rationale, Activities, and Future Plans

Early in 2018 the EPS Board of Governors established several Functional Teams to broaden the interaction between Officers and Members-at-Large around key issues for the Society and to nucleate and develop new initiatives that would provide added-value to EPS members and the community. Four Functional Teams were assembled: **Conferences and Education** – led jointly by Chis Bailey, VP of Conferences, and Beth Keser, VP of Education; **Membership**—led by Jeff Suhling, Director of Membership Programs, and **Technology**—led by Patrick Thompson, VP of Technology, as well as a small **Finance** Functional Team, led by Tom Reynolds, VP of Finance. The full membership of each Functional Team, including several EPS Directors and Members-at-Large, is listed below. It is anticipated that some Functional Teams will be retired, once their mission is completed, and that other Functional Teams will be created as needed to address emerging challenges and opportunities. We invite your comments on any and all of the activities of these Functional Teams and would very much welcome additional participants from among the EPS members in any of the FT's. Please write to Avi Bar-Cohen or Denise Manning to provide your feedback or volunteer for one of the Functional Teams.

Conference/Education Functional Team:
Due to the high connectivity of EPS conference and educational activities, as well as the principals' interest in both domains, it was decided to create a single, combined Functional Team for Conferences and Education. This Functional Team has pursued two primary initiatives:

1) Electronic Packaging Conference Asia Pacific (EPCAP)
EPS currently co-sponsors 8 separate events in the Asia-Pacific region, R10, with a total of approximately 700 attendees in the Financially-(co-)Sponsored Conferences and a similar number for the Technically-(co-)Sponsored conferences. The FT is exploring whether a larger, 1,000+ attendees, annual, fully-sponsored EPS Conference, building on the "best practices" established by ECTC, would better "brand" EPS and more effectively serve our members and the Packaging community in Region 10. The current discussion envisions building on and regionalizing EPTC—the EPS flagship Conference—and like ECTC, have it rotate across 3–4 R10 cities, include 50+ exhibits and sponsorships, provide broad topical coverage across all domains of Packaging, with special emphasis on emerging technologies. Moreover, it is hoped that the additional resources generated by such an EPCAP could be used to support Workshops and educational activities in the narrower topical areas covered by ICSJ, EDAPS, EMAPS, and IEMT, as well as new emerging areas, including 5G, "digital manufacturing," and Quantum, as well as Neuromorphic Computing.

2) EPS Proficiency Program
In addition to Continuing Education Units (CEU) and Professional Development Hours (PDH) for the EPS Professional Development Courses at our flagship Conferences, we are now offering PDHs for our webinars. The PDCs and webinars are growing in popularity and IEEE-wide surveys with non-members, especially Young Professionals, have identified a strong interest in additional "credentialing," at intermediate levels between Member/Senior Member

and Fellow. The Conference/Education FT is exploring the possibility of developing an EPS Proficiency Program that would recognize a participant's completion of a set number of the available PDCs and webinars, as well as "softer" skill IEEE webinars, with an EPS Proficiency certificate. Higher levels of Proficiency could also be recognized with higher-level certificates.

Membership Functional Team

Membership growth, especially in the Young Professional category, is a critical requirement for the future viability of EPS. The membership Functional Team is addressing 3 distinct areas of membership development: Student Members, Young Professionals, and new Chapter formation. In the Student category, the FT has recommended that students attending ECTC and/or ITHERM receive a "free" half-year membership in IEEE/EPS. Effort is also being devoted to reinvigorating existing Student Branch Chapters and developing new Student Branch Chapters on campuses with active electronic packaging programs. Other ideas under consideration, include: collecting student resumes and holding Job Fairs at EPS Conferences, adding Electronic Bulletin Board on the EPS website for packaging position announcements, developing a pool of EPS Mentors, made available through the EPS Website and Collabratec, and updating the list of Universities doing Packaging research.

EPS has appointed Yan Liu as its representative to the IEEE Young Professional Council and also to a 1-year term on the EPS BOG. Dr. Liu is recruiting an EPS YP Committee that will recommend a range of YP activities to the BOG.

The Membership FT is helping to develop a new SE New York Chapter and analyzing membership statistics to identify areas of membership concentration that could benefit from a local Section.

Technology Functional Team

The Technology FT has been examining ways to reinvigorate the EPS Technical Committees, with special emphasis on the Emerging Technologies Committee that plays a critical role in maintaining EPS' presence on the cutting edge of packaging technology. Under the guidance of Karlheinz Bock, the newly appointed Chair of the Emerging Technologies committee, is exploring the best ways to announce and manage a pilot White Paper competition on visions of "Packaging 2025," focused primarily on Young Professionals and Graduate students. It is expected that the Committee will solicit, review, and rank White Paper contributions from EPS members and invite the top teams to present their Vision(s) to the BOG, and—perhaps—attendees—at ECTC.

The FT is also seeking to play a role in coordinating and scheduling EPS Webinars with the VP-Education and look for other collaboration opportunities with the VP-Education and VP-Conferences. Identifying EPS representatives to IEEE-wide Councils and Working Groups remains a challenge and concern for this functional team.

Finance Functional Team

The Finance FT is engaged in reviewing and implementing IEEE-wide efforts to bring greater clarity and transparency to the budgeting and indirect/direct charging process. It is also helping to define the best ways to fund projects and initiatives that increase and improve the services and benefits to EPS members.

Conference/Education Functional Team

- Chris Bailey, EPS VP-Conference
- Beth Keser, EPS VP-Education
- Avi Bar-Cohen, EPS President
- Xuejun Fan, EPS Member at Large
- Alan Huffman, EPS Member at Large
- Grace O'Malley, EPS Member at Large
- Yasumitsu Orii, EPS Program Director – Region 10
- Andrew Tay, EPS Program Director – Student Programs

Membership Functional Team

- Jeff Suhling, EPS Program Director – Membership Programs
- Kitty Pearsall, EPS Program Director – Chapter Programs
- Andrew Tay, EPS Program Director – Student Programs
- Avi Bar-Cohen, EPS President
- Jie Xue, EPS Senior Past President
- Pat Thompson, EPS VP-Technology
- Grace O'Malley, EPS Member at Large
- C. Robert Kao, EPS Member at Large
- Sam Karikalan, EPS Member at Large
- Eric Perfecto, EPS Program Director – Awards Programs
- Alan Huffman, EPS Member at Large
- Yoichi Taira, EPS Member at Large
- Yan Liu, EPS Young Professional Representative

Technology Functional Team

- Pat Thompson, EPS VP-Technology
- Avi Bar-Cohen, EPS President
- Bill Chen, EPS Program Director – Industry Programs
- Eric Perfecto, EPS Program Director – Awards Programs
- Dave McCann, EPS Member at Large
- Raj Pulugurtha, EPS Technical Committee Chair

Finance Functional Team

- Pat Thompson, EPS VP-Technology
- Tom Reynolds, EPS VP-Finance
- Avi Bar-Cohen, EPS President

If you are interested in participating in one of the Functional Teams or having any comments for the teams, please send to Denise Manning (d.manning@ieee.org) or Avi Bar-Cohen (Avram.Bar-Cohen@raytheon.com).

Young Professionals Event

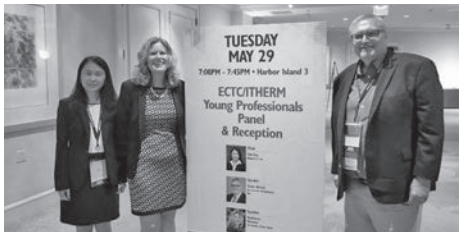
The IEEE Young Professional and Graduate Student Survey in 2016 showed that networking and education are top improvement opportunities among Young Professionals—likely due to being in the early stages of their career. There is significant room for satisfaction improvement in career services as well. Based on the survey results, EPS focuses on improving networking opportunity and providing more career services to YP members this year.

EPS is planning different types of YP meet up events like panel discussion, seminars, and receptions in conferences as well as local sessions. Recently, the 1st ECTC/ITherm Young Professionals Panel Discussion and Reception took place at San Diego on May 29, 2018. Yan Liu, the Electronic Packaging Society Young Professional representative hosted this event. There were 80 attendees joined this event, including ECTC/Therm young professional registrants and IEEE San Diego session young professionals. Two panelists Steve Bezuk (a senior director from Qualcomm Technologies Inc.) and Dr. Kathleen Kramer (IEEE Region 6 director and a professor from University of San Diego) shared their career development advices for young professionals based on their experiences and achievements in industry and academia. This event was very informative and well received. We would like to thank the funding support from IEEE Young Professional, as well as the great support from ECTC/ITherm and IEEE San Diego session.

In addition, EPS monthly eNews covers more resources for YPs, e.g. Webinars, short courses, upcoming conferences, most popular CPMT papers, and career services. Take career services for example, EPS provides new "Career" section on EPS website, including access to latest job listing on IEEE jobsite, access to IEEE Resume Lab, and access to IEEE Mentoring Program where EPS senior members registered as mentors.

EPS YP group also actively involves in IEEE YP activities. The IEEE YP rep groups have regular monthly conference calls to share the local YP events/activities with each other. This year, the IEEE YP Summit took place in Orlando Feb. 2018. The twenty-five YP representatives from different IEEE regions/sections/societies including EPS joined the inspiring meeting. Team discussed about skill gaps, diversity and inclusion, and career development for young professionals. They also brainstormed and shared the keys and strategies to engage young professionals, to benefit the YP initiatives in different regions/sections/societies.

Yan Liu
IEEE EPS Young Professional Representative



PUBLICATION NEWS

2017 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 200 published papers and represent the best, based on criteria including originality, significance, completeness and organization. The awards were presented at the 68th Electronic Components and Technology Conference (ECTC), June 2018.

Subscribers to this publication can access the papers on-line in IEEE Xplore at:

http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870

Components: Characterization and Modeling Category
"Monolithic Integration of a Micropin-fin Heat Sink in a 28 nm FPGA"
VOL. 7, ISSUE 10, OCTOBER 2017
Thomas Sarvey, Yang Zhang, Colman Cheung, Ravi Gutala, Arifur Rahman, Aravind Dasu, Muhannad S. Bakir

Abstract: Microfluidic cooling has been demonstrated as an effective means of cooling microelectronic circuits with a very low convective thermal resistance and potential for integration in close proximity to the area of heat generation. However, microfluidic cooling experiments to date have been limited to silicon with resistive heaters representing the heat generating circuitry. In this paper, a micropin-fin heat sink is etched into the back side of an Altera Stratix V field-programmable gate array (FPGA), built in a 28-nm CMOS process. Thermal and electrical measurements are made running a benchmark pulse compression algorithm on the FPGA. Deionized water is used as a coolant with flow rates ranging from 0.15 to 3.0 mL/s and inlet temperature ranging from 21 °C to 50 °C. An average junction-to-inlet thermal resistance of 0.07 °C/W is achieved.

URL: https://ieeexplore.ieee.org/document/8038817/

Electrical Performance of Integrated Systems Category
"Big-Data Tensor Recovery for High-Dimensional Uncertainty Quantification of Process Variations"
VOL. 7, ISSUE 5, MAY 2017
Zheng Zhang, Tsui-Wei Weng, Luca Daniel

Abstract: Fabrication process variations are a major source of yield degradation in the nanoscale design of integrated circuits (ICs), microelectromechanical systems (MEMSs), and photonic circuits. Stochastic spectral methods are a promising technique to quantify the uncertainties caused by process variations. Despite their superior efficiency over Monte Carlo for many design cases, stochastic spectral methods suffer from the curse of dimensionality, i.e., their computational cost grows very fast as the number of random parameters increases. In order to solve this challenging problem, this paper presents a high-dimensional uncertainty quantification algorithm from a big data perspective. Specifically, we show that the huge number of (e.g., 1.5×10^{27}) simulation samples in standard stochastic collocation can be reduced to a very small one (e.g., 500) by exploiting some hidden structures of a high-dimensional data array. This idea is formulated as a tensor recovery problem with sparse and low-rank constraints, and it is solved with an alternating minimization approach. The numerical results show that our approach can efficiently simulate some IC, MEMS, and photonic problems with over 50 independent random parameters, whereas the traditional algorithm can only deal with a small number of random parameters.

URL: https://ieeexplore.ieee.org/document/7775008/

AND

"High-Fidelity, High-Performance Computational Algorithms for Intra-System Electromagnetic Interference Analysis of IC and Electronics"
VOL. 7, ISSUE 5, MAY 2017
Zhen Peng, Yang Shao, Hong-Wei Gao, Shu Wang, Shen Lin

Abstract: Ever-increasing complexity in high-speed electronic devices and systems presents significant computational challenges in the numerical analysis in terms of desired accuracy, efficiency, and scalable parallelism. The objective of this paper is to investigate high-resolution, high-performance full-wave field solvers for scalable electromagnetic simulations of product-level integrated circuits (ICs) and electronics. The emphasis is placed on advancing parallel algorithms that are provably scalable facilitating a design-through-analysis paradigm, and enabling concurrent multiscale modeling and computation. The capability and the benefits of the algorithms are validated and illustrated through complex 3-D IC and electronics applications.

URL: https://ieeexplore.ieee.org/document/7817743/

5 Most Popular Articles According to May 2018 Usage Statistics

Manufacturing Considerations in the 3-D Printing of Fractal Antennas
Sung Yun Jun; Benito Sanz-Izquierdo; Edward A. Parker; David Bird; Alan McClelland
Publication Year: 2017, Page(s): 1891–1898

3-D Printed Metal-Pipe Rectangular Waveguides
Mario D'Auria; William J. Otter; Jonathan Hazell; Brendan T. W. Gillatt; Callum Long-Collins; Nick M. Ridler; Stepan Lucyszyn
Publication Year: 2015, Page(s): 1339–1349

Expected Failures in 3-D Technology and Related Failure Analysis Challenges
Ingrid De Wolf; Kristof Croes; Eric Beyne
Publication Year: 2018, Page(s): 711–718

Managing Electronics Part Changes in the Supply Chain
Michael Pecht; François Dagorn; Diganta Das
Publication Year: 2018, Page(s): 883–895

A Filtering Dual-Polarized Antenna Subarray Targeting for Base Stations in Millimeter-Wave 5G Wireless Communications
Hui Chu; Yong-Xin Guo
Publication Year: 2017, Page(s): 964–973

President's Column (*Continued from page 1*)

EPS you already enjoy the highest quality technical Conferences, Workshops, and Seminars in the business, as well as discounts on Conferences, free Webinars, low-price online subscriptions to the IEEE Transactions, awards and recognition, and opportunities for professional and personal relationships with your peers at the local level throughout the world. But even more importantly, membership and engagement in EPS puts you in the center of the packaging universe—allowing you to recognize emerging technologies in "real time," to interact with many of the packaging luminaries "up close and personally," to work with your packaging peers to drive the next generations of packaging S&T, and to define and steer your professional trajectory towards your personal and professional goals.

So, please take this opportunity to contact me directly (avram.bar-cohen@raytheon.com) to express an opinion or raise a question about our activities and to let me know of your interest join or start a new Technical Committee, volunteer to represent EPS on one of the IEEE-wide Initiatives, or to find out how to join our Board of Governors. It is only with all of you that we can successfully usher in the packaging technologies for future product generations and drive innovation in the microelectronic industry.

EPS Announces a New PhD Fellowship Award

The EPS Board of Governors voted unanimously to establish a PhD Fellowship award in the area of electronics packaging. Graduate Students—Here is what you need to know.

Description/Objective
To promote, recognize, and support PhD level study and research within the Electronics Packaging Society's field of interest.

Prize
A plaque and a single annual award of US$5,000, applicable towards the student's research.

Eligibility
Candidate must be an IEEE EPS member, at the time of nomination, and be pursuing a doctorate degree within the EPS field of interest on a full-time basis from an accredited graduate school or institution. The candidate must have studied with her/his advisor for at least 1 year, at the time of nomination, to be eligible.

A Student who received a Fellowship award from another IEEE Society, within the same year, or is a previous EPS Fellowship winner is ineligible.

Schedule
- On-Line application available by September 21
- Complete application packages are due by Jan 15
- Recipients will be notified by Mar 15
- Formal award presentations will take place at the IEEE EPS luncheon at ECTC at end of May.
- Monetary awards will be given by Jun 15 (or at ECTC)

Selection/Basis for Judging
Demonstration of his/her significant ability to perform independent research in the fields of electronic packaging and a proven history of academic excellence, as documented in:
- Nomination by an IEEE EPS Member. Only one nomination per member per year.
- Two-page (maximum) statement by the student describing his or her education and
- Research interests, accomplishments, and impact on the electronics package industry.
- Proof of contributions to the community may consist of open literature publications (preferred) such as papers, patents, books, and conference presentations and reports (available to the public).
- At least one letter of recommendation from someone familiar with the student's work
- Student resume

Award Committee
The committee will consists of the EPS Awards program Director and 4 representatives from industry and academia.

EPS Distinguished Lecturers are selected from among EPS Fellows, Award winners, and Society leaders, who are members of the technical community and experts in their field. They are available to present lectures and/or courses at EPS events—Chapters, Conferences, Workshops or Symposia; as well as IEEE Student Chapter events.

The EPS Distinguished Lecturer Program (DLP) aims at serving communities interested in the scientific, engineering, and production aspects of materials, component parts, modules, hybrids and micro-electronic systems for all electronic applications.

The Program strives to support EPS Chapters worldwide by helping them to invite leading researchers in their respective fields and IEEE Student Chapters to encourage students to pursue EPS related fields and to join the EPS society. The DLP talk is a major event in the life of the inviting Chapter.

EPS Distinguished Lecturers

Mudasir Ahmad
Cisco Systems, Inc. San Jose, CA USA
Topics: Internet of Things (IoT), Advanced Packaging, 2.5D, Heterogeneous Silicon Photonics, Advanced Reliability (Thermo-mechanical, Mechanical Shock), Numerical Modeling, Advanced Thermal Solutions, Stochastic Analysis, Bayesian Inference, Machine Learning, Artificial Intelligence

Muhannad Bakir
Georgia Institute of Technology, Atlanta, GA USA
Topics: Emerging interconnection architectures and technologies; heterogeneous system design and integration

Avram Bar-Cohen
University of Maryland, College Park, Maryland USA
Topics: Thermal packaging

Karlheinz Bock
Technische Universität, Dresden, Germany
Topics: Multifunctionality & heterosystemintegration & additive manufacturing (IoT, Industry 4.0, tactile internet…), packaging for mechanical, digital and power co-integration (automotive, machines, robots..), 2.5D and 3D electro-optical-RF interposer and board (high performance), heterointegration for flexible, bio, organic and large area electronics (open form factor)

Bill Bottoms
Third Millennium Test Solutions, Santa Clara, CA USA

Topics: Heterogeneous Integration, Semiconductor test technology, Emerging research materials, Packaging of electronic components and systems, the global network and its future requirements, the internet of things and Smart manufacturing

Chris Bower
X-Celeprint Inc. North Carolina, USA
Topics: Novel assembly methods, elastomer stamp micro-transfer-printing, heterogeneous integration, three-dimensional integration, manufacturing of micro-assembled displays and other large-format electronics.

Moises Cases
The Cases Group, LLC, Austin, Texas, U.S.A.
Topics: Signal and power distribution integrity for complex high-speed multiple board system designs; Modeling, simulation and verification of integrated circuits, electronic packages and system interconnect technologies; High-speed and low powers systems interconnect design methodology and tools; Digital system electrical designs, timings and integration; High-speed I/O architectures and designs; Service science management and engineering applied to engineering services

William T. Chen, Ph.D. (1/2015–1/2019)
ASE (U.S.) INC
Santa Clara, CA USA
Topics: Semiconductor and Electronics Industry Trends and Roadmap

Xuejun Fan
Lamar University, Beaumont TX USA
Topics: Design, modeling and reliability in micro-/nano- electronic packaging and microsystems

Paul D. Franzon
NC State University, Raleigh, NC USA
Topics: 3DIC and 3D Packaging Application,Design and CAD; I/O Macromodeling, including IBIS; High-Speed, Low Power Chip to Chip Communications

Philip Garrou
Microelectronic Consultants of North Carolina, Research Triangle Park, NC USA
Topics: Thin film technology; IC packaging and interconnect; Microelectronic materials; 3D-IC integration

R. Wayne Johnson
Tennessee Tech University, Cookeville, TN USA
Topics: Extreme Environment Electronics

Beth Keser
Intel, Neubiberg, Germany
Topics: Fan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; photoimageable liquid polymer films

John H. Lau
4ASM Pacific Technology, Hong Kong
Topics: Electronics and Photonics 2D and 3D packaging and manufacturing

Ning-Cheng Lee
Indium Corporation of America, Clinton, NY USA
Topics: Lead-free soldering including solderalloys, surface finishes, components, substrates, and other materials; Processes, reliability, failure modes, and troubleshooting; Advanced applications including packaging, and ultra-fine pitch applications

S. W. Ricky Lee
Hong Kong University of Science and Technology,
Clear Water Bay, Kowloon, Hong Kong
Topics: Solder Joint Reliability, 3D IC Integration, and LED Packaging

Johan Liu
Chalmers University of Technology, Gothenburg, Sweden
Topics: Micro and nano-electronic electrically conductive adhesives

Ravi Mahajan
Intel Corporation, Arizona, USA
Topics: Advanced Packaging Architectures, Assembly Processes and Thermal Management

James E. Morris
Portland State University, Portland, Oregon USA
Topics: Electrically conductive adhesives; Electronics packaging; Nanotechnologies

Kyung W. Paik
Korea Advanced Institute of Science & Technology,
Daejon, Korea
Topics: Electrically conductive adhesives (ACF, NCF, ACP, NC)

Mervi Paulasto-Kröckel
Aalto University, Helsinki, Finland
Topics: MEMS, electronics reliability, automotive components and packaging, implantable electronics, dissimilar materials & interfaces

Michael Pecht
University of Maryland, College Park, MD USA
Topics: Prognostics and reliability of electronic products and systems

Eric D. Perfecto
GLOBALFOUNDRIES, Hopewell Jct., NY USA
Topics: Fine pitch interconnect, chip to chip and chip to laminate connection, UBM and solder selection, chip package interaction and 2.5D fabrication

Karl J. Puttlitz
Puttlitz Engineering Consultancy, LLC, Wappingers Falls, NY USA
Topics: Flip Chip Issues/Technology; Area Array (1st & 2nd Level) Issues/Technology; Lead-free Issues/Technology

Dongkai Shangguan
National Center for Advanced Packaging Co., LTD., Wuxi, China
Topics: Materials, reliability, lead-free, microelectronics packaging, board assembly, electronics manufacturing

Nihal Sinnadurai
Suffolk, UK
Topics: Accelerated Ageing for Reliability Assurance -theory and practical methods—including HAST (my invention originally); The use of encapsulation and plastic packaging and reliability evaluation method; PCB & Hybrid technologies; Thermal management and design

Ephraim Suhir
Los Altos, CA USA
Topics: Accelerated life testing; Probabilistic physical design for reliability; Bonded assemblies; Thermal stress; Predictive modeling; Fiber optics structures: design for reliability; Dynamic response to shocks and vibrations

Rao Tummala
Georgia Institute of Technology, Atlanta, GA USA
Topics: Electronics Packaging

Walter Trybula
Trybula Foundation, Inc., Austin, TX USA
Topics: Emerging Technology, Advanced Lithography, Nanotechnology, Nano manufacturing, Nanomaterials, Environmental issues of Nanotechnology, Business Requirements of Nanotechnology

E. Jan Vardaman
TechSearch International, Inc., Austin, TX USA
Topics: International developments in semiconductor packaging, manufacturing and assembly; SiP: Business and technology Trends; drivers in advanced packaging; Flip chip and wafer level packaging

Paul Wesling
Saratoga, CA USA
Topics: Using Xplore, and Google Scholar to Mine IEEE's Online Repository of Technical Information; Origins of Silicon Valley and the EPS

C.P. Wong
Georgia Institute of Technology, Atlanta, GA, USA
Topics: Materials

Jie Xue
Cisco Systems, Inc, San Jose, CA, USA
Topics: Advanced Packaging for Networking Application; Impact of Internet of Everything (IoE) to Semiconductor Industry eco-system; High performance substrate technologies; Trends and challenges of Silicon Photonics for datacenter and networking applications

Kishio Yokouchi
Fujitsu Interconnect Technologies Ltd., Nagano City, Nagano, Japan
Topics: Thermal management technologies; Embedded passive component technologies; Chip to chip optical interconnection technologies

CONFERENCE NEWS

The 68th ECTC in San Diego—A Superb Edition Reaching New Heights

This year's IEEE Electronic Components and Technology Conference (ECTC) was held at the Sheraton Hotel in San Diego, California from May 29 to June 1. The conference brought together a total of 1,756 industry professionals, academics, and students in attendance from 28 countries, reaching a new record for ECTC, with more than 200 more attendees compared with previous highest attendance records.

In addition to general attendance, 2018 was the year for setting ECTC records. The Tuesday professional development courses drew a record 480 attendees, and overall sponsors and sponsorship broke the current record set last year in Orlando. The conference included 369 papers in 36 oral sessions and 5 interactive poster sessions. There were five special technical sessions and two special networking receptions with invited panelists. This year's Technology Corner Exhibit featured 106 exhibits—slightly more than last year in Orlando. This is a tribute to the quality of the conference and its attendees.

Preparations for the 68th ECTC started last October, when the professional volunteers serving in the technical committees reviewed 562 submitted abstracts. Ultimately, 66% of the submissions were accepted, leading to 359 presentations at the conference. This year, 48% of the submitted abstracts were from corporations, and 52% were from academia and research institutions. In a testimony to the diversity of the industry and the conference, abstracts were received from 27 countries.

The conference program came together at the Technical Program Committee's annual planning meeting near Dallas, Texas, on November 2 and 3, 2017. The subcommittee chairs and session chairs did an excellent job developing interesting sessions and communicating with their session authors, which enabled all the manuscripts to be publication-ready well before the start of the conference. ECTC again used, for the third year, the IEEE Computer Society Conference Publishing

The attendance at the 68th ECTC set a new record: 1,756!

68th ECTC offered 18 Professional Development Courses, reaching this year a record attendance of 480 participants.

Speaker Breakfast—Christopher Bower (in the back) providing guidelines to speakers and committee chairs. Session chairs and speakers making last minute preparations for their sessions.

Avi Bar-Cohen/IEEE EPS President (standing) co-chairs together with Chris Bailey, University of Greenwich, the panel session focused on IC Package Co-Design for Heterogeneous Integration.

Boon Chye Ooi (left), Senior Vice President, Global Operations at Broadcom Inc. receives a recognition award as a Keynote Speaker from Sam Karikalan (right) from Broadcom Inc., 68th ECTC General Chair.

Patrick Thompson/Texas Instruments at a great networking reception organized for students.

Services to receive and process manuscripts. As in previous years, the IEEE CrossCheck system was used to ensure that all of the ECTC manuscripts maintain a high level of original content. New for 2018 was implementing the review process performed by the session chairs for all the submitted manuscripts.

As usual, the first day of the conference, the Tuesday following Memorial Day, included professional development courses (PDCs), special sessions, and workshops. Once again, the conference had nine morning PDCs, running from 8 a.m. to noon, and nine afternoon PDCs, running from 1:15 p.m. to 5:15 p.m. The courses continue to serve as a great source for students and engineers to quickly get "up to speed" on a variety of topics, such as wafer-level and fan-out (FO) packaging, system-in-package (SiP), materials for electronics, and reliability. There were also some newcomers, such as photonic packaging, flexible hybrid electronics, and power electronics.

On Tuesday, ECTC also hosted the Heterogeneous Integration Roadmap Workshop, which took place from 8–5 p.m. The workshop was open to all ECTC attendees. The agenda was divided into four sessions plus a wrap-up session, and covered several topics relevant to heterogeneous integration, from applications such as high-performance computing, consumer, and industrial, to integration processes such as 3D integration and wafer-level packaging, as well as materials and simulation, supply chain, and testing. The wrap-up covered technical working group cross-collaboration, manuscript completions, SEMICON West plans, and 2018 events.

There were two special sessions and one evening plenary panel on Tuesday. All three represented breaks from tradition, as they focused on emerging technologies, and new applications, in a nod to the changing landscape inspired by heterogeneous integration at the system level.

At 10 a.m., Hong Yeo, of Georgia Institute of Technology, and C.S. Premachandran, GLOBALFOUNDRIES, co-chaired an emerging technologies session on "Soft Material-Enabled Electronics for Medicine, Healthcare, and Human-Machine Interfaces." Session speakers included Michael McAlpine, University of

2017 ECTC Best Paper Awards

1) Best Session Paper
"High Thermal Conductivity Mold Compounds for Advanced Packaging Applications" Makoto Shibuya & Luu Nguyen—Texas Instruments, Inc.

2) Best Interactive Presentation Paper
"Development of Die Attachment Technology for Power IC Module by Introducing Indium into Sintered Nano-silver Joint," ChunAn Yang and C. Robert Kao—National Taiwan University; and Hiroshi Nishikawa—Osaka University

3) Outstanding Session Paper
"Warpage Modeling and Characterization of the Visco-elastic Relaxation for Cured Molding Process in Fan-Out Packages," Shu-Shen Yeh, Po-Yao Lin, Kuang-Chun Lee, Jin-Hua Wang, Wen-Yi Lin, Ming-Chih Yew, Po-Chen Lai, Shyue-Ter Leu, and Shin-Puu Jeng—Taiwan Semiconductor Manufacturing Company, Ltd.

4) Outstanding Interactive Presentation Paper
"Via-in-Trench: A Revolutionary Panel-based Package RDL Configuration capable of 200-450 IO/mm/layer, an Innovation for More-Than-Moore System Integration," Fuhan Liu, Chandrasekharan Nair, Hao Lu, Rui Zhang, Hang Chen, Venky Sundaram, and Rao R. Tummala—Georgia Institute of Technology; Atsushi Kubo and Tomoyuki Ando—Tokyo Ohka Kogyi; Kwon Sang Lee—Disco Corporation

5) Intel Best Student Paper
"Latency, Bandwidth and Power Benefits of the Super CHIPS Integration Scheme," Siva Chandra Jangam, Saptadeep Pal, Adeel Bajwa, Sudhakar Pamarti, Puneet Gupta, and Subramanian Iyer—University of California, Los Angeles

6) Texas Instruments Outstanding Student Interactive Presentation Paper Award
"Development of Die Attachment Technology for Power IC Module by Introducing Indium into Sintered Nano-Silver Joint" Chun An Yang and C. Robert Kao—National Taiwan University; Hiroshi Nishikawa—Osaka University

Minnesota; Todd Coleman, University of California, San Diego; Aadeel Akhtar, Psyonic; and Rooz Ghaffari, Epicore Biosystems. The speakers offered expertise on advancements in soft materials, and how they will impact our lives in the future.

The afternoon special session, Frontiers in Assembly, chaired by Florian Herrault, HRL Laboratories, focused on emerging device assembly methods and applications to accommodate the needs of heterogeneous integration at the system level. Speakers Jeff Demmin, DARPA; Stefan Behler, Besi; Matthew Meitl, X-Celeprint; Doris Tang, PlayNitride; and Val Marinov, Uniquarta discussed the latest advancements in assembly technologies for chip packaging, microLED displays, and ultra-thin chip placement for flexible electronic applications.

On Tuesday evening at 7:45 p.m., Avi Bar-Cohen, IEEE EPS President; and Chris Bailey, University of Greenwich co-chaired the panel session titled "IC/Package Co-Design for Heterogeneous Systems." Panelists represented different segments of the heterogeneous integration supply chain, and included Harrison Chang, Advanced Semiconductor Engineering, Inc.; John Parry, Mentor Graphics; Yong Liu, ON Semiconductor; Xuejun Fan, Lamar University; Madhavan Swaminathan, Georgia Institute of Technology; and Andrew Kahng, University of California, San Diego. Panelists explained the challenges of integrating different components made up of different materials with different properties. The key takeaway from the session was the importance of understanding the interaction between the chip, package, and board.

Let's not forget the networking opportunities that took place prior to Tuesday's plenary session. Again this year, Texas Instruments sponsored the ECTC Student Reception on Tuesday at 5 p.m. A steady stream of student attendees took advantage of the opportunity to mingle and network with industry leaders, in hopes of getting guidance for their job search.

From 6–7 p.m., speakers and session chairs gathered in Grand Ballroom B for the annual General Chair's speaker reception. These receptions provided a great start to the conference, and helped prepare everyone for the following three days filled with technical presentations and networking opportunities.

Each day at ECTC begins with the Speakers Breakfast, in which the presenters and session chairs meet and handle the preparatory work for their respective sessions. The PDC Chair, Kitty Pearsall, provided instructions to the PDC instructors and proctors on Tuesday morning, and Christopher Bower, the Program Chair, hosted these breakfast meetings, and provided instructions and guidance to the speakers and session chairs.

Wednesday marked the start of the technical sessions, with six sessions running in parallel, both in the morning and in the afternoon each day. Wednesday morning started with large crowds in numerous sessions, including "Flexible Electronics, Substrate for High Frequency Applications," "Advances in Wafer and Panel Level Fan-Out Packaging," "3D Design, Assembly and Additive Manufacturing," and "Automotive and Harsh Environment Reliability," "Antenna-in-Package for RF and mm-Wave Systems," and "Warpage and Moisture Characterization." Afternoon topics covered "Low-Temperature Metallic Interconnection Technologies," "Fan-Out Packaging Applications and Architectures," "Flip-Chip Manufacturing Challenges," "Innovative Design, Modeling and Predictions for Reliability," "Emerging Packaging Technologies for 5G and Advanced Computing," and "Sintering Pastes, Transient Liquid Phase and Direct Bonding." The fan-out sessions drew the largest crowds bar far, with attendees lining up outside the door to get a glimpse of the presentations. This demonstrates the importance of this advanced packaging platform. Just like last year, all oral session paper ratings were done only through the ECTC mobile app.

Boon Chye Ooi, Senior Vice President, Global Operations at Broadcom Inc., presented this year's keynote speech at the ECTC luncheon on Wednesday. His presentation, titled "Packaging Advancement to Enable Artificial Intelligence, Autonomous Cars and Wearables in the Near Future: Cost and Implications" focused on what is needed from the packaging community to enable these rapidly growing markets by 2022.

Specifically, Ooi stressed the growing need for 5G technologies to handle all the data traffic that these applications will require. Noting that while 5G will come sooner than we expect, the U.S. will not be the first implement it, due to a lack of infrastructure.

The 68th ECTC had 106 exhibitor booths at the Technology Corner.

Cristina Amon from University of Toronto and iTherm representative (standing) moderating the panel together with Tanja Braun from Fraunhofer Institute for Reliability and Microintegration (IZM), ECTC representative (far right) the Women's Panel. The panelists seated are (from left to right), Kawthan (Kat) Kasim from Boeing Research and Technology, Jayathi Murthy, UCLA Dean of Engineering and Li Ming, R&D Director with ASM Pacific Technology.

68th ECTC had five Interactive Presentation (IP) sessions with a total of 107 presentations, including 20 in the Student IP Session.

Kemal Aygun/Intel (standing) moderating the Plenary Session on Artificial Intelligence.

IC packaging technology will be the key enabler, particularly 2.5D and 3D technologies. Ooi concluded with a call-to-action to enable the supply chain. Assembly yield management needs to be upgraded to fab level to support Big Data. Development of µbump probe and test technologies are needed. Substrates for low-loss mmWave channels on large packages are needed. Low-cost thermal solutions to reduce end-customers' system costs need to be developed. Most importantly, multiple supplier sources for silicon content, packaging raw materials, and substrates and assembly are needed to maintain business continuity.

Awards for best and outstanding papers from last year's (67th) ECTC, both in oral presentation sessions and interactive sessions, were presented by the ECTC 2018 Program Chair, Chris Bower, at this luncheon. Also presented was the Intel Best Student Paper Award for ECTC 2017.

As is customary at the Sheraton venue in San Diego, The Technology Corner exhibit area was located in a marquee tent with a beautiful view of the bay. Attendees didn't seem to mind the opportunity for a short walk outdoors to visit 106 exhibitors. The exhibits enjoyed a steady stream of attendees, with very busy bursts of activity during the breaks from the technical sessions. The exhibitors hosted a reception on Wednesday evening that provided more opportunities for technical and business exchanges with prospective customers and collaborators. The Interactive Presentation sessions were located in the Nautilus Foyer, outside session rooms, and had a high number of patrons studying the presented results.

ECTC and ITHERM teamed up this year to host the Women's Panel and Reception, which focused on the topic, "How to Enhance Women's Participation in Engineering Around the Globe," chaired by Cristina Amon, University of Toronto, and Tanja Braun, Fraunhofer Institute for Reliability and Microintegration (IZM). This year's distinguished speakers included Kawthar (Kat) Kasim, Boeing Research and Technology; Jayathi Murthy, UCLA Dean of Engineering; and Li Ming, R&D Director, Enabling Technologies at ASM Pacific Technology, Hong Kong.


The Gala Reception was a great time for socializing by the beautiful shores of San Diego after a day full of technical meetings and brainstorming.

Before the panel got underway, Jan Vardaman, Techsearch International, took a few moments to announce that the IEEE Frances B. Hugle Engineering Scholarship, which her company spearheaded in 2013, is fully funded, and will begin awarding annual scholarships this year. She thanked all the companies who have made donations over the years, and showed a short video from the family of Frances. B. Hugle, who also extended their appreciation.

The panelists then discussed their respective career paths, and the challenges women face in the engineering field, as well as the advantages of being a woman in the field. It was interesting to hear

The 2018 ECTC Executive Committee members from left to right: Nancy Stoffel/GE, Assistant Program Chair, Christopher Bower/X-Celeprint Inc., Program Chair, Mark Poliks/Binghamton University, Vice General Chair, and Sam Karikalan/Broadcom Inc., General Chair.

The 68th ECTC Event Management team.

the differing experiences and perspectives, as all the women on the panel were at different stages of their careers, and as a result, had different stories to tell. The discussion ended with a Q & A session with the audience, and was followed by an in-room reception where discussions and networking continued.

While the panel didn't really address how we can attract more women to the field, attendees—both men and women—came away feeling they had learned something.

The Wednesday evening Plenary Session titled "Artificial Intelligence and Its Impact on System Design" was chaired by Kemal Aygun from Intel Corporation, and included presentations from leading foundries and integrated device manufacturers, as well as representatives from academia and software. Speakers included Igor Arsovski, GLOBALFOUNDRIES; Kailash Gopalakrishnan, IBM Corporation; Andrew Putnam, Microsoft Corporation; Madhavan Swaminathan, Georgia Institute of Technology; and Dan Oh, Samsung. The panelists discussed the computing, memory, and power challenges that come from AI, deep learning, and high-performance computing, and the best ways to solve them from a system architecture perspective.

The Thursday morning sessions were well-attended, and covered topics ranging from "Fan-Out and Interposer Interconnections" to "Technology Advances in Nano, Biochemical, Thermal and Flexible Applications" to "Silicon Photonics." Thursday afternoon included sessions on "Interconnect Reliability," "MEMS, Sensor, IoT and Flex," and "Optical Module Integration."

The IEEE EPS Society President, Avi Bar-Cohen, presided over the luncheon on Thursday and presented the EPS Society Awards. The recipients were presented with a plaque and received warm applause from the audience.

The ECTC 2018 Technical Program Committee meeting was held on Thursday at 5:30 p.m. Nancy Stoffel, who will serve as the Program Chair for ECTC 2019, chaired this meeting, and presented the statistics of the 68th ECTC and the timeline for the run-up to the 69th ECTC, which will be held in Las Vegas next year. The EPS Representative on the ECTC Executive Committee, C.P. Wong, introduced Rozalia Beica of DowDuPont as the Assistant Program Chair of the 69th ECTC. This meeting also allowed the ECTC technical program subcommittees to connect with potential new members of their committees.

As always, the Gala Reception on Thursday evening was the highlight of the week for the conference attendees, exhibitors, sponsors, and their guests. It was a time to celebrate the success of the ECTC by socializing and enjoying the excellent food and beverages that were supported by the Gala Reception Gold and Silver sponsors.

Following the Gala Reception, the 2018 IEEE EPS Seminar on "High Density Packaging Technologies in the Era of Big Data" got underway, chaired by Yasumitsu Orii, Nagase, Japan; Shigenori Aoki, Fujitsu. Speakers included Shunichi Kikuchi, Fujitsu; Spike Narayan, IBM Research; Urmi Ray, JCET STATS ChipPAC; Masato Tanaka, Shinko; and Toshihisa Nonaka, Hitachi Chemical. The panelists shared many insights on this evolving segment, bringing different perspectives on the needs and challenges created by Big Data and enabling packaging technologies and materials with a focus on high-density requirements.

Friday sessions continued with more traditional advanced packaging topics, fan-out and TSV-related sessions, as well as a focus on power electronics. The morning sessions ranged from "Fabrication and Characterization of TSV" to "Automotive and Power Electronics" to "Modeling of Power Electronics." The afternoon included sessions on "Advanced Wirebond and Interconnect Technologies," "Next-Generation Materials and Processes for Through Vias and 3D Interconnects," and "Power Delivery Solutions for Components and Systems." At lunch on Friday, everyone had the usual fun at the famous ECTC raffle, where Tom Reynolds, the ECTC Treasurer, kept everyone laughing and longing to hear the numbers on their ticket called.

Overall, the 68th ECTC was the best year yet in terms of its record attendance, strong exhibitor presence, record sponsorship, and number of high-quality technical presentations and submitted abstracts. The ECTC Executive Committee sincerely thanks all the attendees, exhibitors, and conference sponsors for their support as well as all the committee members and chairs who are volunteering their time to help organize the sessions and make ECTC such a success every year. Special thanks also to our event management.

The 69th ECTC will be held at The Cosmopolitan, Las Vegas, Nevada, USA, May 28–31, 2019. Mark Poliks from Binghamton University will be the General Chair of this conference. The Call for Papers and PDC Proposals will be available at www.ectc.net, and the abstract submission will close on October 8, 2018. So get those abstracts ready and submit them as soon as abstract submission opens online.

We are looking forward to see you all in Las Vegas in 2019!

Rozalia Beica
Assistant Program Chair, IEEE ECTC 2019

Article on EPTC on the occasion of its 20th Anniversary

This December 4–7, 2018, we celebrate the 20th Anniversary of the Electronics Packaging Technology Conference (EPTC), our Society's flagship conference in the Asia-Pacific region, which will be held at Resorts World Sentosa, Singapore. To celebrate this historic milestone, the EPS Board of Governors (BoG) will be holding its next meeting in conjunction with EPTC 2018. Although a BoG delegation has attended EPTC in the past, this meeting would be making history as it will be the first-ever BoG meeting outside the USA! It is a concrete demonstration of the internationalisation of our Society and the exponential growth of electronics packaging in Asia. To commemorate this event, we shall give a brief account of the history of EPTC.

The idea for EPTC was mooted by the IEEE Singapore Joint Rel/CPMT/ED Chapter towards the end of 1995. It was felt that there was no Society-sponsored, ECTC-like electronics packaging conference in Asia at that time. It was thought that the great distance between USA and Asia and the expenses involved were preventing many packaging engineers from Asia to attend ECTC. It was then decided to organise an international electronics packaging conference to provide a platform for packaging engineers from all over the world but especially in the Asian region, to exchange ideas and share experiences. The inaugural EPTC was convened on 8–10 October 1997 under the General Chairmanship of Professor Andrew Tay of the National University of Singapore with wide support from universities, research institutes and electronics companies in Singapore. In 2006, in order to steer the long term development of EPTC, the EPTC Board was formed with Prof Andrew as its inaugural Chairman.

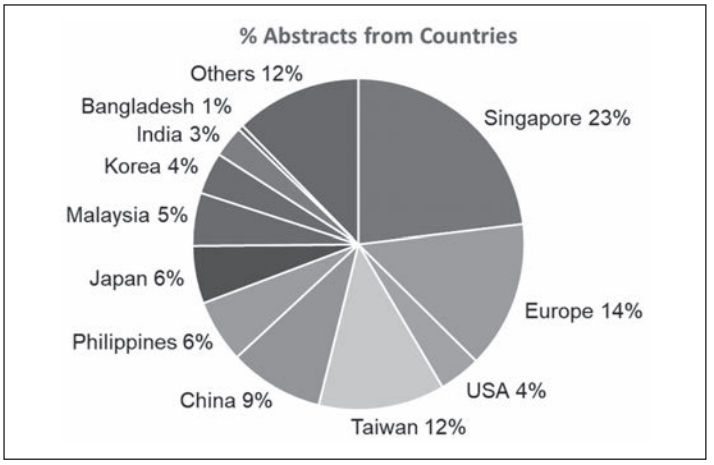
EPTC is usually a 3-day conference comprising Professional Development Courses and a Panel on the first day, and keynotes, invited presentations and technical sessions on the remaining two days. The conference is also well supported by a table-top exhibition and sponsorships by companies from all over the world. EPTC has been modelled after ECTC in scope and structure. It has the following 10 categories covering the whole range of topics in electronics packaging:

1) Advanced Packaging
2) TSV/Wafer Level Packaging
3) Interconnection Technologies
4) Emerging Technologies
5) Materials and Processing
6) Equipment and Process Automation
7) Electrical Modeling & Characterization
8) Mechanical Modeling & Simulations
9) Thermal Characterization & Cooling Solutions
10) Quality, Reliability and Failure Analysis

Abstracts of papers are reviewed by 10 Technical Committees which are formed from about 120 international experts.

In 2003, our Society's leadership conceived the idea of establishing "flagship" conferences in North America, Asia and Europe. By 2003, after 53 years, ECTC has been well established as the premier electronics packaging conference in the world and our Society's flagship conference in North America. By 2003, a few packaging conferences have sprung up in Asia but EPTC was adopted as our Society's flagship conference in Asia due to several reasons: the topical coverage is good; the conference proceedings are of high quality; Singapore is able to draw participants from all over Asia (good transportation and facilities); and the standard language there is English (the interchange language chosen by IEEE). In 2006, a new flagship conference was established in Europe, namely the Electronics System-Integration Technology Conferences (ESTC). In fact, the name of the new conference was purposefully chosen so that the triumvirate relationship between the 3 flagship conferences would be evident from their acronyms ECTC, EPTC and ESTC.

The inaugural conference had only 51 papers and was attended by about 110 conferees but this has grown more than 3 times to 163 papers and 362 conferees in 2017. In 2017, there were 195 abstracts which were received from 24 countries making it a truly international conference indeed. 50% of the abstracts were from industry, 20% from research institutes and 30% from academia making the technical program well-balanced. What is also of great significance is the percentage of abstracts submitted from various main countries as illustrated in the figure below which shows that there is very wide and good contributions from Asian countries as well as good contributions from Europe and USA.



One of the feature highlights of EPTC is the conference banquet cum social event which is usually held in some iconic venues or feature some interesting locations in Singapore. These include the Night Safari (tour through the Singapore Zoo at night), the Malay Heritage Centre, Seafood Centre, new Marina Bay area, Gardens by the Bay, boat tour down historic Singapore River, ride on the Singapore Flyer (giant ferris wheel) and Harbour cruise cum dinner on board ancient Chinese sailing ship. Some of these are shown in the photographs below:

Harbour cruise with buffet dinner on board, EPTC2008.

EPTC2017 Organising Committee in banquet at Marina Bay showing iconic skyline.

This year, the 20th EPTC will be held at the Resorts World Sentosa (RWS) which has many attractions including Universal studios, a casino, an ocean gallery and water theme park as shown below:

Universal Studios.

Casino, Resorts World Sentosa.

Ocean Gallery—Venue of Conference Banquet EPTC 2018.

As a tribute to the EPTC leaders who have come forward to take on the challenge of developing an excellent electronics packaging conference in Region 10, we would like to list and acknowledge the following General Chairs for the 20 EPTCs to date:

EPTC	Year	Genera Chair	Affiliation
1st	1997	Prof Andrew Tay	National University of Singapore
2nd	1998	Prof Andrew Tay	National University of Singapore
3rd	2000	Dr Thiam Beng Lim	Institute of Microelectronics
4th	2002	Mr Charles Lee	Infineon Technology
5th	2003	Dr Mahadevan Iyer	Institute of Microelectronics
6th	2004	Prof Kok Chuan Toh	Nanyang Technological Institute
7th	2005	Mr Yew Cheong Mui	Advanced Micro Devices
8th	2006	Prof John Pang	Nanyang Technological Institute
9th	2007	Dr Kripesh Vaidyanathan	Institute of Microelectronics
10th	2008	Dr Tong Yan Tee	Amkor Technology
11th	2009	Mr James How	Motorola
12th	2010	Dr Yoon Seung Yoon	Stats-Chippac
13th	2011	Dr Albert Lu	Singapore Institute of Manufacturing Technoogy
14th	2012	Mr Navas Khan	Freescale
15th	2013	Mr Ashok Anand	Advanced Micro Devices
16th	2014	Dr Alfred Yeo	Infineon Technology
17th	2015	Dr Chin Hui Choong	Micron Semiconductor
18th	2016	Mr Ranjan Rajoo	Globalfoundries
19th	2017	Dr Xueren Zhang	Xilinx
20th	2018	Mr Vempati Srinivasa Rao	Institute of Microelectronics

Andrew Tay
EPS Program Director – Region 10

EPTC 2018

20th Electronics Packaging Technology Conference
4th – 7th Dec 2018, Resorts World Sentosa, Singapore

IEEE EPS Flagship Conference
In Asia Pacific Region

FINAL CALL FOR PAPERS

ABOUT EPTC

The 20th Electronics Packaging Technology Conference (EPTC 2018) is an International event organized by the IEEE RS/EPS /EDS Singapore Chapter and co-sponsored by IEEE Electronics Packaging Society (EPS). EPTC 2018 will feature keynotes, technical sessions, short courses, forums, an exhibition, social and networking activities. It aims to provide a good coverage of technology developments in all areas of electronics packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts. Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in the Asia-Pacific and is well attended by experts in all aspects of packaging technology from all over the world. EPTC is the flagship conference of IEEE EPS in Region 10. **This year, to commemorate the 20th anniversary of EPTC, one extra day of special technical presentations will be added to the conference program.**

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new developments in the following categories:

- **Advanced Packaging:** Advanced Flip-chip, 2.5D & 3D, PoP, embedded passives & actives on substrates, System in Packaging, embedded chip packaging technologies, Panel level packaging, RF, Microwave & Millimeter-wave, Power and Rugged Electronics Packaging etc.
- **TSV/Wafer Level Packaging:** Wafer level packaging (Fan in/Fan out), embedded chip packaging, 2.5D/3D integration, TSV, Silicon & Glass interposer, RDL, bumping technologies, etc.
- **Interconnection Technologies:** Au/Ag/Cu/Al Wire-bond / Wedge bond technology, Flip-chip & Cu pillar, solder alternatives (ICP, ACP, ACF, NCP, ICA), Cu to Cu, Wafer level bonding & die attachment (Pb-free) etc.
- **Emerging Technologies:** Packaging technologies for MEMS, biomedical, optoelectronics, Internet of things, photo voltaic, printed electronics, wearable electronics, Photonics, LED, etc.
- **Materials and Processing:** advanced materials such 3D materials, photoresist, polymer dielectrics, solder materials, die attach, underfill, Substrates, Lead-frames, PCB etc for advanced packaging, and assembly processes using advanced materials
- **Equipment and Process Development & Automation:** processes development, equipment automation, process and equipment hardware improvements, data analytics, in-situ metrology.
- **Electrical Simulation & Characterization:** Power plane modeling, signal integrity analysis by simulations and characterization. 2D/2.5D/3D package level high-speed signal design, characterization and test methodologies.
- **Mechanical Simulation & Characterization:** Thermo-mechanical, moisture, fracture, fatigue, vibration, Shock and drop impact modeling, chip-package interaction, etc.
- **Thermal Characterization & Cooling Solutions:** Thermal modeling and simulation, component, system and product level thermal management and characterization
- **Quality, Reliability & Failure Analysis:** Component, board, system and product level reliability assessment, Interfacial adhesion, accelerated testing, failure characterization, etc.

Others are also welcomed, e.g. Market trends, Environmental, legislation, Patents, Education, Cost Analysis

IMPORTANT DATES

Online abstract submission start	**30th Mar 2018**
Closing of abstract submission	**Extended to 27th July 2018**
Notification of acceptance	**15th August 2018**
Submission of manuscript	**15th September 2018**

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited which describe original and unpublished work. The abstract should be at least 500-750 words long and clearly state the purpose, methodology, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications should be included in the abstract as well. Authors can choose between oral or interactive presentation. Accepted papers that are registered and presented (oral & interactive) at the conference will qualify for publication in IEEE Xplore.

All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by 27th July 2018. Authors must include their affiliation, mailing address, telephone number and email address. Authors will be notified of paper acceptance and publication instruction by 15th August 2018. The final manuscript for publication in the conference proceedings is due by 15th September 2018. The conference proceedings is an official IEEE publication and accepted papers will be available in IEEE Xplore.

BEST PAPER AWARDS

Awards will be given to the best oral papers from Academia, Industry and Students, and to the best interactive papers from Student and Open categories. More details can be found at http://www.eptc-ieee.net

CALL FOR SHORT COURSES

The conference program includes short courses which will be conducted by leading experts in the field. Details will be updated in the conference website. Proposals for short courses can be submitted to pdc@eptc-ieee.net

CALL FOR EXHIBITION / SPONSORSHIP PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment and services to the microelectronics packaging and assembly industries, will be held during the conference. For details, please e-mail to exhibition@eptc-ieee.net and sponsorship@eptc-ieee.net.

EPTC 2018: website: **http://www.eptc-ieee.net** Email: secretariat@eptc-ieee.net Join us on: **Linkedin [EPTC OC]**

Organized by
IEEE Reliability/EPS/ED Singapore Chapter

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IEEE ELECTRONICS PACKAGING SOCIETY

EPTC 2018

20th Electronics Packaging Technology Conference
4th – 7th Dec 2018, Resorts World Sentosa, Singapore

IEEE EPS Flagship Conference
In Asia Pacific Region

PROGRAM HIGHLIGHTS

(SUBJECT TO CHANGE)

PROFESSIONAL DEVELOPMENT COURSES

- Introduction to fan-out wafer-level packaging, Dr. Beth Keser – Intel Corporation.
- Understanding flip chip technology and its applications, Dr. Eric Perfecto – Globalfoundries.
- Advanced integrated circuit design for reliability, Dr. Richard Rao – Microsemi Corp, USA.
- Introduction to 3D interconnect and packaging technologies, Prof. Sarah Kim – Seoul National University of Science and Technology.
- And more

SPECIAL 20TH ANNIVERSARY PROGRAM

Keynotes and Invited Presentations by experts:

- Ivor Barber, VP, AMD, USA.
- David McCann, VP, Globalfoundries, USA.
- Dr Avram Bar Cohen, Raytheon Corporation, USA.
- Dr. Stevan G Hunter, On Semiconductor, USA.
- Dr. Bill Chen, Fellow, ASE Group, USA.
- Prof. Robert Kao, National Taiwan University.
- Prof. Jeffrey Suhling, Auburn University, USA.
- Dr. Evelyn Napetschnig, Infineon Technologies.
- Mr. Sam Karikalan, Broadcom Inc., USA.
- Mr. Paul Werbaneth, Intevac.
- And many more

VIBRANT VENUE – RESORTS WORLD SENTOSA

World-class venue with attractions including Universal Studios, RWS Casino and theme parks.

BOG MEETING

First time ever IEEE EPS Board Of Governors meeting held outside USA. Many packaging experts who are members of BoG will be participating in the conference program.

CONFERENCE BANQUET IN S.E.A. AQUARIUM

Fine dining at a stunning and memorable backdrop with marine animals sighted through a panoramic window to the ocean.

PARTIAL LIST OF ABSTRACTS RECEIVED TO DATE

1. Guided Interconnect – The Next-Generation Flex Circuits for High-Performance System Design, J. Kong et al, Intel Corporation.
2. Study of the die position accuracy in the fabrication process of a die first type FO-PLP, K. Nishido et al, Hitachi Chemical Co. Ltd., Japan.
3. Novel concept of an in-situ test system for the thermal-mechanical reliability evaluation of electronic joints. R. Metasch et al, Fraunhofer Institute, Germany.
4. High Frequency Power Integrity Design Sensitivity to Package Design Rules, S. Shekhar et al, Intel Corporation.
5. Within-die coplanarity improvement strategies for electro-plated Cu pillars, G. Graham et al, Lam Research, USA.
6. One Micron Damascene Redistribution for Fan-Out Wafer Level Packaging using a Photosensitive Dielectric Material, R Hsieh et al, Veeco, IMEC & JSR MICRO NV, Belgium.
7. Develop Smart Wire Bonding Processes for Smart Factories, I. Qin et al, Kulicke & Soffa Inc, USA.
8. Critical Factors impacting strength of UBM in smaller and denser bumps and methodologies for optimization, A Ramasamy et al, Xilinx Singapore, USA, Taiwan.
9. Innovative Packaging Solutions of 3D System in Package with Antenna Integration for IoT and 5G Application, M. Tsai, SPIL, Taiwan.
10. Effective Electromagnetic shielding method for A new fan-out package utilizing Cu Substrate, S. Kim et al, Hanyang University, South Korea.
11. Impact of lifetime and mechanical behaviors on TIM performance on high-end processor, R. Gamal et al, Xilinx USA.
12. Design and optimization of the 10Tbps optical transmission system, H. He et al, Institute of Microelectronics of Chinese Academy of Sciences, China.
13. Analysis of Low Profile Ferrite Material Based Planar Shell Core Inductor, Z. Zeeshan et al, Infineon, Germany.
14. A New Failure Mechanism of Inter Layer Dielectric Crack, H. Liu et al, NXP, China.
15. Thermal Performance Characterization and Enhancement for High Power Package Development, B. S. Chen et al, Advanced Semiconductor Engineering, Inc, Taiwan.
16. Temporary Bonding Material Study for Room Temperature Mechanical Debonding with eWLB Wafer Application, S. Masuda et al, FUJIFILM Corporation, Japan.
17. Ceramic Interposers for Ultra-High Density Packaging and 3D Circuit Integration, A Adibi et al, École de Technologie Supérieure, Canada.
18. High bonding strength of silver sintered joints on non-precious metal surfaces by pressure sintering under air atmosphere using micro-silver sinter paste"; L. M. Chew et al, Heraeus Deutschland GmbH & Co. KG, Germany.
19. Design Optimization of Through-Silicon Vias for Substrate-Integrated Waveguides embedded in High-Resistive Silicon Interposer, M Wietstruck et al, IHP, Germany and Sabanci University, Turkey.
20. Millimeter-Wave Antenna in Package (AiP) Using Unbalanced Substrate with and without Solder Mask, K. T. Chen et al, SPIL, Taiwan.
21. Highly Stretchable, Durable, and Printable Textile Conductor, W. J. Lee et al, Seoul National University of Science and Technology, South Korea.

22. Failure Analysis on Mobile Phone Batteries and Accessories, Z Jin, Osaka University, Japan, City University of Hong Kong.
23. Investigations of Silver Sintered Interconnections on 3-Dimensional Ceramics with Plasma Based Additive Copper Metallizations, A. Hensel et al, Friedrich-Alexander University, Erlangen,-Nürnberg, Germany.
24. Characterization of interfacial intermetallic compounds in gold wire bonding with copper pad, B. Wang et al, Huawei.
25. Investigation on solder void formation mechanism after high temperatures stress by 3D CT scan and EDX analysis, C. Y. Lai et al, Infineon, Malaysia.
26. Via Interconnections for Half-Inch Sized Package Fabricated by Minimal Fab, National Institute of Advanced Industrial Science and Technology (AIST), Japan.
27. High Density Bumpless Interconnections Using Novel Wafer Bonding Approach For 3D IC Heterogeneous Integration Applications, K. Hemanth et al, IIT Hyderabad, India.
28. "3rd Level" Solder Joint Reliability Investigations for Transfer of Consumer Electronics in Automotive Use, R. Dudek et al, Fraunhofer ENAS, Germany.
29. Post processing of a SiN-based photonic stack above a CMOS imager sensor, N Pham et al, IMEC, Belgium.
30. Simulation And Electrical Characterization Of A Novel 2D-Printed Incontinence Sensor With Conductive Polymer PEDOT:PSS For Medical Applications, M. Baeuscher et al, Fraunhofer Institute for Reliability and Microintegration Berlin, Germany.
31. Challenges and Approaches of 2.5D high density Flip chip interconnect on through mold interposer, S. Lim et al, Institute of Microelectronics, Singapore.
32. Development of SiC Chip Based Power Package for High Power and High Performance Application, G.Y. Tang et al, Institute of Microelectronic, Singapore.
33. Laser Separation of Dissimilar Substrates Using Water Washable Materials , J Moore et al, Daetec LLC, USA.
34. Solder Mask Crack Investigation and Optimization for Larger FCBGA Package, V Lin et al, SPIL, Taiwan.
35. Wideband slot array antenna for 1 THz band imaging device, K Tsugami et al, Kyushu University, Japan.
36. Hybrid Cu-SiN and Cu-SiOx Direct Bonding of 200 MM CMOS Wafers With Five Metal Levels: Morphological, Electrical and Reliability Characterization, C Cavaco et al, IMEC, Belgium.
37. Pluggable Silicon Photonics MEMS Switch Package for Data Centre, H.Y. Hwang,Tyndall National Institute, Ireland.
38. Simulation Approach to Predict Warpage based on Resin Curing Behavior during Substrate Manufacturing Process, M Furuyama et al, Fujitsu Laboratories Ltd, Japan.
39. Si-based Hybrid Microfluidic Cooling for Server Processor of Data Centre Y. Han, Institute of Microelectronics, A*STAR, Singapore.
40. Low Transmission Loss Polyimides Substrates: A Novel Alternative to Liquid crystal polymers, T. Tasaki, Arakwa Chemical Industries Ltd., Japan.

EPS Board of Governors Meeting June 2, 2018

30TH ANNUAL

ELECTRONICS PACKAGING SYMPOSIUM

SMALL SYSTEMS INTEGRATION

SEPTEMBER 18-19, 2018 • BINGHAMTON, NY

The 30th annual Binghamton University and GE Electronics Packaging Symposium, the premier electronics manufacturing conference in the Northeast, features more than 40 invited technical presentations by academic, industry, and government leaders, influencers, and decision makers. The program includes an IEEE Electronics Packaging Society-sponsored workshop on Heterogeneous Integration, a student poster session and exhibits.

Session topics will include:

- 2.5/3D packaging
- 5G needs in packaging
- Automotive and harsh environments
- Bioelectronics
- Flexible and additive electronics
- Flexible electronics for medical and wearable applications
- Materials for packaging and energy storage
- MEMS
- Photonics
- Power electronics
- Sensors and embedded electronics/ IoT
- Thermal challenges

SIP IEEC Integrated Electronics Engineering Center Binghamton University

IEEE ELECTRONICS PACKAGING SOCIETY

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1 6-foot table (2 days of exhibit time)

Company name listed in program and on website

IEEE ESTC EPS DRESDEN 2018

7th ELECTRONICS SYSTEM-INTEGRATION TECHNOLOGY CONFERENCE

www.estc-conference.net

September 18-20, 2018

CALL FOR ATTENDANCE

THE SINGLE LARGEST SEMICONDUCTOR PACKAGING CONFERENCE IN EUROPE

It is our pleasure to announce the **7th ESTC Conference**, the premier European scientific conference event in the field of microelectronics packaging and system integration.
It will be held **from 18th to 20th of September, 2018, at the Westin Bellevue Hotel in Dresden, Germany**. ESTC provides a perfect opportunity to learn about the latest developments in packaging and integration technologies. **Save the date right now!** ESTC is supported by IEEE-EPS in association with IMAPS-Europe.

ESTC 2018 received more than 200 abstracts from 30 countries, promising a high level technical program.

Visit the **www.estc-conference.net** to register. Early bird discount ends before July 31st.

AVT ZENTRUM FÜR MIKROTECHNISCHE PRODUKTION

IEEE ELECTRONICS PACKAGING SOCIETY

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ADDITIONAL CONFERENCE HIGHLIGHTS

Professional Development Courses: „Robust Electronics for Autonomous Driving“, „Introduction into Photonic Packaging and Interconnection Technology“, „Understanding Flip Chip Technology and its Applications“ or „From Wafer to Panel Level Packaging“.

Keynote Presentations are given by experts from Robert Bosch Semiconductor Manufacturing Dresden GmbH, Center Automotive Research of University Duisburg-Essen and Infineon Technologies.

Exhibitors at ESTC 2018: AMIC GmbH, Amkor Technology, budatec GmbH, CeTaQ GmbH, CWM GmbH, Cicor Group, Dyconex, First Sensor, Fraunhofer ENAS, Fraunhofer IZM, FRT GmbH, GE Sensing & Inspection Technologies, Häcker Automation, IEEE-EPS, Lintec Advanced Technologies (Europe) GmbH, Nanotest GmbH, Pac Tech GmbH, Pfarr Stanztechnik, Sentec E&E Co. Ltd., SGS Institut Fresenius, SHT Smart High Tech AB, TechSearch International, Tresky GmbH, XYZTEC bv.

Industrial Tours: First Sensor Microelectronic Packaging GmbH, Fraunhofer IPMS, SGS Institut Fresenius, VW „Gläserne Manufaktur“, Institute of Electronic Packaging Technology and Centre for Microtechnical Manufacturing of TU Dresden.

Visit website www.estc-conference.net to get up-to-date information.

General Chair:
Karlheinz Bock
TU Dresden, Germany

Executive Chair:
Thomas Zerna
TU Dresden, Germany

Technical Program Chair:
Steffen Kröhnert
Amkor Technology, Portugal

EPEPS 2018 – The Design and Analysis Frontier of Electronics Packaging

27th Conference on Electrical Performance of Electronic Packaging and Systems

San Jose, CA, USA

October 14 – 17, 2018

IEEE **Call for Papers**

IEEE ELECTRONICS PACKAGING SOCIETY MTT-S

EPEPS is the premier international conference on advanced and emerging issues in electrical modeling, measurement, analysis, synthesis, and design of electronic interconnections, packages, and systems. It also focuses on new methodologies and CAD/design techniques for evaluating signal, power, and thermal integrity and ensuring performance in high-speed, RF, and wireless designs. EPEPS is jointly sponsored by IEEE Electronics Packaging Society, IEEE Microwave Theory and Techniques Society and IEEE Antennas and Propagation Society. Submitted papers should describe new technical contributions related to the area of electrical performance of high-performance interconnect systems, covering:

- System-level, board-level, package-level and on-chip interconnects
- High-speed channels, links, backplanes, serial and parallel interconnects, SerDes
- RF/microwave/mm-wave packaging structures and components, antenna-in-package and RFIC co-design, mixed signal modules and wireless switches
- Signal and thermal integrity
- Power integrity and power distribution networks
- Low power mobile and personal applications
- Memory and DDR interfaces
- Jitter and noise management
- Electronic packages and microsystems
- Heterogeneous integration, 2.5D/3D interconnects and packages, TSVs and MCMs
- Electromagnetic (EM) and EM interference modeling, simulation algorithms, tools, and flows
- Macromodeling and model order reduction as it applies to electrical analysis
- Advanced and parallel CAD techniques for signal, power, and thermal integrity analysis
- Measurement and data analysis techniques for system-level and on-chip structures.

Submission Deadline: **July 15, 2018,** 8 p.m. Pacific Time

Conference Chairs:
Xiaoxiong Gu (IBM Research) xgu@us.ibm.com
Roni Khazaka (McGill University) roni.khazaka@mcgill.ca

For more information/contact: **epeps-admin@illinois.edu**

Submission Format: **2-column, 3-page PDF format only.** Selected papers will be invited for a special issue in *IEEE Transactions on Components, Packaging, and Manufacturing Technology.* Information for authors can be found at www.epeps.org. Submitted manuscripts should be camera ready and compliant with the general standards of the IEEE, including appropriate referencing. Noncompliant manuscripts will not be considered for review.

Location: San Jose Marriott, 301 S. Market St., San Jose, CA 95113, USA

Tutorials: EPEPS offers tutorials on state-of-the-art topics during the conference.

CAD Training: EPEPS offers training on the latest CAD software and tools on package/PCB design, SI and PI modeling, and high-speed SerDes simulation.

IEEE Education Credits: IEEE offers professional development hours (PDHs) and continuing education units (CEUs) for attending the EPEPS program.

Exhibits: EPEPS offers an excellent array of vendor exhibits. EPEPS is an exciting forum for vendors to demonstrate their state-of-the-art tools to attendees. Interested vendors can contact the conference administration for more details.

Conference Website: **www.epeps.org**

IEEE Electrical Design of Advanced Packaging and Systems

16th December – 18th December, 2018

CHANDIGARH, INDIA

Call for Papers

The IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium is the premier international conference in Asia-Pacific region to share the recent progress of design, modeling, simulation and measurement related to the electrical issues arising at the chip, package and system levels. Covering the paper presentations, industry exhibitions, workshops and tutorials, the EDAPS 2018 will be held at the **Taj Chandigarh, in Chandigarh, India from December 16 to 18, 2018**. The technical program of the symposium not only addresses the current technical issues but also brings out the topics on IC design, SiP/SoP packaging, EMI/EMC, EDA tools and most importantly the challenging issues in advanced 3D-IC and TSV design. For further information, please consult the web site at www.edaps2018.org.

IMPORTANT DATES

Paper Submission Portal Open: **July 15, 2018**
Paper Submission Portal Closed: **August 21, 2018**
Acceptance Notification: **September 21, 2018**

www.edaps2018.org

TOPICS

- 3D-ICs/TSVs/Interposers
- Testing on 3D-IC and SiP
- Signal and Thermal Integrity
- Power Integrity/Power Distribution Networks (PDNs) /Ground Noise
- Computational Electromagnetics and Multi-physics Methods for SI/PI/TI Analysis
- Thermal Management Design for 3D-ICs and SiP
- Design and Modeling for High-speed Channels and Interconnects
- High speed serial links jitter budgeting
- Jitter segregation algorithms and tools
- Time / Frequency Domain Measurement Techniques
- Power supply induced jitter and transfer functions.
- Nanoelectronics for 3D-ICs and SiP
- Active Devices and Circuit Modeling Technologies
- Electronic Packages, SiP/ SoP
- IC and Package Level EMC
- Antennas in Packages (AiP)
- RF/mm-wave and THz Packages
- Miniaturized and Embedded Passives
- Power Electronic Packages
- Advanced Simulation Tools and CAD
- Substrate Technology for Packages and PCBs
- Electrical Design of Flexible Devices and Sensing
- 2-D Materials for 3D-ICs and SiP
- 3-D ICs and SiP Reliability
- Electrical Design for 5G Wireless Communication
- DDR's Signal and Power integrity considerations
- Others

STUDENT TRAVEL GRANTS - A limited number of travel grants will be provided to support students of accepted papers. Selection will be based on papers submitted and requires paper presentation by the student at the conference.

PAPER SUBMISSION

All papers should be submitted electronically in **two-column and three-page** PDF file format. All submissions must be made through EDAPS website (**www.edaps2018.org**). A Microsoft Word template is available on the symposium website. Hardcopy submission will NOT be accepted. Submitted manuscripts should be camera ready and compliant with the general standards of the IEEE, including appropriate referencing. Non-compliant manuscripts will not be considered for review. An IEEE copyright transfer form completed with paper title, author(s) name(s) and authors' signatures should be submitted at the time of the paper submission. Files with scanned signatures are considered valid documents. Please check back with the symposium website (**www.edaps2018.org**) for updates on the paper submission. Selected contributions will be eligible for submission to a special issue of IEEE Transactions on Components, Packaging and Manufacturing Technology (TCPMT).

Call for Papers

The 20th International Conference on Electronics Materials and Packaging (EMAP 2018) will be held in Hong Kong, a gateway in between the East and West. The purpose of the conference is to promote awareness of new advances in materials, design and simulations, fabrication, reliability, and thermal management of microsystem/MEMS packages. The EMAP 2018 Committee is now inviting researchers, engineers, scientists and professors and students to submit an abstract and join EMAP 2018. The accepted papers will be submitted for inclusion into IEEE Xplore® Digital Library.

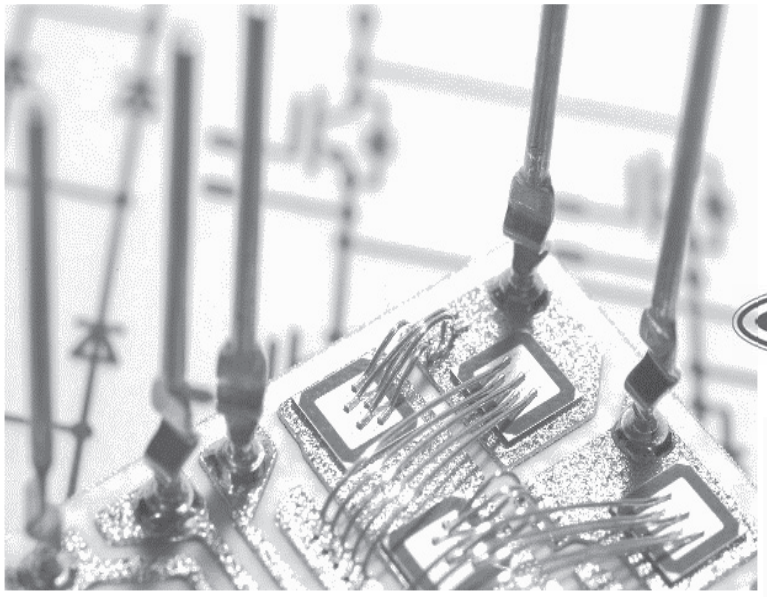
From the successful stories of previous EMAP conferences held in Japan, Korea, Malaysia, Singapore, and Taiwan, this annual event offers a great opportunity to unite people from academia, research institutions and industries to share their innovative thoughts, state-of-the-art technologies and recent developments. The program includes invited and keynote presentation from world-renowned speakers, interactive sharing sessions and technical short courses. Excursion will be arranged after the technical sessions to show you the natural side of Hong Kong. Come and join us. See you in EMAP 2018.

Topics:

- Additive Manufacturing
- Advanced Packaging Technologies
- Emerging Technologies
- Design, Modeling and Simulation
- High Density and 3D Packaging
- Interconnections
- Materials and Processing
- Microsystems Packaging and Applications
- Optoelectronics and Photonics
- Power Electronics Integration
- Quality and Reliability Assessment
- System Integration
- Thermal Management

Please submit your abstract between 200 – 300 words that describe the subject and key points of your paper to emap2018@ust.hk. Please download the abstract template from our website (http://emap2018.ust.hk).

Abstract Due: 31 August 2018



April 24-26, 2019
LAPLACE-ENSEEIHT,
Toulouse, France

CALL FOR PAPERS

INTERNATIONAL WORKSHOP ON INTEGRATED POWER PACKAGING 2019

The purpose of this workshop is to bring together researchers in the field of power electronics components, electrical insulating materials, and packaging technologies to rapidly promote the development and commercialization of high-density and high-efficiency power converters. Papers ranging from core material technologies to power converters are sought that address important challenges and present solutions to increase reliability and manufacturability of power electronic components and systems while targeting increased performance and reduced system cost. Papers are solicited in the following topics:

- System Integration And Optimization
- Compact Converter Design Techniques
- Modeling & Simulation - Components to Reliability
- Materials & Packaging Technology
- Power Semiconductor Devices / Modules
- Gate/Base Drivers
- Thermal Management & 3D Packaging
- Electromagnetic Interference
- Sensors & Protection
- High-Frequency Magnetics
- High Temperature & High Voltage Dielectrics
- Testing of Electrical Insulating Materials (e.g Space Charge and Partial Discharge Measurements)
- High-Temperature Capacitors
- Reliability Assessment & Lifetime Prediction
- Functional Safety & Product/Data Sheet Standards
- System/Component Design for Manufacturability, Compatibility with Standards, and Reliability

IWIPP COMMITTEE

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Treasurer: Andrew Lemmon | Univ. of Alabama
Publications Chair: Patrick McCluskey | Univ. of Maryland

DEADLINES

Abstract Submission: November 17, 2018
Notice of Acceptance: December 16, 2018
Final Paper Submission: February 15, 2019

WWW.IWIPP.ORG

Top Conference Papers based on 2017 Usage

Electronic System-Integration Technology Conference (ESTC), 2016 6th

(held on 13–15 Sept. 2016)

Manufacturing supply chain challenges—globalization and IOT
Katherine Pearsall

Indoor air quality sensing indicators
Markus Tuomikoski; Sami Ihme; Arttu Huttunen; Marko Korkalainen; Samuli Yrjänä

Design of a GaN HEMT based inverter leg power module for aeronautic applications
Benoit Thollin; Fadi Zaki; Zoubir Khatir; Régis Meuret; Donatien Martineau; Clément Fita; Pierre-Olivier Jeannin; Johan Delaine; Pierre Lefranc; Laurent Mendizabal; René Escoffier; Farid Hamrani; Laurent Quellec; Eric Lorin

High frequency high voltage power conversion with silicon carbide power semiconductor devices
Saijun Mao; Tao Wu; Xi Lu; Jelena Popovic; Jan Abraham Ferreira

Organic electronics application overview from automotive HMI to X-ray detectors
Romain Gwoziecki; Jean-Marie Verilhac; Antoine Latour; Amélie Revaux; Christophe Serbutoviez; Audrey Martinent

Electronics Packaging Technology Conference (EPTC), 2016 IEEE 18th

(held on Nov. 30 2016–Dec. 3 2016)

3D-printing and electronic packaging—current status and future challenges
C. Bailey; S. Stoyanov; T. Tilford; G. Tourloukis

Embedding of wearable electronics into smart sensor insole
M. Hubl; O. Pohl; V. Noack; P. Hahlweg; C. Ehm; M. Derleh; T. Weiland; E. Schick; H-H. Müller; D. Hampicke; P. Gregorius; T. Schwartzinger; T. Jablonski; J.-P. Maurer; R. Hahn; O. Ehrmann; K.-D. Lang; E. Shin; H. -D. Ngo

Copper wire bond pad/IMC interfacial layer crack study during HTSL (high temperature storage life) test
Mingchuan Han; Miao Wang; Lidong Zhang; Beiyue Yan; Jun Li; Meijiang Song; Varughese Mathew

Development of Chip-to-Wafer (C2W) bonding process for high density I/Os Fan-Out Wafer Level Package (FOWLP)
Sharon Pei-Siang Lim; Ser Choong Chong; Mian Zhi Ding; Vempati Srinivasa Rao

Integration of MEMS/Sensors in Fan-Out wafer-level packaging technology based system-in-package (WLSiP)
André Cardoso; Steffen Kroehnert; Raquel Pinto; Elisabete Fernandes; Isabel Barros

Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2017 16th IEEE Intersociety Conference on

(held on May 30 2017–June 2 2017)

Microchannel cooling strategies for high heat flux (1 kW/cm^2) power electronic applications
Ki Wook Jung; Chirag R. Kharangate; Hyoungsoon Lee; James Palko; Feng Zhou; Mehdi Asheghi; Ercan M. Dede; Kenneth E. Goodson

Electro-thermal reliability study of GaN high electron mobility transistors
B. Chatterjee; J. S. Lundh; J. Dallas; H. Kim; S. Choi

Liquid cooled system for aircraft power electronics cooling
Debabrata Pal; Mark Severson

Micromesh-covered superhydrophobic surfaces for efficient condensation heat transfer
Rongfu Wen; Shanshan Xu; Ronggui Yang

Experimental-theoretical thermal and electrical analyses of insulated gate bipolar transistors (IGBT) power module
Philippe R. d'Egmont; Carolina P. Naveira-Cotta; Robson F. S. Dias; Christopher P. Tostado; Fernando P. Duda; Kelvin Chen

Electronic Components and Technology Conference (ECTC), 2017 IEEE 67th

(held on May 30 2017–June 2 2017)

A Design Study of 5G Antennas Optimized Using Genetic Algorithms
Vincens Gjokaj; John Doroshewitz; Jeffrey Nanzer; Premjeet Chahal

First Demonstration of 28 GHz and 39 GHz Transmission Lines and Antennas on Glass Substrates for 5G Modules
Atom O. Watanabe; Muhammad Ali; Bijan Tehrani; Jimmy Hester; Hiroyuki Matsuura; Tomonori Ogawa; P. Markondeya Raj; Venky Sundaram; Manos M. Tentzeris; Rao R. Tummala

Latency, Bandwidth and Power Benefits of the SuperCHIPS Integration Scheme
SivaChandra Jangam; Saptadeep Pal; Adeel Bajwa; Sudhakar Pamarti; Puneet Gupta; Subramanian S. Iyer

Reliability Challenges in 2.5D and 3D IC Integration
Li Li; Paul Ton; Mohan Nagar; Pierre Chia

Heterogeneous Integration at Fine Pitch (≤ 10 μm) Using Thermal Compression Bonding
Adeel A. Bajwa; SivaChandra Jangam; Saptadeep Pal; Niteesh Marathe; Tingyu Bai; Takafumi Fukushima; Mark Goorsky; Subramanian S. Iyer

Upcoming EPS Sponsored and Cosponsored Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the EPS sponsors and supports a number of global and regional conferences, workshops and other technical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through IEEE Xplore.

Name: 2018 19th International Conference on Electronic Packaging Technology (ICEPT)
Location: Shanghai, China
Dates: Aug 8, 2018–Aug 11, 2018

Name: 2018 IEEE 38th International Electronics Manufacturing Technology Conference (IEMT)
Location: Melaka, Malaysia
Dates: Sep 4, 2018–Sep 6, 2018

Name: 2018 IEEE Electronic Design Process Symposium (EDPS)
Location: Milpitas, CA USA
Abstract Submission Date: Jun 15, 2018
Dates: Sep 13, 2018–Sep 14, 2018

Name: 2018 7th Electronic System-Integration Technology Conference (ESTC)
Location: Dresden, Germany
Dates: Sep 18, 2018–Sep 21, 2018

Name: 2018 40th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)
Location: Reno, NV USA
Dates: Sep 23, 2018–Sep 28, 2018

Name: 2018 13th International Congress Molded Interconnect Devices (MID)
Location: Würzburg, Germany
Dates: Sep 25, 2018–Sep 26, 2018

Name: 2018 24rd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)
Location: Stockholm, Sweden
Dates: Sep 26, 2018–Sep 28, 2018

Name: 2018 IEEE 27th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
Location: San Jose, CA USA
Dates: Oct 14, 2018–Oct 17, 2018

Name: 2018 IEEE Holm Conference on Electrical Contacts
Location: Albuquerque, NM USA
Dates: Oct 14, 2018–Oct 18, 2018

Name: 2018 13th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)
Location: Taipei, Taiwan
Abstract Submission Date: Jun 15, 2018
Dates: Oct 24, 2018–Oct 26, 2018

Name: 2018 IEEE 24th International Symposium for Design and Technology in Electronic Packaging (SIITME)
Location: Iasi, Romania
Dates: Oct 25, 2018–Oct 28, 2018

Name: 2018 IEEE CPMT Symposium Japan (ICSJ)
Location: Kyoto, Japan
Dates: Nov 19, 2018–Nov 21, 2018

Name: 2018 IEEE 20th Electronics Packaging Technology Conference (EPTC)
Location: Singapore
Abstract Submission Date: Jun 15, 2018
Dates: Dec 4, 2018–Dec 7, 2018

Name: 2018 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)
Location: Chandigarh, India
Abstract Submission Date: Jul 22, 2018
Dates: Dec 16, 2018–Dec 18, 2018

Name: 2018 20th International Conference on Electronic Materials and Packaging (EMAP)
Location: Hong Kong
Abstract Submission Date: Jul 31, 2018

Nanopackaging Activities in EPS

Nanopackaging is defined as the packaging of devices and systems with nanoscale materials and processes for improved performance, functionality, reliability and cost. Nanopackaging seeks to bridge the gap between ICs, which are at the nanoscale, and the rest of the system components that are typically at milliscale or microscale. It plays a key role in all the major aspects of system integration: improved functional density, higher power densities and power efficiency, higher bandwidth with lower power, improved thermal management, and better reliability.

The role of nanopackaging is briefly described in the five categories below.

Interconnections, assembly and reliability: Nanoscale materials can be engineered to attain an unusual and beneficial combination of properties. Examples include: a) nanoscale underfills with low CTE, high Tg and high thermal conductivity for applications in 3D IC stacks and packages, b)nanometallic interconnections for low-temperature assembly with higher current-handling and finer pitch, c) Nanoscale barriers as ultra-thin conformal coatings to replace bulky ceramic cases and hermetic cans in flexible electronics and bioelectronics implants.

Thermal management: Nanoscale materials and interfaces improve the heat rejection and spreading from the chip to the heat-pipe or coldplates, from where the heat is rejected to the ambience. Two-dimensional nanomaterials that are made of graphene and boron nitride can improve the film thermal conductivity, while also allowing better phonon transfer across the interfaces, when fabricated as thin conducting or insulating films.

Functional Components: Nanomaterials can provide unique RF, sensing and digital packaging functions. As one such example, ferromagnetic nanowires are emerging as suitable candidates for integrated nonreciprocal components for mm wave communication functions. Nanopackaging also encompasses packaging of nanoscale devices using both top-down nanopatterning processes and bottom-up self-assembly processes.

Flexible and Printed Electronics: These are emerging to address the large market need for IoT (Internet of Things), healthcare and monitoring through wearable and implantable electronics. Nanomaterials play a role in low-temperature deposition of conductors with printed or additive manufacturing approaches. Nanowire composites can achieve high electrical conductivity with low filler loading by using nanowire fillers. Such composites can be also applied in transparent electronics. Printed graphene- and CNT-based switches are being explored for printed active devices on flex packages.

Power Supply and Conversion: Nanostructured electrodes improve the volumetric power densities because of their higher surface area, conformal ultra-thin dielectrics, and counter electrodes and thus lead to thinner power components. These can be embedded into the package or on wafers, instead of mounting them as discrete surface-assembled bulky components.

In the future, nanostructured materials and processes will dominate almost all aspects of electronic packaging. IEEE EPS and IEEE Nanotechnology Council are releasing a special issue in IEEE Nanotechnology Magazine to describe the importance of this Nanopackaging to IEEE nanotechnology audience. They are also planning on organizing three technical sessions at the IEEE Nanotechnology Materials and Devices Conference in the areas of Thermal Materials and Nanometal Interconnects; High-Speed Nanopackaging Interconnects and Devices; and Nano Bio Packaging. The IEEE NTC and EPS also takes active role in shaping up Nanopackaging Sessions at IEEE NANO conference, short courses across the globe and EPS webinars. Headed by Prof. James Morris, they also are releasing the second edition of Nanopackaging Handbook this summer.

The committee is headed by M. Raj Pulugurtha (Florida International University, mpulugur@fiu.edu), Chris Bailey (University of Greenwich), James Cai (Tsinghua University) and advised by James Morris (Portland State University) and Katsuaki Suganama (Osaka University). Please contact them if you like to contribute to the committee's activities.

M. Raj Pulugurtha
IEEE EPS Nanotechnology Technical Committee Chair

IEEE 5G Initiative Status

5G is the next generation wireless network technology that is expected to significantly increase data speeds, produce ultra-low latency times, support the connection of many more devices, and increase energy efficiency of the network elements. Some future applications that will require the characteristics of 5G include:

- Vehicle-to-vehicle and vehicle-to-infrastructure communication
- Autonomous vehicles
- Remote health services and health care monitoring
- Augmented and virtual reality
- Smart cities and smart homes
- Industrial automation
- Device interconnection (IoT)

As part of the IEEE Future Directions Initiative, the IEEE 5G Initiative was formed to foster a new technical community that will address the technical challenges posed by the extremely difficult challenges need to be solved in order for 5G to become a viable ecosystem. To assist in charting the progress of technology solutions for 5G, the IEEE 5G Initiative has embarked on a 5G Roadmap and estabslihed a working group is to identify short (~3 years), mid-term (~5 years) and long-term (~10 years) research, innovation and technology trends in the communications ecosystem. This will enable the development of a concrete innovation and engagement roadmap guiding the IEEE community towards maximum impact contributions across its societies, and in conjunction with its demand-side as well as the wider industry and standards ecosystem. The outcome shall be a live document with a clear set of (accountable) recommendations; the document shall be updated annually and be developed in conjunction with the other working

groups. To read the initial 5G White paper which is a condensed summary of the 5G Roadmap which is being developed, visit https://5g.ieee.org/roadmap and download a copy.

The IEEE 5G Initiative "Beyond 5G Roadmap Workshop" took place on 5/23-24 during IEEE International Conference on Communication (ICC2018) in Kansas City with the objective to populate the 5G Roadmap technology versus timeline tables. Technical workgroups include Standardization Building Blocks, Millimeter Wave, Hardware, Massive MIMO, Applications and Services, Edge Automation Platform, Security, Satellite, and Testbed. During this workshop, participants from IEEE Societies looked into the chances, challenges, gaps, and possible directions of solutions with respect to these focus areas in three-year, five-year, and up to ten-year timeframes. Special attention is given to cross-discipline cross-workgroup sync and information flow during breakouts, exercises, and crosscuts sessions. At the end, each TWG presented their process report and invited comment across teams, followed by leadership team feedback and analysis roundtable. The next milestone is at IEEE 5G World Forum on July 9–11 in Santa Clara CA, http://ieee-wf-5g.org

The EPS Society, as the focus is on the heterogeneous integration & system in package technologies of assembly and testing, found resonance in TWGs such as Hardware, mmWave, Massive MIMO, and Test bed. Much of the challenges such as miniaturization, thermo, heterogeneous integration, as well as characterization and verification, can be addressed only by re-visiting the basics of theory and technologies from various design communities. As the 5G service is ramping up in 2020, each section of the supply chain must be ready to address the use cases, deliver the critical technical effectiveness during the new product engineering, then excel in scaling, yield, and cost.

Deep dive into the roadmap readiness found that the 5G technologies for under 6 GHz is relative matured, though challenges remains in topics from miniaturization and component performance issues closer to 6 GHz. On the other hand, technologies for millimeter wave range, including phase array antenna, power amplifier efficiency/thermo, co-existence with other sub-systems, and cost-effective testing methodologies, are among those that are more open to innovation and development. It is agreed that the challenge is complexity in nature, hence co-design across the industries and trainings is critical. The gaps present themselves as opportunities for the equipment venders, material suppliers, semiconductor and component manufacturers, system integrators, and many more.

Henceforth, the Heterogeneous Integration Roadmap (HIR) would find itself an essential underlying framework for the 5G Initiatives. Not only the focus areas match with the 5G landscape well (e.g. Fixed wireless, space and aerospace, back-hull, mobile/wearable/IoT etc), but also the multi-physics, across IC/package/PCBA co-design process HIR promotes would find value and create innovation for all. This is where EPS, together with societies that works on millimeter wave, semiconductors, and communications, should work closely together in the coming years.

As for the millimeter wave front-end implementation, which remains one of the most focused elements of 5G deployment, close collaboration of the industries and research community in EPS and in MTT Societies is crucial to progress. There is close coorporation and collaboration between the IEEE 5G Roadmap initiated by the MTT Society and the heterogeneous Integration Roadmap initiated by the EPS Society, now sponsored by EPS, EDS, Photonics, together with ASME EPPD & SEMI. Working in collaboration together sharing vision and learning from each other's perspectives will be important for us to accelerate finding potential solutions to difficult challenges, for the benefit of society.

Dr. Harrison Chang
EPS Representative to the IEEE 5G Initiative

Dr. Timothy Lee
HIR Aerospace and Defense Technical Working Group Chair

MEMBERS SPEAK

Personal Reflections on IEEE Membership

Reprinting an article from 2011

Introduction

The purpose of this article is to answer a question often asked by new engineering graduates. The answer to this question bedevils officers in IEEE. The question is "How does IEEE benefit me?"

The best answer to such an open-ended and very personal question is provided by a case study, a common pedagogical approach used in business school. I will use my own experience as the basis of a case study.

Let me begin this short article with full disclosure: I am an electronics engineer rather than an electrical engineer. Although I have worked for a number of large firms dominated by electrical engineers, my bachelors degree is in General Engineering.

Career Development

I joined IEEE while I worked at Motorola GEG in the 1980s (after working at Lockheed). My engineering colleagues at Motorola were, by an overwhelming majority, electrical engineers. My motivation was driven my several self-perceptions. These included a sense of awe of the advances underway in electronics and, admittedly, a personal sense of inadequacy.

As I received IEEE literature, I became engrossed in the CPMT Transactions. CPMT was the society in IEEE that most embraced mechanical aspects, and this was a time in which technical change was largely driven by innovation of electrical components and integration of electronics into products. Reading the CPMT Transactions drove me to the ASU library to read further on many subjects, primarily materials science (a course not in my undergraduate curriculum).

I worked for a couple additional defense electronics firms (Ford Aerospace and Teledyne), but my deeper involvement in IEEE developed after the end of the Cold War. After the Berlin Wall fell, I transitioned to commercial electronics with Compaq Computer. Compaq was a company growing so fast that President Reagan

had visited to see who was affecting the international balance of trade. As a consequence of explosive growth, the Compaq working environment offered challenges.

At Compaq, I used what I saw as the congruence of my skills with apparent needs. Commercial electronics did not embrace the level of rigor common in military electronics, and I saw an opportunity to contribute in a meaningful way. Eventually, my small group was moved to reliability engineering. I sought out help after that organization shuffle, again, using IEEE connections. Mike Pecht at the University of Maryland (IEEE Fellow) and his staff offered much assistance. He invited me to participate in an IEEE reliability standard. Through this activity, I learned much about standards activities, and I have since participated in a number of standards in other standards bodies.

While at Compaq, I began to serve as an Associate Editor of the CPMT Transactions under Avi Bar-Cohen (IEEE Fellow). Avi spent a good deal of time training me how to be an editor. My writing skills definitely improved.

After ten years at Compaq, I moved to a disk drive company for a year. I then worked for Mike Pecht in his reliability lab for two years. This was a life changing experience, because the University had such a rich collection of equipment and so many expert faculty and staff. On a part time basis, I complete a dissertation on a reliability aspect of ceramic capacitors. Since 2006, the University has monitored how many times each dissertation has been downloaded. At this time, that download number is approximately 3000 times. If it had not been for IEEE, I probably would not have had this opportunity.

I took a job in Menlo Park with a consulting firm after the two years at the University of Maryland. I became active in IEEE in Santa Clara Valley in the hope of finding consulting work. Although I did find some consulting work, what I found in IEEE/SCV was a group of volunteers in the finest traditions of professionalism.

Paul Wesling (Fellow IEEE) provided me with a complete set of the IEEE/SCV newsletter called "Grid" going back to its beginning. I used this to write a short chapter history for Allen Earman's CPMT/SCV chapter guideline. As I read through the decades of Grids (during which Silicon Valley was created), I enjoyed reading between the lines of history. For example, student protests at the University of Illinois in Champaign-Urbana drove the first big parallel process based mainframe to government facilities in the Bay Area. The consequential software job listings were clearly listed in "Grid".

Paul Wesling continues with an electronic version of Grid he calls eGrid. This is a one page summary of technical talks in the valley. There are typically more than one each weekday. For the most part, these talks are free to the public. And, for the most part, these talks are riveting, because these talks are provided by the people who are actually doing the work they are discussion. All the drama of real life people is evident.

During my period in Menlo Park, I volunteered to give some presentations for CPMT/SCV. Harvey Miller, a Silicon Valley icon, has long served as the organizer of the CPMT presentations. My first presentation was on economics and engineering for a joint meeting of GOLD and CPMT. In doing this presentation, I invited a colleague from the east coast who had an economics undergraduate degree. She and I have since coauthored several presentations and articles.

I served as Secretary, Chair and Vice Chair of CPMT/SCV chapter. The CPMT chapter had a long history, one of the longest in Silicon Valley. Allen Earman (who became the IEEE/SCV section chair) insisted that I participate in the section meetings. Of course Allen was correct. I also found this to be a wonderfully insightful experience, because I was meeting the people who were the backbone of Silicon Valley.

The IEEE connections transcend just one organization. I created the Silicon Valley Engineering Council Journal by requesting articles from my many IEEE colleagues. The Journal has now been in three volumes.

Currently, I am serving on the Board of Governors of CPMT. This is an exciting opportunity, and I hope to bring more technical scope and breadth to CPMT related to the word "components".

Conclusion

My library research has since grown since the 1980s to become habit. I have held citizen library cards at many local university libraries, and my interests have expanded to allied subjects. My IEEE colleagues have been of great help to me in learning about electronics. I have transitioned from a general engineer to an electronics engineer.

IEEE/SCV is a pot of gold. It is there for you to mine.

Daniel Donahoe
IEEE Senior Member

IEEE Mentoring Connection

Interview by Eric Perfecto, BOG member, with Cathy Downer, Project Manager of IEEE Mentoring Connection Coordinator

When was the TMC instituted as the prefer IEEE mentoring site?
We conducted focus groups with IEEE GOLD members to find out what they were looking for in a mentoring program. We wanted to make sure there was a need and to find out who or what type of IEEE member they were looking for as a mentor. We wanted to propose a unique membership benefit to this group to help with retention. Our focus group participants (3 focus groups held via internet) consisted of one with US/Canada members, second with European members, and third with Asia, South Pacific (Australian area) members—all working within their time zones. Members within these focus groups told us they would value another IEEE member as a mentor—in fact they valued that relationship very highly.

While we ran these focus groups, I searched the web for an online mentoring program that was user friendly, worked within our parameters (less focused on staff administrative) and one that the mentee or protégé searched for their mentor. Not the type of

matching that staff reviewed files and matched the individuals up. I also did research with other membership organizations to find out who they used and how they ran their member mentoring programs.

When I came across The Training Connection, I talked with them and asked for references. They offered information on how to help with setting up a program and on the issues we had. They offered a demo site that helped us make a decision. The people running the company were skilled in coaching, training, and running mentoring programs.

We ran a pilot program that began in 2005 with Region 1 and in August opened to Regions 2 and 3 to increase the pool of participants. We selected this area because of the larger cities, larger number of IEEE members in those cities to help with mentoring partnerships that would be close. After a six-month and year-end evaluations, we opened the program in 2006 to IEEE members.

Who and how can apply to be a mentor or to find a mentor?
IEEE members above the grade of Student Member can participate in the program as a mentor or mentee. We made the decision early not to include Students so we could offer a specific and unique program after they graduate to help with the transition into the professional fields and with career development. We did not want the program and the members participating to be used as an employment resource.

When entering the program for the first time you are asked how you are participating—as a mentor or mentee.

Why is this mentoring limited to professionals to professionals?
We wanted a unique membership benefit to offer to those members transitioning from student to the engineering professional fields. Our research told us that the members valued another IEEE member with more experience in the profession as an ideal mentor. IEEE is known as a professional membership organization.

In December 2007, we invited IEEE Graduate Student Members (GSM) to join the program. These members have graduated with their first degree and are in advanced degree programs.

Where can IEEE students go to get matched with professionals?
Many colleges and universities have their own mentoring programs for students who are matched with the college's alumni. MentorNet is an online program designed to match female students with professionals from various professional organizations within the U.S.

How does the mentor to protégé match occur?
When you enter the program as a mentor or mentee, you will complete a User Profile form with basic information. Next, the application form will ask for information that will assist in identifying and requesting the search for a match. The program will prompt you to each step. In the application form, the mentor's questions are a bit different than those of the mentee. The mentee will be asked to define their goals, while a mentor will be asked to

- check off skill competencies that you will bring to a mentoring partnership;
- provide a short biographical summary (can be pasted in from Word);
- check off your technical background based on the IEEE technical societies;
- reply to some short questions on what you would bring to a mentoring partnership as a mentor.

The next step is in the hands of the mentee as they decide who their ideal mentor will be. The mentee will decide if they want a mentor to be close geographically (by country, state/province, and city) so a face-to-face meeting can take place. If close proximity to the mentor is not the primary search criteria, the mentee can search based on skill competencies or gender. Whichever type of search is conducted, a list of potential mentors will be provided to the mentee. The mentee will review the list, along with access to their application, and then decide who they would like to contact through the system (via email) to initiate a mentoring partnership.

Once the mentee and mentor have decided to become partners, they will be encouraged to complete the mentoring agreement to help clarify expectations and define boundaries in their partnership. The IEEE Mentoring Connection Program also has a Mentoring Action Plan for the mentee to work on based on the agreed upon expectations. The Mentoring Action Plan will be reviewed at intervals by both the mentor and mentee.

What is the communication medium: email, phone, face to face?
Communication among the mentoring partners usually originates via email with the request to enter into a mentoring partnership and then each partnership decides how they will communicate. Most use email and phone. Some who are close enough meet face-to-face and also communicate via email.

Can you provide some statistics?
Presently we have 1176 mentees in the program with 540 mentors with over 80 countries represented. We have 256 active mentoring partnerships. Some mentees have more than one mentor. Since the inception of this program we have had twice as many mentees as mentors. We also have over 240 open requests for mentoring partnerships—something I try to work to close up and move over to our active partnerships.

What is the average connection (mentor to protégé relationship) time?
The mentoring partnerships run for one year. If a partnership is not working and both partners have decided to end it, we will close their partnership. Each is open to form new partnerships after one closes.

Can one have more that one mentor?
Yes, we have many mentees who have more than one mentor. We have asked that mentors have no more than two mentoring partnerships at one time. This is to allow time and effort for each partnership to grow and be successful, without causing stress on the mentor's schedule.

What is the average time required per month for a useful relationship?
We ask that mentoring partnerships use a minimum of two hours each month to communicate and discuss goals and issues.

How do you measure the success of the program?
I consider the active partnerships as success. This means that members have found a mentoring partner and are working to reach goals set by the mentee in discussion with their mentor.

What kind of resources does the program provide?
The Training Connection mentoring website has a section, "Library", which has a mentoring guide, newsletters, documents, presentations and other files related to mentoring and its partnerships. The site also has an active Discussion Forum where participants respond to questions posted by myself or our vendor. We also have a mentoring website on the IEEE site, http://www.ieee.org/mentoring which may have additional information you are looking for.

Can we find testimonials on the effectiveness of the program?

Craig Chatterton (mentor)
"Participating in the IEEE Mentoring program has been very rewarding and educational. It has given me the opportunity to share some of my experiences with younger engineers…I have participated in other long-distance mentoring programs and enjoyed them. However, the IEEE program stands out due to the focus on engineering backgrounds and professional careers. I look forward to these new and ongoing relationships."

Jamie Garcia (mentee)
"I went to the site and found it easy to navigate, searched by location, and was astounded to have such a wide selection of local potential mentors. I contacted by current mentor and arranged a meeting. I immediately received suggestions on how to best position myself for my upcoming performance review."

"It is a pleasure to have made such as strong connection, IEEE has honed a valuable service and whether you are a mentor or mentee, there is a great deal of value in this program."

Gary C. Hinkle (mentor)
"Helping young engineers develop in their careers is very rewarding. Working with some of these individuals has proven to be quite a challenge, because of the diversity among those seeking mentors. I'm glad to be contributing to this program."

I have been interviewing mentors and mentees in active mentoring partnerships! We have filmed half of them for the purpose of creating a mentoring product commercial. The mentors interviewed and filmed so far are from Pittsburgh, Ireland and Canada. Our mentees we will be interviewing and filming are from Cairo, Japan, Saudi Arabia. One mentee we interviewed and filmed is in Pittsburgh. This has been a lengthy process in finding members who wanted to participate, agreeable to be filmed and to use their comments on the program. I am also planning to hold an online forum with this group of participants so they can discuss their partnerships, successes, and how they worked through their partnerships—while attendees can send in questions for responses.

We are also working with The Training Connection for an online mentoring orientation program on 22 May 2008 at 7:00 am and again at 4:00 pm Eastern. A brief announcement will be placed in The Institute Online Alert for early April. We are not ready yet for registration, but will take any questions early for the program.

Thanks you very much for your time. My hope is that by publicizing this IEEE resource more people will use it.

Q&A with Dr. William Chen

Dr. William Chen is an IEEE Life Fellow, an ASME Fellow, a Fellow of ASE Group, one of the world's leading companies in semiconductor packaging and test, and a prominent leader in the packaging community since his early years at IBM. He is a former president of the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society, as which the IEEE Electronics Packaging Society (EPS) was formerly known. Dr. Chen was accorded the 2018 IEEE Electronics Packaging Award in recognition for his pioneering contributions to the field—from research and development through industrialization—and for his leadership in strategic roadmapping efforts in heterogeneous integration. Here, Dr. Chen speaks to the revolutionary developments in electronics packaging over the last decades and looks ahead to the innovations on the horizon that most excite him.

Why is now the right time for heterogeneous integration?
In the simplest terms, heterogeneous integration is driven by the fact that all electronic products, serving consumer and beyond, comprise many different components involving diverse technologies from a broad spectrum of ecosystem players. I am quite sure that you have a smartphone, a smartwatch, and a laptop. Maybe you also have a smart assistant at home. You may even have a robot that cleans the floor for you. All of these involve different technologies from different companies. So the big challenge becomes the integration of all these components together to achieve very specific functional and performance requirements. In this sense, the market—the demand of the consumers, you and I, all of us—has become the driving force behind the fast and disruptive changes in our industry, and subsequently the growing importance of electronics packaging.

It used to be that the leading industry driver was to build the most advanced computer. That's the original premise that we had—we all wanted to make computers go faster and faster. That was our world 10 or 15 years ago. Today, our world is changing dramatically, as we are now using electronics in so many life-changing ways, given the constant stream of evolving functions

and applications. Electronics are deeply embedded in the fabric of our societies and everyday life. Heterogeneous integration is playing an instrumental role, because it empowers creativity, innovation and collaboration across our industry, from large companies to startups to academia to research institutes to engineering students.

At what point in your career did you see that this was the way that the industry would be progressing?

There's always hindsight; many of us look back and say, "Oh, we should have known that!" In actual fact, the idea of heterogeneous integration and system-in-package (SiP) has been around for a long, long time, evidenced in the last sentence in the famous 1965 Gordon Moore paper who expressed his vision so well. But the reality is that progress has taken time, and ideas on how to implement heterogeneous integration as a comprehensive and structured technology have only gained prominence in recent years.

When I graduated with my first degree in London many years ago, I thought I knew everything. But following my graduate studies at both Brown and Cornell, my realization was that I knew a little bit of engineering very well, but the rest of it? I didn't know anything. I then went to work for a company called IBM and that is where I learned about the practice of engineering. I learned that it's just as important to know what you know as it is to understand what you don't know. My career at IBM set me on a path to expand my knowledge in those areas that I didn't know much about. I started as a mechanical engineer, and then I learned about electrical engineering, and then I learned about physics, chemistry, materials and interfaces. At every stage, what I didn't know was always primary in my mind and the motivation to gain as much knowledge as I could. While at IBM, I was extremely fortunate that I could reach out to other parts of the company, like IBM Research, and universities, as well as attend technical conferences. I learned the importance of collaboration across discipline lines and respect for people with different perspectives. I remember one very good professor who said to me, "Bill, you asked me questions about things that I thought were obvious, but these questions actually sparked an important research project later."

As the market changes, the requirements change, and the things I don't know are also changing. Homogeneous integration raised many, many important questions to which we do not have answers, and we are only now learning how to address them.

Could you please tell us about working across the different IEEE societies and engineers in the road-mapping part?

When we work on developing new technologies and developing new products, we all come with very different perspectives. But key to our success is how we interface with each other when approaching an issue. We consider how a physicist might look at it, how a chemist might look at it, how a mechanical engineer might look at it, and so on. Naturally, there are cultural differences across different scientific disciplines. But for the sake of science and progress, we try not to view these differing perspectives as a culture clash. Rather, we prefer to view them as vigorous discussions, where science and progress always wins!

It was always extremely important for us to have these vigorous discussions. When you want to put a product into the field, the idea first comes in from design engineers. Then we go through developmental engineers, and, at that time, it is very important to understand predictive modeling so that we go through the thought process of the different mechanisms—physics, chemistry and so forth—that go into making a product. Predictive modeling is thinking through from the beginning of concept to manufacturing and out to the field. That is a very similar thing to developing this roadmap.

Developing the roadmap is looking into the future and asking, What is our vision? What do we know? What don't we know? Where are the roadblocks? What research and innovation is needed to overcome these roadblocks? But the further we look out into the future, the greater are the unknowns. As we collectively decide the important knowledge gaps and understand the roadblocks—whether we should overcome the roadblocks or maybe walk around them—we put these ideas out into the ecosystem so as to inspire vigorous discussions and productive research. I wish to paraphrase the title of Jack Kilby's Nobel Prize acceptance speech, "Turning Potential into Reality." This is fundamentally what the roadmap is all about—it is about turning vision into reality. (I recall that Jack Kilby was an IEEE member and an EPS member.)

What are some of the ways that you are most proud to see how IEEE EPS itself has grown?

I am very pleased that packaging engineering is recognized as a profession, and that although our engineering education may come from different disciplines, it is recognized that we absorb these different knowledge bases and move forward as our own profession. This is very gratifying. The mere fact that CPMT changed its name to the Electronics Packaging Society is both recognition and validation; it means that the whole ecosystem is coming together and packaging is recognizably playing a major role.

Further, the value proposition that packaging brings to the greater electronics industry is increasingly important. We are moving further away from the traditional business model, where semiconductor people worked exclusively with packaging people. Now, packaging people are working with systems people, again underscoring the importance of heterogeneous integration. Today, the electronics ecosystem is drawing closer and tighter, and the interfaces are becoming less visible and distinct. We are seeing more of a wave of continuity. It is making the value proposition of packaging more important, and that, too, is very gratifying.

What's the thing that you don't know right now that you would like to learn more about?

That is actually a pretty long list. There are things that excite me in terms of building new products, and there are things that excite me in terms of learning something new—these are not always the same.

The interface between materials, interface between people, interface between different disciplines … that is always the most difficult thing. It's always most difficult to understand the boundary between the different sciences and the boundary between different businesses. In our profession, the interface is the question that we are always the opportunity and the challenge.

What's something that genuinely has surprised you about your industry?

I am genuinely surprised by how fast things are changing. The speed of change is staggering—and only accelerating. It is so stimulating that it keeps me awake at night and actually makes my brain work harder.

SANTA CLARA VALLEY CHAPTER HISTORY

The electronics industry was established on the San Francisco peninsula in the early part of the 20th century with firms such as Federal Telegraph and Magnavox, but in the early 1950's electronic products were unreliable by today's standards, suffering from poor manufacturing control and material failure mechanisms unfamiliar today such as mold. A joint conference held in Washington, D.C. in 1950 called the Symposium on Improved Quality Electronic Products created dialog that eventually spawned the Institute of Radio Engineers (IRE) Professional Group on Component Parts in 1953. A companion manufacturing group called the IRE Professional Group on Product Engineering and Production (PEP) was formed in 1954. Formal published Transactions began with the Transactions of the IRE Professional Group on Component Parts in 1954 and the IRE Transactions on Production Techniques in 1956.

In 1955 there was a young production manager at Hewlett Packard (HP) named Bud Eldon. This was Bud's first job after service in the U.S. Navy during World War II and completion of a bachelors degree in physics and M.BA at Stanford. At direction from Bill Hewlett to the HP vice president of manufacturing, Ed Parker, Bud was asked to begin a local chapter IRE PEP. Bud recruited about a dozen local professionals with similar interests from local firms including AMPEX, HP, Litton, Sierra Electronics, SRI and Varian. They formed the San Francisco chapter of the IRE PEP in 1956. Their shared purpose was to exchange non-proprietary information to address a key technical problem facing the handful of bay area electronics firms in 1955, fabricating printed wiring boards (PWB). The PWB at the time was rudimentary by today's standards and was fabricated from paper. In forming this organization, the IRE PEP members were building the foundation that historian Christophe Lecuyer described as a "manufacturing district, a region where there is a community of learning, practice and collaboration," a manufacturing district we today call Silicon Valley.

In 1963, IRE merged with the American Institute of Electrical Engineers (AIEE) to form IEEE. At this time Bud was chairman of the IRE PEP, and the new organization focused on consolidation. Bud and the chairman of the IRE Components group, Lew Kahn, merged the groups together to form the Professional Group on Components, Packaging and Production.

Both commercial electronics and military electronics grew in the 1960's with development and production of the IBM 360 mainframe computer and CDC 7600 supercomputer and the Polaris and Minuteman missiles. These 1960s products used glass-epoxy circuit boards, ceramic substrates and early integrated circuit packages in configurations such as the dual in-line package (DIP.)

What we call Silicon Valley developed in the 1970's with the success of Intel and the other integrated circuit firms. In addition, the systems that used the integrated circuit blossomed in new personal computer firms like Apple in 1976. These systems firms grew more successful with Sun Microsystems and Silicon Graphics founded in 1982 and Cisco Systems in 1984. Much of the emphasis of the CPMT Society was on components in the 1980s, although many of its members worked at the system level at firms such as Tandem Computer.

Bud Eldon became the Director of Region 6, the IEEE Treasurer and the President of IEEE in 1985. Bud led the effort to internationalize IEEE and was elected IEEE Fellow in 1987.

The 1990s saw explosive growth of the computer industry, especially with the advent of the Internet. Of course, the end of the decade experienced the painful dot com boom and bust. The CPMT Chapter elected its first woman chapter chair, Linda Matthew in 1994.

In 2003 while Tom Tarter was chairman, the Chapter was awarded the CPMT Chapter of the year award. Also in 2003, continuing his influence at the highest levels, Bud was chair of an ad hoc committee to promote elevation of engineers and practitioners to IEEE Fellow grade.

The chapter has supported many CPMT conferences including ECTC, APM, IEMT, and Holm.

Answering the call that was expressed by John Powers as “keep CPMT vital” and the call to action provided by many technology leaders in response to recent declines in the number of bachelors degrees in engineering, chapter chairman, Allen Earman (2005-2006) formed a sister chapter in Malaysia, a student chapter at San Jose State University and a region 6 micromouse best packaging award. Dan Donahoe, chapter chair 2007-2008, is serving as the chief editor for the inaugural Santa Clara Valley Engineers Week Journal in 2009.

The story of our chapter reflects the story of the electronics industry, the story of Silicon Valley and the story of success due to continuity of leadership from many volunteers such as Bud Eldon. As we move into a new century, our chapter’s story continues to evolve to face new technical challenges in nanotechnology and biologically based electronics.

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IEEE Senior Member

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3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
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