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President's Column....

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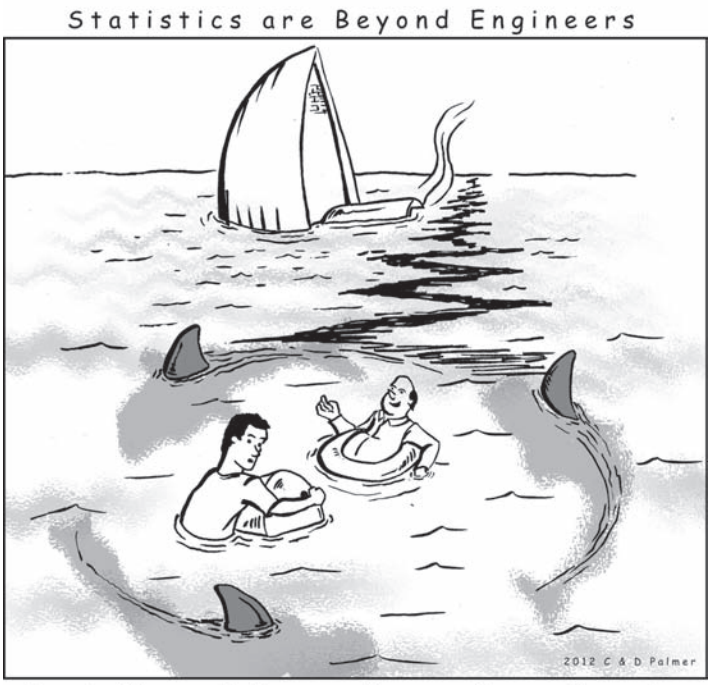
This is a new page of the IEEE CPMT Society. It is not only because there is a new face-lift for the CPMT official website (cpmt.ieee.org), but also because this is the first time ever a representative from Region 10 (Asia Pacific Region) has become the President of CPMT. The message is clear: IEEE CPMT is a global professional society! I would like to take this opportunity to thank my predecessors Rao Tummala, Phil Garrou, Bill Chen, and Rolf Aschenbrenner for their continuing effort to push the trend of globalization. Gratitude is also due to the CPMT Board of Governors (BoG) for their support to make this happen. Perhaps this is a good time for me to tell my personal story with CPMT….

I joined IEEE in 1996. My ECTC experience started from 1999. My first CPMT appointment was the Secretary of CPMT Hong Kong Chapter in 2000. I was elected the Chapter Chair in the following year. After two years of Chapter Chair service, I was appointed to fill a vacant CPMT BoG member-at-large position in 2003. Afterward, I was elected to take office of VP-Conferences for the term of 2004–2005. In 2006, I became a Distinguished Lecturer of CPMT and co-Editor-in-Chief of *IEEE Transactions on Components & Packaging Technologies*. I was elected to the CPMT BoG as a member-at-large again in 2010 and then was drafted to take office of interim VP-Technical in mid 2011. On the other hand, my IEEE membership grade was elevated to the Senior Member in 2001 and I was elected IEEE Fellow in 2008. Additionally, I received one ECTC Best Paper Award and one CPMT Society Award, respectively, in 2004 and 2008. I wish my journey from

(continued on page 3)



Dont Worry! Every Year, More People Die from Hippo and Dog attacks than from Sharks.

NEWSLETTER SUBMISSION DEADLINES:

1 May 2012
1 August 2012
1 November 2012
1 February 2013

Submit all material to nsltr-input@cpmt.org

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Chapters and Student Branches

Refer to cpmt.ieee.org for CPMT Society Chapters and Student Branches list

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the local Chapter Secretary to the global Society President could inspire our members to find their paths in the CPMT community.

It is a common practice for an officer to talk about ***VISIONS*** during his/her inauguration. But I plan to save that part for the next Newsletter as a dedicated topic. I would rather spend the remaining space in this column to emphasize the ***VALUES*** that I found along my path in CPMT. In my opinion, there have been four elements to drive me forward. They are ***Connection***, ***Information***, ***Publication***, and ***Recognition***. I first joined the CPMT Society for establishing connection with professional peers around the world. Afterward I found that CPMT sponsored conferences are indeed express channels to obtaining first-hand technical information. In addition, the CPMT Transactions are an excellent platform for the publication of my research outcome. Furthermore, the reputation built up from conference presentations and journal publications rewarded me with professional recognitions. These four elements have been closely tied to my journey with CPMT for more than a decade. Over the years, within the CPMT community, I made friends with many outstanding professionals, gained a lot of knowledge from them, published interesting papers, and received a number of honors and awards. I trust that many colleagues in CPMT feel the same way.

In *Sutta Nipata*, Gautama Buddha said "Thousands of candles can be lit from a single candle, and the life of the candle will not be shortened. Happiness never decreases by being shared." I would like to encourage our active members to share their fruitful CPMT experience with their professional colleagues and promote the values of CPMT as much, as far as possible. I look forward to seeing many more candles in our future CPMT events.

Past President's Message

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With my term as CPMT President now at an end, I'd like to extend my gratitude to you all for ensuring two such exciting and productive years. It has been an honor to be involved at this level of the organization. I plan to continue my involvement with CPMT wherever possible and further its aims, namely the ongoing development and networking of our profession, in other areas of my career.

The fact that we were able to launch the new CPMT website in 2011 is nice note to end on. I hope you agree with me that the new look and functionality is a great improvement. Thanks to the CPMT organizational team for their dedication to this project.

CPMT continues on its path towards globalization, which was already initiated by my predecessors. I am happy to report that over the last two years we have significantly expanded CPMT workshops, conferences and other activities in geographic regions not traditionally renowned for microelectronic research and development, but which are by any measure rapidly developing and increasingly central to our profession worldwide. I am also pleased to report that this expansion is also reflected by the make-up of our membership.

Congratulations go to our newly elected CPMT President, Ricky Lee. Professor Lee has long been strongly dedicated to developing our profession as a whole, evidenced by his numerous previous roles in CPMT and IEEE. I wish Ricky and the entire new team the best of success and look forward to working with them over the next two years.

CPMT Society News....

CPMT Society Officers Elected For 2012–2013

The CPMT Society Board of Governors elected its Officers for the two-year term of 1 January 2012 through 31 December 2013. The following individuals were elected:

President

S.W. RICKY LEE (M'97, SM'01, F'08) received his BSc degree from National Taiwan University in 1981. He went to the US for graduate studies in 1986 and received MSc from Virginia Polytechnic Institute & State University and PhD from Purdue University in 1987 and 1992, respectively. After one year of post-doctoral research at Purdue, he started his academic career at the Hong Kong University of Science and Technology (HKUST) in 1993. Ricky went through the ladders of tenure track faculty. In addition, from 2006 to 2008, he was on secondment to serve as Chief Technology Officer of the Nano & Advanced Materials Institute (NAMI) at HKUST. Currently Ricky is Professor of Mechanical Engineering and Director of Center for Advanced Microsystems Packaging at HKUST. He is also appointed the founding Director of HKUST LED-FPD Technology R&D Center at Foshan (near Guangzhou, Mainland China).

Ricky's research activities cover wafer level packaging and 3D IC integration, LED packaging and solid state lighting, lead-free soldering and solder joint reliability. He has substantial publications in international journals and conference proceedings. He also co-authored three books, published eight book chapters, and owned seven patents. Ricky has made vital contributions in the following technical areas: (1) applications of finite element method and fracture mechanics for stress analysis in electronic packaging; (2) investigation of board level solder joint reliability under thermal and mechanical loading; (3) development of microvias and high density

interconnect technologies for 3D packaging; and (4) development of LED wafer level packaging technologies for solid state lighting. A large number of researchers and engineers have been using Ricky's publications as their major sources of references. Due to his performance and achievements in electronic packaging research, Ricky was elected IEEE Fellow, ASME Fellow, and Institute of Physics (UK) Fellow. He is also the recipient of IEEE CPMT Electronics Manufacturing Technology Award, ASME EPPD Excellence in Mechanics Awards, IMAPS John A. Wagnon Jr. Technical Achievement Award, CIE-EMPT Electronic Packaging Technology Significant Contribution Award, ECTC Best Poster Paper Award, two-time ASME Journal of Electronic Packaging Best Paper Awards, and several other international conference best paper awards.

Ricky is very active in international societies and has been appointed many leadership positions. His professional services and contributions include: interim VP-Technical and VP-Conferences of IEEE CPMT Society, Member-at-large of CPMT Board of Governors, CPMT Distinguished Lecturer, co-Editor-in-Chief of IEEE Transactions on Components and Packaging Technologies, Associate Editor of IEEE Transactions on Advanced Packaging and ASME Journal of Electronic Packaging, Executive Committee Chair of ASME Electronic & Photonic Packaging Division, Chair of ASME Hong Kong Section, Chair of IEEE CPMT Hong Kong Chapter, General Chair of EMAP2006 Conference, Program Chair of ChinaSSL2011 Conference, Professional Development Course Committee Chair of ECTC, seven-time Professional Development Course Lecturer of ECTC, 12-year Members of Advanced Packaging/ Emerging Technology/Interconnection Technical Sub-committees of ECTC, and International Advisory Board Member of EPTC, ESTC, ICEPT, EMAP, IEMT, IMPACT, VLSI, SPJW. In addition, Ricky is a member of Assembly & Packaging Technical Working Group of International Technology Roadmap for Semiconductors (ITRS).

Vice President – Technical

JIE XUE (M'93, SM'09) is currently the director of Component Quality and Technology Group at Cisco Systems, Inc., San Jose, California. Her team is responsible for component technology development and qualification of ASIC, network processors and optical modules, as well as the development of advanced semiconductor and packaging technologies. Since joining Cisco in 2000, she has been working on developing high performance flip chip packaging, system-in-package, multichip modules, chip-scale-packaging for high reliability networking products. Prior to joining Cisco, Jie held several management and engineering positions in Motorola Inc., working on R&D and product development in the areas of high density interconnect for wireless applications, and packaging materials for MEMS sensors, automotive Engine Control Unit (ECU), displays, and optical interconnects.

Jie received a BS degree from Tsinghua University, a MS and Ph.D. from Cornell University. She is an IEEE Fellow and IMAPS Fellow. Her research has resulted in over 70 technical publications and conference presentations. She was IEEE-CPMT VP of Conference 2010–2011.

Vice President – Conferences

JEAN M. TREWHELLA (M'06) Ms. Trewhella received her B.S. in Physics from Antioch College (1987) and her M.S. in Applied Physics from Columbia University (1992). She joined the T.J. Watson Research Center, IBM, in 1988 where her work included polymer optical waveguides fabrication, electrical modeling, and optomechanical package design for data communication systems. In 2000 she created the High Speed Electrical and Optical Packaging Group in IBM Research directing work in electrical link signal integrity, advanced 1st and 2nd level packaging, and low cost high speed optomechanical packaging. She received an Outstanding Technical Achievement Award for her work on 10Gbps Ethernet Transceiver Development in 2003. In 2005 she drove IBM wide team of engineers and scientists to highlight key disruptive technologies synthesizing the messages into three GTO topics: Technology, Application-Optimized Systems, and Services 2.0. From 2006–2008 she was responsible for the Electronic Packaging Integration Group in IBM STG where her team developed the power5 and z10 system hardware. Currently Jean Trewhella is the Director of IBM Packaging Research and Development Center with responsibility of 3D, low cost, and high performance packaging technology for current and future products.

Ms. Trewhella was on the Strategic Advisory Board for NSF STC – Materials & Devices for Information Technology Research 2004–2008, she served as the General Chair of the 60th ECTC and is currently a member at large of the CPMT Board of Governors. She has authored numerous papers and holds over 20 US patents.

Vice President – Publications

R. WAYNE JOHNSON (S'77, M'79, S'80, M'82, S'85, M'87, SM'94, F'04) is a Professor of Electrical and Computer Engineering at Auburn University and Director of the Laboratory for Electronics Assembly & Packaging (LEAP). During his 24 years at Auburn, he has established teaching and research laboratories for advanced packaging and electronics assembly. Research efforts are focused on materials, processing, and reliability for electronics assembly and for extreme environment electronics. Current research projects span the temperature range for –180ºC to +500ºC. He is a CPMT Distinguished Lecturer on Extreme Environment Electronics. He has published and presented numerous papers at workshops and conferences and in technical journals. He was a co-author of the 2010 ECTC Best Paper of Conference and co-faculty advisor for the 2009 ECTC Intel Best Student Paper winner. He has also co-edited one IEEE book on MCM technology and written book chapters in the areas of silicon MCM technology, MCM assembly, automotive MCMs (IEEE Press), flip chip assembly and high temperature packaging (IEEE Press). Wayne was elected a Fellow of IEEE in 2004 for "his contributions to electronics that must operate in harsh environments."

Dr. Johnson received the B.E. and M.Sc. degrees in 1979 and 1982 from Vanderbilt University, Nashville, TN, and the Ph.D. degree in 1987 from Auburn University, Auburn, AL, all in electrical engineering.

Wayne is the current Vice President of Publications for the IEEE CPMT Society and serves as the Chair of the Publications Committee. He is a Co-Editor-in-Chief of the IEEE Transactions on Components, Packaging and Manufacturing Technology. He is also a member of the International Microelectronics and Packaging Society (IMAPS), the Surface Mount Technology Association (SMTA) and IPC.

Vice President – Education

KITTY PEARSALL (A'84, M'01, SM'02) Kitty Pearsall received the BS degree in Metallurgical Engineering in May 1971 from the University of Texas at El Paso. In 1972 she joined IBM as a Materials Engineer. In 1976 she left IBM on an educational leave of absence. During this absence, Kitty received the MS and PhD degree in Mechanical Engineering, Materials Option from the University of Texas at Austin in May 1979 and May 1983 respectively. From 1983 to present Kitty has served as an IBM technical resource in materials/package engineering in manufacturing, procurement and development environments. Twelve of these years were spent in technical management focusing on the qualification of various commodities.

In 2005 Kitty was appointed an IBM Distinguished Engineer (DE) and was elected into the IBM Academy of Technology. As a DE in the Integrated Supply Chain Kitty serves as a process consultant and subject matter expert working on strategic initiatives impacting qualification and end quality of procured commodities. She is engaged with WW teams implementing these cross-brand, cross commodity processes/products. As a technical executive in IBM Kitty is passionate about the development of the ISC technical pipeline and was awarded the Women in Technology Fran E. Allan Mentoring Award (2006) in recognition of her people development both in and outside of IBM.

Kitty has been a licensed Professional Engineer in the State of Texas since 1993. She is the holder of 2 US patents, 7 patent pending and several disclosures that have contributed to the IBM patent portfolio. She has numerous internal publications as well as 19 external publications in IEEE conferences and journals. Kitty was recognized as a 2007 recipient of the Cockrell Engineering Distinguished Engineering Graduate by University of Texas Austin. In 2008 she was inducted into the University of Texas Mechanical Engineering Department Academy of Distinguished Alumni.

Kitty is an active member in IEEE and CPMT. She holds memberships in TMS, American Society of Metals and CPMT. Kitty has been a member of the ECTC Manufacturing Technology Committee since 1993 and has been on the Professional Development Course (PDC) Committee since 2006. Since 2008 Kitty assumed the Chair position of the PDC.

During Kitty's tenure on the CPMT Board of Governors she has served as a Member at Large, the Strategic Awards Director, and currently as VP of Education. If reelected she plans to continue this and will focus on increased recognition of contributions to the CPMT Society in emerging Geos, and technical development of the CPMT women membership.

Vice President – Finance

THOMAS G. REYNOLDS III (M'92, SM'04) Dr. Reynolds received his PHD from Brown University in 1972 where he worked on synthetic inorganic chemistry of electronic materials. His MS (1966) and BS (1964) were from the University of Virginia in Materials Science and Mechanical Engineering respectively. Tom has worked in the field of electronic ceramic materials and other advanced technologies for more than 35 years.

Retiring in 2003, from 1992 Tom was the Director of Technology at Murata Electronics N.A., Inc. He has worked in the areas of leading edge designs in decoupling capacitors, hard disk drive activation, LTCC modules, and integrated passive components. He has acted as liaison between American designs and Asian development activities, as well as in merger and acquisition analysis. Prior to joining Murata, Dr. Reynolds worked for Philips Electronics for 18 years in both the US and Europe, developing processes and methods for electronic (dielectric) ceramics, and from 1968 to 1973 he was staff scientist at Texas Instruments.

Tom has been involved with CPMT and ECTC (Electronic Components Technology Conference) for more than 19 years. He was General Chair for ECTC in 2000 and was active for several years following this as Finance Chairman. He is also a Senior Member of IEEE. Tom has been a member of the CPMT Board of Governors since 2004 and VP of Finance since 2006. In addition he is currently serving as Treasurer of the ECTC.

Additional activities and responsibilities include Treasurer of the Ft Walton Sail & Power Squadron of the United States Power Squadron and he was Commodore of the Ft Walton Yacht Club in 2006. Tom also served on the Board and the Finance Committee of that Club from 2007–2010. Tom is also a Founding Member of the Florida Commodores Association – an association of more than 250 with the goal of fostering communication, guidance and mentoring of past present and future leaders. Tom is also a member of the Institute for Senior Professionals (North West Florida State College), an association of business, professional, medical and military professionals to advise and serve the local community based on their experience and expertise.

Newly-Elected and Appointed Members of the CPMT Society Board of Governors

In late 2011, CPMT Society members elected new Members-at-Large to the CPMT Board of Governors for the three-year term of 1 January 2012 through 31 December 2014. The following individuals were elected:

MASAHIRO AOYAGI (M'94, SM'10) received the Bachelor of Engineering in Electronic Engineering from Nagoya Institute of Technology, Nagoya, Japan, in 1982; and the Doctor of Engineering degree in Electronic Engineering from Nagoya Institute of Technology, in 1992.

He joined Electrotechnical Laboratory (ETL), Tsukuba, Japan in 1982, where he was engaged in the research and development of Nb, NbN superconducting devices and Josephson integrated circuits until 1994, for establishing Josephson Computer Technology. He was engaged in that of high speed signal measurement technology until 2000. He worked in optoelectronic sampling measurement technology as a guest researcher in National Physical Laboratory (NPL), Teddington, UK, from 1994

to 1995. ETL was reorganized into National Institute of Advanced Industrial Science and Technology (AIST) in 2000. He became a group leader of High Density Interconnection Group, Nanoelectronics Research Institute (NeRI), AIST. He worked as a group leader specified for fundamental 3D LSI chip stacking technology in the national R&D project of High Density Electronic System Integration from 1999 to 2004. He was a team leader of Opto-Electronic System Integration Collaborative Research Team, NeRI, from 2004 to 2009. He has been a principal research scientist of NeRI since 2009. His present research field is high-speed high-density electronic packaging and interconnection technology including 3D LSI chip stacking and optoelectronic hybrid packaging.

Masahiro Aoyagi was awarded the Tsukuba prize of 1991 for the development of Josephson prototype computer ETL-JC1. He has authored or co-authored 225 technical papers and has 80 patents.

Masahiro Aoyagi has been an IEEE CPMT member since 1998. He has been involved in the technical committee of Electronics Packaging Technology Conference (EPTC) held in Singapore and International Conference of Electronic Packaging (ICEP) held in Japan. He was the chair of IEEE CPMT Japan Chapter from 2009 to 2010.

Masahiro Aoyagi holds memberships in Institution of Engineering and Technology (IET), International Microelectronics and Packaging Society (IMAPS), Society of Photo-Optical Instrumentation Engineers (SPIE), Institute of Electronics Information and Communication Engineers (IEICE), Japan Institute of Electronics Packaging (JIEP), Institute of Electrical Engineers of Japan (IEEJ), and Japan Society of Applied Physics (JSAP).

AVRAM BAR-COHEN (M'85, SM'87, F'93) Dr. Avram Bar-Cohen is an internationally recognized leader in thermal science and technology, an Honorary member of ASME, and Fellow of IEEE, as well as Distinguished University Professor in the Department of Mechanical Engineering at the University of Maryland. His publications, lectures, short courses, and research outcomes, as well as professional service in ASME and IEEE, have helped to create the scientific foundation for the thermal management of electronic components and systems and pioneered techniques for energy-efficient sustainable design of manufactured products. His current research focuses on on-chip thermoelectric and two-phase microchannel coolers for high heat flux electronic components, thermal control of solid-state lighting systems, and polymer-fiber composite heat exchangers for seawater applications. Bar-Cohen was the general chair for the 2010 International Heat Transfer Conference in Washington DC and is the President of the Assembly of International Heat Transfer Conferences. He is the Editor-in-Chief of World Scientific Press' forthcoming Encyclopedia of Thermal Packaging. From 2001 to 2010 he served as the Chair of Mechanical Engineering at Maryland and is currently on assignment as a Program Manager in the Microsystem Technology Office at the Defense Advanced Projects Agency in Virginia.

In addition to Honorary membership in ASME, Bar-Cohen's honors include the Luikov Medal from the International Center for Heat and Mass Transfer in Turkey (2008), ASME's Heat Transfer Memorial Award (1999), Curriculum Innovation Award (1999), Edwin F. Church Medal (1994) and Worcester Reed Warner Medal (2000), and the Electronic and Electrical Packaging Division's Outstanding Contribution Award (1994) as well as the InterPack Achievement Award (2007). Bar-Cohen was the founding chair of the IEEE Intersociety Conference on Thermal Management in Electronic Equipment (ITHERM) in 1988 and was recognized with the IEEE CPMT Society's Outstanding Sustained Technical Contributions Award (2002), the ASME/IEEE ITHERM Achievement Award (1998) and the THERMI Award from the IEEE/SemiTherm Conference (1997).

Bar-Cohen has co-authored *Design and Analysis of Heat Sinks* (Wiley, 1995) and *Thermal Analysis and Control of Electronic Equipment* (McGraw-Hill, 1983), and has co-edited 14 books in this field. He has authored/co-authored some 350 journal papers, refereed proceedings papers, and chapters in books; has delivered 70 keynote, plenary and invited lectures at major technical conferences and institutions, and he holds 8 US and 3 Japanese patents. He has advised to completion 60 master's and Ph.D. students at the University of Maryland, the University of Minnesota and the Ben Gurion University (Beer Sheva, Israel), where he began his academic career in 1972. From 1998–2001 he directed the University of Minnesota Center for the Development of Technological Leadership and held the Sweatt Chair in Technological Leadership.

DARVIN R. EDWARDS (M'87, SM'10) Mr. Darvin R. Edwards received the B.S. degree in Physics from Arizona State University, Tempe, AZ in 1980. After joining Texas Instruments Incorporated in 1980, he developed integrated test structures such as strain gages, moisture sensors, thermal sensors, and structures to determine the impact of package stresses on IC thin film layers. He developed a set of IC design rules for packaging which has been continuously updated and is still in use today. He then worked to build TI's competence in thermal characterization and thermal management. Elected TI Fellow in 1999, he is presently manager of the Advanced Package Modeling and Characterization group which is responsible for thermal, electrical, and stress analysis for a wide range of product families, as well as ensuring successful qualification and introduction of products to the market. Packages and technologies he has helped develop include TSV, POP, MCM, FC-BGA, PBGA, QFN, WCSP, QFP, and SOICs. He is currently chair of the SRC GRC Interconnect and Packaging Sciences' Science Area Coordinating Committee, and works regularly with universities to coordinate TI's packaging research interests. Professional activities have included over 25 years of service on the Applied Reliability program selection committee of the ECTC, authoring 5 JEDEC standards, and serving as an industrial liaison on multiple SRC projects. Mr. Edwards has authored and co-authored over 45 papers in the field of IC packaging, has written two book chapters, and holds 20 US patents.

BETH KESER (M'99, SM'10) has over 15 years experience in the semiconductor industry. Beth received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. in Materials Science and Engineering at the University of Illinois at Urbana-Champaign. Beth's interests include developing revolutionary materials and packaging technologies for the semiconductor industry resulting in 7 patents, 5 patents pending, and over 33

publications in this area. Currently, Beth is the Wafer Level Packaging Product and Technology Manager at Qualcomm in San Diego. Her team and co-authors just presented 3 papers on their work on advancements in wafer level packaging at the 61st ECTC in Orlando.

Before joining Qualcomm in 2009, Beth Keser was instrumental in developing 2 packaging technologies during her career at Motorola and Freescale Semiconductor. Beth led the Wafer-Level Chip Scale packaging team at Motorola, which included directing the activities of process engineering, package characterization, package reliability, and mechanical modeling. Beth developed an innovative new double-bump structure where the first bump on the wafer was encapsulated with a photoimageable, filled stress compensation layer. Beth is a co-inventor on this invention US Patent. Also, to improve ball attach method for the first ball and second ball for the WL-CSP technology a new super-saturated flux was designed. Beth is a co-inventor of this invention US Patent. In addition, Beth and her co-inventors created a new under bump metallurgy specifically for this WL-CSP and had it patented.

In addition, Beth Keser was the lead technologist and manager of the Redistributed Chip Packaging Technology (RCP). Beth led the team that developed this technology for 6 years. Beth developed several process and material solutions for this new technology. Beth has filed 6 patents on this technology. Her team had 10 patents granted and 10 other patents filed. Beth presented RCP at the Phoenix local chapter of IEEE WAD and CPMT meetings, as well as at the Phoenix local MEPTEC luncheon. In addition, 2 papers were published at ECTC on RCP.

Beth is an IEEE Senior Member whose volunteer activities and professional society responsibilities include: ECTC Executive Committee 2010–present, 2012 ECTC Assistant Program Chair, ECTC Advanced Packaging Sub-committee member 2000–present, IMAPS Device Packaging Conference Technical Chair 2006–2009, IMAPS Flip Chip/CSP Sub-committee member 2000–2009, chair 2005–2008, SMTA's International WLP Conference WLP Track Chair 2010–2011.

Beth has been very active in IEEE CPMT's ECTC conference both as a volunteer and as a technical contributor. Beth has presented 4 papers at ECTC (2001, 2007 and 2011) and co-authored 5 other papers (2000, 2003, 2008, and 2011).

MERVI PAULASTO-KRÖCKEL (M'09) Dr. Mervi Paulasto-Kröckel is currently working as a professor at the Aalto University* School of Electrical Engineering in the Department of Electronics. She has broad experience in microelectronics packaging development specifically for automotive and power electronics market. Before transferring into the academic world in 2008, she worked over 12 years in the semiconductor industry in various R&D and management positions.

Paulasto-Kröckel began her studies at the Helsinki University of Technology in 1985. She studied materials science and engineering as her major and semiconductor technology as minor. After graduation as Master of Science in Technology in 1990 she continued her studies in the Technical Universities of Aachen (RWTH Aachen) and Helsinki and attained her doctoral degree in 1995.

After a 2-years post-doctoral appointment at the Joint Research Centre of European Commission in the Netherlands, her professional career continued in the electronics industry. In 1996, she moved to Munich, Germany where she started at Motorola Semiconductor Products Sector in a new team focusing on automotive electronics development. At Motorola she worked on several research and development assignments including flip chip process development and technology transfer to manufacturing. Her career took a new direction when she was invited to lead the packaging development of Infineon Automotive Power in 2004. At Infineon Technologies she was promoted to Director Package Development responsible for semiconductor assembly and interconnect development for automotive products worldwide. In this role she was responsible for over 10 M€ development budget and 50+ varying size projects interfacing with a large matrix organization of business managers, product and technology developers.

In the fall 2008 Paulasto-Kröckel was selected to become the successor of her former supervisor, professor Jorma Kivilahti. She moved with her Finnish-German family to Finland end of 2008, and is now chairing Electronics integration and reliability as well as Bioadaptive technology in Aalto University. Her research focus is on materials compatibility in electronics and MEMS, implantable electronics, interconnect technologies, multimaterial assemblies behavior under different loads and their characteristic failure modes and mechanisms. Her research group is heading several academic research projects, but has also a broad cooperation with major electronics companies.

Prof. Paulasto-Kröckel has over 40 international publications in fields of microelectronics packaging and interfacial compatibility of dissimilar materials. She is member of IEEE/CPMT and has participated in technical programme committees, chairing sessions and giving key note lectures in several IEEE CPMT conferences including ESTC, EPTC, APM, EuroSimE, IEMT, ASTR as well as IEEE ESSDERC conference.

She is also a member of the board of Okmetic, Finnish based wafer manufacturing company. Recently, she was selected to become a member of Finnish Academy of Technical Sciences.

Prof. Paulasto-Kröckel would like to contribute to the continuous development of CPMT and foster international co-operation between industrial and academic partners and between different disciplines. She would prefer to increase the focus in CPMT conferences on new research areas with high innovation potential and also on the frontend-backend integration. Also, she would strengthen the visibility of CPMT in Finland by organizing visits and conferences like ESTC2014.

*Aalto University is a new university created from a high-profile merger between three leading universities in Finland – the Helsinki University of Technology, the Helsinki School of Economics and the University of Art and Design

C. P. WONG (SM'87, F'92) Prof. C. P. Wong is currently Dean of the Faculty of Engineering at the Chinese University of Hong Kong. He is on a no pay leave from the Georgia Institute of Technology(GT) where he is a Regents' Professor and the Charles Smithgall Institute- Endowed Chair at the School of Materials Science and Engineering. He received his B.S. degree from Purdue University, and his MS. and Ph.D. degrees from the Pennsylvania State University. After his doctoral study, he was

awarded a two-year postdoctoral fellowship with Nobel Laureate Professor Henry Taube at Stanford University. Prior to joining GT in 1996, he was with AT&T Bell Laboratories for many years and became an AT&T Bell Laboratories Fellow in 1992 for his seminal contributions to low-cost high-performance packaging of semiconductor devices and components.

His research interests lie in the fields of polymeric electronic materials, electronic, photonic and MEMS packaging and interconnect, interfacial adhesions, nanofunctional material syntheses and characterizations, nanocomposites, such as well-aligned carbon nanotubes, graphenes, high performance electrical conductive adhesives, ultra high k capacitor composites, lead-free alloys, flip chip underfills, and novel lotus effect coating materials.

He received many awards, among those, the AT&T Bell Labs Fellow Award in 1992 (the most prestigious Technical Award bestowed by Bell Labs), the IEEE Components, Packaging and Manufacturing Technology (CPMT) Society Outstanding Sustained Technical Contributions Award in 1995, the IEEE Third Millennium Medal in 2000, the IEEE Educational Activities Board Outstanding Education Award in 2001, the IEEE CPMT Society Exceptional Technical Contributions Award in 2002, the Georgia Tech Class 1934 Distinguished Professor Award (the highest award bestowed by GT to a faculty) in 2004, named holder of the Charles Smithgall Institute-Endowed Chair Professor (holder of one of the two GT Institute-Endowed Chairs) in 2005, the GT Outstanding BS and PhD Thesis Advisor Awards, the IEEE Components, Packaging and Manufacturing Technology Field Award in 2006 (hailed by the IEEE as "Father of Modern Semiconductor Packaging"), the Sigma Xi's Monie Ferst Outstanding Educational Award in 2007, the Society of Manufacturing Engineers' Total Excellence in Electronic Manufacturing Award in 2008 and the IEEE CPMT David Feldman Award and the Pennsylvania State University Distinguished Alumni Award in 2009.

Prof. Wong served as CPMT Society President in 1992 and 1993, and is currently Chair of the CPMT Society Fellow Evaluation Committee.

He holds over 50 U.S. patents, and has published over 1,000 technical papers, co-authored and edited 10 books and is a member of the National Academy of Engineering of the USA since 2000.

Additionally, the following individuals were appointed to fill interm vacancies as Members-at-Large:

DANIEL LU (S'98, M'00, SM'04) Dr. Daniel Lu is the Technical Director of Product Development of the General Industry business unit of Henkel Corporation in China. He was the director of product development of Henkel Electronics in China for almost two years from 2008 to 2009. Prior to joining Henkel, he worked for the R&D department of Intel Corp. as a Sr. Scientist and program manager for 7 years. He also had worked for Lucent Technologies, Amoco's Electronics Materials Division, and the Electronics Materials Group of National Starch and Chemical Company before. He has extensive experience in electronic packaging and materials and processing. He received his MS and PhD degrees on Polymer Science and Engineering from Georgia Institute of Technology in 1996 and 2000, respectively. Dr. Lu received many awards including the IEEE/CPMT Outstanding Young Engineer Award in 2004, the IEEE ECTC best poster paper in 2007, Intel's most patent filing in 2003–2007, Intel Divisional Recognition Awards in 2002, 2003, and 2007, Intel most patent granting of the year for 2006 and 2007. Dr. Lu has published more than 50 technical papers, wrote chapters for five books, and holds 68 US patents. He is the editor of the book "Materials for Advanced Packaging (2008)" and co-author of the book "Electronically Conductive Adhesives with Nanotechnologies (2009)". He has been serving key roles in organizing international electronic packaging conferences and teaching professional development short courses in these conferences. Dr. Lu is a senior member of IEEE, and an associate editor of *IEEE Transactions on Components, Packaging and Manufacturing Technology* and *Journal of Nanomaterials*, and an editorial board member of *Nanoscience & Nanotechnology-Asia.*

GILLES POUPON (M'05, SM'10) Gilles Poupon received his formal education at University of Grenoble (France) and Conservatoire National des Arts et Métiers in Paris. He received his M.S. in Electrochemistry in 1985. He joined CEA-LETI, Grenoble, France in 1987 where he worked during 10 years on the development of electrode position processes for magnetic thin film heads. In this theme he has published more than 10 publications and three patents. Since 2004, Gilles is Director Strategic Program on Advanced Packaging at CEA-LETI. Subsequently, he became the Manager of the High Density Interconnection and Packaging Laboratory at LETI. He has an extensive experience in technologies relating to micro-systems packaging, 3D integration and heterogeneous integration (SiP, wafer level packaging, flip-chip, fine pitch interconnections, lead free alloys, thermal management, MEMS packaging, lead free alloys). In the course of his involvement in packaging, he worked on specific technologies based on wafer level packaging, eWLP, fine pitch & high density interconnections, TSV processes, micro-cooling (silicon heat pipes).

Gilles Poupon has been active in Electronic Packaging since 2001 and he is Senior Member of IEEE (SM'10). He is program committee member for ECTC conference (co-chair in 2011) and member of the Board of the IEEE-CPMT French branch. He has worked with other CPMT colleagues in establishing the IEEE workshops and he has been involved with membership of technical committees for ESTC, EMPC in Europe. Additionally, Gilles is the technical director of French Chapter of IMAPS since 2006 and involved on technical committee of Imaps European events. He has been nominated to be General Chair of the next EMPC conference in Grenoble in 2013. He is a Scientific Advisory of EURIPIDES (European cluster on packaging) and committee member of Smart System Integration Conference (from EPOSS network in Europe). He is also a member of ITRS Assembly & Packaging Technical Working Group and European Branch of JISSO working group. He is also member of the Electrochemical Society. Gilles has published two books on Advanced Packaging and New processes for interconnections, over 50 papers, book chapters and conference presentations and has more than 10 patents in the field of advanced packaging, micro systems technologies and 3D integration.

To see the full list of CPMT Society Board of Governors members, go to http://cpmt.ieee.org/board-of-governors.html

New IEEE CPMT Senior Members

The members listed below were recently elevated to the grade of Senior Member.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

Ahn, Choon Ki
Bakir, Muhannad
Deckman, Blythe
Georgakopoulos, Stavros
Gunturi, Satish
Harada, Takashi
Hasegawa, Makoto
Inoue, Hiroshi
Kim, Joungho
Michel, Bruno
Shang, Jintang
Wei, Lixiang
Young, Brian

CPMT Chapter News....

Orange County Chapter's All-Day Workshop on "3D Integrated Circuits"

submitted by Sam Karikalan, Chair, CPMT Orange County Chapter

The newly formed IEEE CPMT Orange County Chapter held its first ever All-day Workshop on Friday, December 9, 2011, at the Jazz Semiconductor Auditorium, Newport Beach, CA, on the topic "3D Integrated Circuits – Technologies enabling the Revolution". This workshop was attended by 163 people, coming from the wide spectrum of companies and institutions in the region, including:

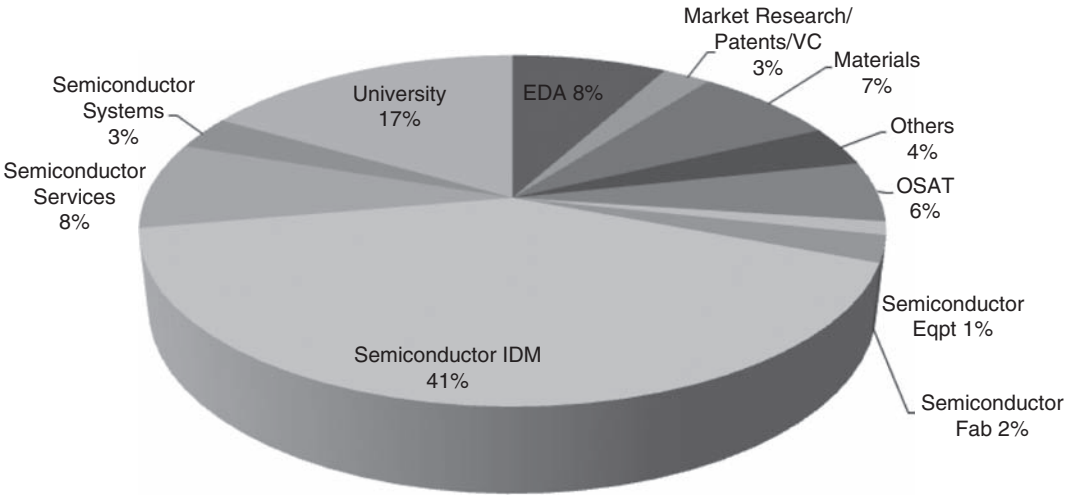
- Semiconductor Integrated Device Manufacturers (IDM) such as Broadcom, Conexant, Hynix, ISC8, Mindspeed, Peregrine, QLogic, Qualcomm, Skyworks and others
- Universities such as UC Irvine, UC San Diego, USC and Cal State Long Beach.
- EDA companies Ansys, Cadence and Mentor Graphics.
- Semiconductor Services companies such as EAG, Nu-Trek, Unisem and others.
- Material companies Henkel and Hitachi; OSAT Companies such as Amkor, SPIL and others.

The audience also included representatives of Semiconductor Fabs, Equipment makers, System Companies, Air & Space industry, Venture Capital community and Patent Attorneys in Southern California, making this first ever workshop by the chapter one of the well attended and successful regional workshops of the CPMT Society.

Workshop proceedings

The forenoon session of the workshop was on "Market, Architecture and Design" of 3D Integrated Circuits. Six invited speakers from Technology Research, Market Research, IDM and EDA branches of the 3DIC Industry presented at this session.

The first half of this session was chaired by Yokai Cheok, Director of ASIC Design at Broadcom Corporation. Prof. Muhannad Bakir of Georgia Tech was the first speaker, who presented on "Opportunities and Challenges for 3D Integrated Heterogeneous Electronic Systems". His discussion on micro-machined on-silicon heat sinks generated a lot of excitement in the audience and provided the perfect start for the workshop. Dr. Phil Garrou, Distinguished Lecturer and Past President of our Society, presented next on "Economics to drive 3D Stacking" in which he drove home the point that 3D Stacking would soon become a necessity for economics rather than just remaining as a technological path for smaller form factor and performance. Dr. Suresh Ramalingam, Senior Director from Xilinx, was the last speaker in the first half of this session, who spoke on "Stack Silicon Interconnect (SSI) – Road to Production". With Xilinx's pioneering work on commercial Through-Silicon-Interposer products, Dr. Ramalingam had to go through the longest Q&A interaction with the audience in the entire workshop.



Type of industries represented at the CPMT OC Chapter's 2011 All-Day Workshop.

Prof. Chin C Lee from UCI chaired the second half of the forenoon session. The first presenter in this half was Dr. Norman Chang, Co-Founder of Apache Design Solutions, Ansys, who spoke on "Emerging Challenges for Power, Signal and Reliability Verification on 3D-IC/Silicon Interposer Designs". Dr. Chang discussed on how some of the contemporary and upcoming tools and flows can address those design verification challenges. Dr. Stephen Pateras from Mentor Graphics presented next with his discussion on the Test Challenges, with his presentation on "3D IC Test Challenges and Solutions" that covered several DFT based test solutions. The presentation "3D Integration Challenges and Progress – From TSVs to Stacked Die Technologies" by Dr. Eric Beyne of IMEC, Belgium was the last one in the morning session of the workshop. Dr. Beyne discussed IMEC's views and work on 3D IC Applications, TSV Wafer Processing, 3D Die Stacking Approaches and the Underfill requirements.

The first half of the afternoon session was chaired by Robert Warren, Executive Director at Conexant Systems. The session began with the presentation "Cost-effective 3D Semiconductor Packaging Solutions based on Embedded Die in Laminate Technology" by Ted Tessier, Chief Technology Officer of Flip Chip International. This presentation proposed a commercially available non-TSV way of 3D stacking, jointly developed by FCI and Fujikura. Dr. Yeong Lee from STATS ChipPAC spoke next on "Challenges and Solutions in Mid-end and back-end Processes for 2.5D and 3D TSV – an OSAT Perspective", primarily focusing on thin Wafer handling challenges and solutions. Dr. Rose Guino was the third speaker in the afternoon with her presentation on "Advanced Underfills for 2.5D and 3D Applications" that focused on the Wafer-Applied Underfill Film for 3D Applications.

The second half of the afternoon session was chaired by Usama Abdali of Skyworks Solutions. In this half, Dr. GS Kim, Founder and CEO of EPWorks Ltd, Seoul, Korea presented on "3D TSV Interposer and its Applications". His presentation provided some good insight into the 3D IC Industry and its infrastructure in Korea. The last speaker of the day was David Butler, Vice President of Marketing from SPTS Technologies, Newport, UK, who presented on the "Via Reveal – High rate Si Thinning and Low temperature Dielectrics for Post-TSV Processing".

Sponsors and exhibitors

The successful organization of this all-day workshop, that was offered at a highly affordable price, wouldn't have been possible without the financial support from the area companies such as Ansys, Broadcom, Conexant, Skyworks (all Platinum Sponsors), Henkel and Sales & Service (both Gold Sponsors). While Conexant Systems had offered the workshop venue and all support services free of cost, Ansys donated the USB Flash Drives, which were used to distribute soft copies of the presentation material to all attendees. The workshop organizing committee and the OC chapter sincerely thank the above sponsors for their support. The workshop also featured displays from four exhibitors / partners, namely, EAG Labs, Mirror Semiconductors, TechSearch International and UCI. Thanks are due to them as well for their participation and help to make this workshop a big success.

Feedback from the workshop attendees, speakers and sponsors has been overwhelmingly supportive of organizing more of similar workshops every year in Orange County. There is no doubt that the OC Chapter will build on this momentum and keep raising the bar every year, in its quest to become one of the most active chapters of the CPMT Society in the world.

CPMT Past President and Distinguished Lecturer, Dr. Phil Garrou, presenting at the workshop.

CPMT OC Chapter Committee members along with some of the Workshop Speakers
Left to Right: Jianjun Li, Phil Garrou, Fan Yeung, Rose Guino, Ted Tessier, Mark Kuhlman, Wei Koh, Don Frye, Sam Karikalan, Muhannad Bakir, Aaron Edwards, Mehdi Saeidi, Robert Warren, Melissa Lau, Jaydutt Joshi.

News from IEEE CPMT France Chapter

The IEEE CPMT France Chapter has planned two events for 2012. First, the Chapter is a co-sponsor of the 2nd annual MiNaPAD Forum (Micro/Nano-Electronics Packaging and Assembly, Design and Manufacturing Forum) with IMAPS France to be held April 24–25, 2012 at the Minatec campus in Grenoble, France. Last year's MiNaPAD Forum attracted nearly 200 participants from Europe, the United States and Asia. This year, the event will begin with a workshop on Beyond 300mm organized by SEMI on April 24, followed by the conference and exhibition on April 25–26. The conference will feature three keynote speeches – from Fraunhofer Institute, Amkor and IPDIA, – and conference papers presented in two parallel sessions over the two days along with a vendor exhibition. For further information including program and registration form, please refer to the website http://france.imapseurope.org/ or contact Florence VIRETON at +33(0) 1 39 67 17 73 or by e-mail: imaps.france@imapsfrance.org.

Second, the CPMT Chapter is planning a new workshop, NanoPACK,on September 13, 2012 at the Minatec campus in Grenoble. Prof. James Morris, expert in the novel field of nanopackaging and distinguished IEEE/CMPT lecturer, will give the keynote speech. A detailed agenda and registration will be available before June 2012.

17th IEEE International Symposium for Design and Technology of Electronics Packages – SIITME 2011

submitted by Andreea Bonea, Chair of IEEE CPMT Student Branch Chapter of the Politehnica University of Bucharest, Romania

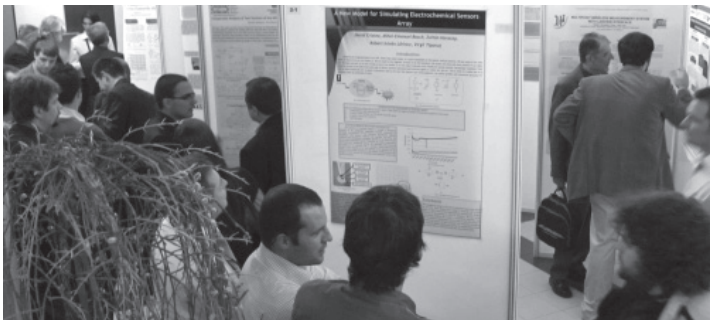
The 17th IEEE 2011 International Symposium for Design and Technology in Electronic Packaging (www.siitme.ro) is an annual Central European event in the field of electronics industry; SIITME event is technically sponsored and organized by IEEE CPMT Society Hu&Ro Joint Chapter.

The IEEE-CPMT Hu&Ro Joint Chapter is involved, through Prof. Pitică (Chair) and Prof. Illyefalvi-Vitez (Vice-Chair), in organizing the SIITME Conference. Since its first edition in 1995 it represented a scientific forum for exchanging information between academia and industry from Central and Eastern Europe on the topics related to their experimental and theoretical work in the field of electronics and micro-systems, manufacturing technologies and advanced packaging.

The beautiful town of Timişoara, the capital of Banat County, Romania hosted the 17th Edition. SIITME 2011 took place between 20th–23rd October 2011. The conference covered a variety of topics related to packaging from assembly and manufacturing technology, microsystems, advanced materials communications and power electronics.

It is generally felt that SIITME 2011 is a conference that has very good representation of young scientists, SIITME being a very proper environment for education and training of the young researcher for their future scientific life. This year various members of Academia, young scientists, students and industry attended the event. The work elaborated by research teams all over Romania or from abroad has been presented. Traditional universities such as Cluj, Iaşi, Timişoara and Bucharest, as well as emerging young universities such as Alba Iulia, Baia Mare, Galaşi, Braşov, Piteşti, Suceava and Sibiu were present through the papers of nationally and internationally renowned professors and professionals. At the event also participated well-known specialists from Germany, Hungary, Czech Republic, Poland, Spain, Turkey and USA.

The Symposium included several workshops with the purpose of creating a forum for debate on the innovation of electronic products such as: Be an entrepreneur! and three presentations of Alfa Test, which were attended, in addition to those present at SIITME,



Discussions with researchers at evaluation during Poster Session three.

by representatives of companies from Romania and Germany, companies involved in development of electronic products.

The conference commenced with the presentations given by the keynote speakers in the opening plenary, who provided an "up to date" overview of the two areas of actuality: printed electronic circuits were discussed in "Current Trends in the Automotive Industry Development" presented by Dr. Christian von Albrichsfeld, General Manager Continental Automotive Romania, Head of Research and Development Romania, as well as "Nanopackaging: Nanotechnologies in Microelectronics Packaging "presented by Prof. James E. Morris, Department of Electrical & Computer Engineering, Portland State University. The issues of electronic microsystems were regarded in the presentation "Reliable Technologies for 3D Integration" given by Prof. Klaus-Jürgen Wolter, Electronics Packaging Laboratory, Technische Universität Dresden.

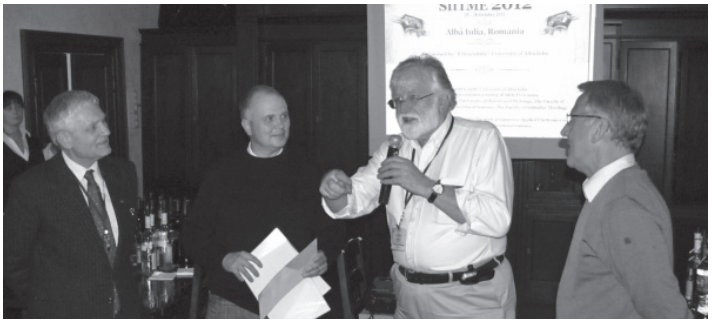
Four oral sections followed, chaired by Paul Mach, Norocel Dragos Codreanu, Zsolt Illyefalvi-Vitez, Paul Schiopu, James E. Morris, Heinz Wohlrabe, Klaus-Jürgen Wolter, Vlad Cehan, along with four poster sessions led by Dr. Ing. Heinz Wolhrabe, Dresden University of Technology. He acted, as General Poster Session Chair, involved in organizing posters evaluation criteria and the heterogeneous review teams. More than 20 evaluators were involved in the evaluation process. Each poster was evaluated by three evaluators' team, one for the short oral presentation (3 minutes), one for the poster layout impact and one for the discussion with the author.

The activities of the IEEE CPMT HU&RO Joint Chapter were the organization of the conference, both in the scientific and in technical sense, which has lead to a high level conference and a pleasant atmosphere.

SIITME 2011 was an IEEE Hu&Ro Joint Chapter Conference and, after the evaluation, the papers of the highest scientific value

The steering committee meeting at SIITME 2011.

Awarding ceremony of SIITME 2011 for Poster Presentations for Young Scientists.



Closing words (left to right): Prof. Ph. D. Paul Svasta (General Chair), Prof. Ph. D. Aurel Gontean (Conference Chair), Prof. Ph. D. James E. Morris (Keynote Speaker), Prof. Ph. D. Klaus Jurgen Wolter (Keynote Speaker, Member of International Steering Committee).

are included in the IEEE Xplore database. The members of the Steering and the scientific committees have participated at evaluation process.

At the closing ceremony, the best scientists were awarded. The General Chair of the Conference, Prof. Paul Svasta, the initiator of SIITME event, presents the awards to the participants. Best presentation award for senior scientist went to Balázs ILLÉS, Budapest University of Technology and Economics and Excellent presentation award for young scientist went to Raul FIZESAN and Rajmond JÁNÓ, Universitatea Tehnică din Cluj Napoca. Further, the Best presentation award for young scientist was received by Radu Alexandru BUNEA, Universitatea "Politehnica" din Bucureşti and Excellent poster award for senior scientist was received by Dan Tudor VUZA, Romanian Academy of Mathematics, Bucharest. Best Poster award for young scientist to Attila BONYÁR, Budapest University of Technology and Economics. Excellent poster awards for young scientist were given to Bogdan MIHĂILESCU, Universitatea "Politehnica" din Bucureşti, Cătălin NEGREA, Universitatea "Politehnica" din Timişoara, István BOSZNAI, Budapest University of Technology and Economics, Attila GÉCZY, Budapest University of Technology and Economics, Réka BÁTORFI, Budapest University of Technology and Economics.

During the cultural program of the conference, the organizers made their best efforts to give an insight into the local specialties during the wine tasting session and to present some of the surrounding sites including the historical monument "Romanian Orthodox Metropolitan Cathedral" or the "National Romanian Opera". The program presented a good opportunity for networking which forecasts future scientific collaborations.

We are eagerly anticipating the next edition held in Alba - Iulia, România, 25–28 October 2012!

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The website link is:ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

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Here are the journals we suggest you select for monitoring:

Transactions on Components, Packaging and Manufacturing Technology
Transactions on Semiconductor Manufacturing

Publication News....

Have You Read Them? The Most Downloaded CPMT Transactions Papers

What might you be missing in the CPMT literature? Following is a list of most downloaded papers in January 2012. Subscribers can access these and other papers on IEEE Xplore.

From the *Transactions on Components, Packaging and Manufacturing Technology:*

PDN Impedance Modeling and Analysis of 3D TSV IC by Using Proposed P/G TSV Array Model Based on Separated P/G TSV and Chip-PDN Models

Jun So Pak; Joohee Kim; Jonghyun Cho; Kiyeong Kim; Taigon Song; Seungyoung Ahn; Junho Lee; Hyungdong Lee; Kunwoo Park; Joungho Kim; Issue Date: Feb 2011 Page(s): 208–219

The impedance of a power-distribution network (PDN) in three-dimensionally stacked chips with multiple through-silicon-via (TSV) connections (a 3D TSV IC) was modeled and analyzed using a power/ground (P/G) TSV array model based on separated P/G TSV and chip-PDN models at frequencies up to 20 GHz. The proposed modeling and analysis methods for the P/G TSV and chip-PDN are fundamental for estimating the PDN impedances of 3D TSV ICs because they are composed of several chip-PDNs and several thousands of P/G TSV connections. Using the proposed P/G TSV array model, we obtained very efficient analyses and estimations of 3D TSV IC PDNs, including the effects of TSV inductance and multiple-TSV inductance, depending on P/G TSV arrangement and the number of stacked chip-PDNs of a 3D TSV IC PDN. Inductances related to TSVs, combined with chip-PDN inductance and capacitance, created high upper peaks of PDN impedance, near 1 GHz. Additionally, the P/G TSV array produced various TSV array inductance effects on stacked chip-PDN impedance, according to their arrangement, and induced high PDN impedance, over 10 GHz.

Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring

Jonghyun Cho; Eakhwan Song; Kihyun Yoon; Jun So Pak; Joohee Kim; Woojin Lee; Taigon Song; Kiyeong Kim; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Minsuk Suh; Kwangyoo Byun; Joungho Kim; Issue Date: Feb 2011 Page(s): 220–233

In three-dimensional integrated circuit (3D-IC) systems that use through-silicon via (TSV) technology, a significant design consideration is the coupling noise to or from a TSV. It is important to estimate the TSV noise transfer function and manage the noise-tolerance budget in the design of a reliable 3D-IC system. In this paper, a TSV noise coupling model is proposed based on a three-dimensional transmission line matrix method (3D-TLM). Using the proposed TSV noise coupling model, the noise transfer functions from TSV to TSV and TSV to the active circuit can be precisely estimated in complicated 3D structures, including TSVs, active circuits, and shielding structures such as guard rings. To validate the proposed model, a test vehicle was fabricated using the Hynix via-last TSV process. The proposed model was successfully verified by frequency- and time-domain measurements. Additionally, a noise isolation technique in 3D-IC using a guard ring structure is proposed. The proposed noise isolation technique was also experimentally demonstrated; it provided –17 dB and –10 dB of noise isolation between the TSV and an active circuit at 100 MHz and 1 GHz, respectively.

High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)

Joohee Kim; Jun So Pak; Jonghyun Cho; Eakhwan Song; Jeonghyeon Cho; Heegon Kim; Taigon Song; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Min-Suk Suh; Kwang-Yoo Byun; Joungho Kim; Issue Date: Feb 2011 Page(s): 181–195

We propose a high-frequency scalable electrical model of a through silicon via (TSV). The proposed model includes not only the TSV, but also the bump and the redistribution layer (RDL), which are additional components when using TSVs for 3-D integrated circuit (IC) design. The proposed model is developed with analytic *RLGC* equations derived from the physical configuration. Each analytic equation is proposed as a function of design parameters of the TSV, bump, and RDL, and is therefore, scalable. The scalability of the proposed model is verified by simulation from the 3-D field solver with parameter variations, such as TSV diameter, pitch between TSVs, and TSV height. The proposed model is experimentally validated through measurements up to 20 GHz with fabricated test vehicles of a TSV channel, which includes TSVs, bumps, and RDLs. Based on the proposed scalable model, we analyze the electrical behaviors of a TSV channel with design parameter variations in the frequency domain. According to the frequency-domain analysis, the capacitive effect of a TSV is dominant under 2 GHz. On the other hand, as frequency increases over 2 GHz, the inductive effect from the RDLs becomes significant. The frequency dependent loss of a TSV channel, which is capacitive and resistive, is also analyzed in the time domain by eye-diagram measurements. Due to the frequency dependent loss, the voltage and timing margins decrease as the data rate increases.

High-Frequency Modeling of TSVs for 3-D Chip Integration and Silicon Interposers Considering Skin-Effect, Dielectric Quasi-TEM and Slow-Wave Modes

Ndip, I.; Curran, B.; Lobbicke, K.; Guttowski, S.; Reichl, H.; Lang, K.-D.; Henke, H.; Issue Date: Oct 2011 Page(s): 1627–1641

Through-silicon vias (TSVs) in low, medium and high resistivity silicon for 3-D chip integration and interposers are modeled and thoroughly characterized from 100 MHz to 130 GHz, considering the slow-wave, dielectric quasi-TEM and skin-effect modes. The frequency ranges of these modes and their transitions are predicted using resistivity-frequency domain charts. The impact of the modes on signal integrity is

quantified, and three coaxial TSV configurations are proposed to minimize this impact. Finally, conventional expressions for calculating the per-unit-length circuit parameters of transmission lines are extended and used to analytically capture the frequency dependent behavior of TSVs, considering the impact of the mixed dielectric (silicon dioxide-silicon-silicon dioxide) around the TSVs. Excellent correlation is obtained between the analytical calculations using the extended expressions and electromagnetic field simulations up to 130 GHz. These extended expressions can be implemented directly in electronic design automation tools to facilitate performance evaluation of TSVs, prior to system design.

Low-Power and Reliable Clock Network Design for Through-Silicon Via (TSV) Based 3D ICs

Xin Zhao; Minz, J.; Sung Kyu Lim; Issue Date: Feb 2011 Page(s) 247–259

This paper focuses on low-power and low-slew clock network design and analysis for through-silicon via (TSV) based three-dimensional stacked ICs (3D ICs). First, we investigate the impact of the TSV count and the TSV resistance-capacitance (RC) parasitics on clock power consumption. Several techniques are introduced to reduce the clock power consumption and slew of the 3D clock distribution network. We analyze how these design factors affect the overall wire length, clock power, slew, and skew in 3D clock network design. Second, we develop a two-step 3D clock tree synthesis method: 1) 3D abstract tree generation based on the three-dimensional method of means and medians (3D-MMM) algorithm; 2) buffering and embedding based on the slew-aware deferred-merge buffering and embedding (sDMBE) algorithm. We also extend the 3D-MMM method (3D-MMM-ext) to determine the optimal number of TSVs to be used in the 3D clock tree so that the overall power consumption is minimized. Related SPICE simulation indicates that: 1) a 3D clock network that uses multiple TSVs significantly reduces the clock power compared with the single-TSV case, 2) as the TSV capacitance increases, the power savings of a multiple-TSV clock network decreases, and 3) our 3D-MMM-ext method finds a close-to-optimal design point in the "TSV count versus power consumption" tradeoff curve very efficiently.

From the *Transactions on Components and Packaging Technologies:*

Dynamic Lithium-Ion Battery Model for System Simulation

Lijun Gao; Shengyi Liu; Dougal, R.A.; Issue Date: Sep 2002 Page(s): 495–505

Presents here a complete dynamic model of a lithium ion battery that is suitable for virtual-prototyping of portable battery-powered systems. The model accounts for nonlinear equilibrium potentials, rate- and temperature-dependencies, thermal effects and response to transient power demand. The model is based on publicly available data such as the manufacturers' data sheets. The Sony US18650 is used as an example. The model output agrees both with manufacturer's data and with experimental results. The model can be easily modified to fit data from different batteries and can be extended for wide dynamic ranges of different temperatures and current rates.

Analytical and Numerical Modeling of the Thermal Performance of Three-Dimensional Integrated Circuits

Jain, A.; Jones, R.E.; Chatterjee, R.; Pozder, S. Issue Date: Mar 2010 Page(s): 56–63

Three-dimensional (3D) interconnection technology offers several electrical advantages, including reduced signal delay, reduced interconnect power, and design flexibility. 3D integration relies on through-silicon vias (TSVs) and the bonding of multiple active layers to stack several die or wafers containing integrated circuits (ICs) and provide direct electrical interconnection between the stacked strata. While this approach provides several electrical benefits, it also offers significant challenges in thermal management. While some work has been done in the past in this field, a comprehensive treatment is still lacking. In the current work, analytical and finite-element models of heat transfer in stacked 3D ICs are developed. The models are used to investigate the limits of thermal feasibility of 3D electronics and to determine the improvements required in traditional packaging in order to accommodate 3D ICs. An analytical model for temperature distribution in a multidie stack with multiple heat sources is developed. The analytical model is used to extend the traditional concept of a single-valued junction-to-air thermal resistance in an IC to thermal resistance and thermal sensitivity matrices for a 3D IC. The impact of various geometric parameters and thermophysical properties on thermal performance of a 3D IC is investigated. It is shown that package and heat sink thermal resistances play a more important role in determining temperature rise compared to thermal resistances intrinsic to the multidie stack. The improvement required in package and heat sink thermal resistances for a 3D logic-on-memory implementation to be thermally feasible is quantified. An increase in maximum temperature in a 3D IC compared to an equivalent system-in-package (SiP) is predicted. This increase is found to be mainly due to the reduced chip footprint. The increased memory die temperature in case of memory-on-logic integration compared to a SiP implementation is identified to be a significant thermal management challenge in the future. The results presented in this paper may be useful in the development of thermal design guidelines for 3D ICs, which are expected to help maximize the electrical benefits of 3D technology without exacerbating thermal management issues when implemented in early-stage electrical design and layout tools.

From the *Transactions on Advanced Packaging:*

Waveform Relaxation Time Domain Solver for Subsystem Arrays

Antonini, G.; Ruehli, A.E. Issue Date: Jan 2011 Page(s): 760–768

In this paper we present a waveform relaxation approach for the transient analysis of 3-D electromagnetic problems using the partial element equivalent circuit (PEEC) method. Relying on weaker couplings among separated systems, a waveform relaxation scheme is proposed to accelerate the transient analysis of large electromagnetic problems. The results are compared with those obtained using a conventional PEEC formulation. They exhibit a significant speed-up while preserving the solution accuracy.

A Flexible Time-Stepping Scheme for Hybrid Field-Circuit Simulation Based on the Extended Time-Domain Finite Element Method

Rui Wang; Jian-Ming **Jin** Issue Date: Nov 2010 Page(s): 769–776

Microelectronics packaging technology has evolved from through-hole and bulk configuration to surface-mount and small-profile ones. In surface mount packaging, such as flip chips, chip scale packages, and ball grid arrays, chips/packages are attached to the substrates/printed wiring board (PWB) using solder bump interconnections. Solder bumps hidden between the chips/packages and the substrate/board are no longer visible for inspection. A novel solder bump inspection system has been developed using laser ultrasound and interferometer techniques. This system has been successfully applied to detect solder bump defects including missing, misaligned, open, and cracked solder bumps in flip chip packages, chip scale packages and land grid arrays. The system uses a pulsed Nd:YAG laser to induce ultrasound in the thermoelastic regime and the transient out-of-plane displacement response in nanometer scale on the package surface is measured using the interferometer technique. In this paper, wavelet analysis of laser ultrasound signals is presented and compared to previous signal processing methods, such as error ratio and correlation coefficient. The results show that wavelet analysis increases measurement sensitivity for inspecting solder bumps in electronic packages. Laser ultrasound inspection results are also compared to X-ray results. In particular, this paper discusses defect detection for a 6.35 mm ?? 6.35 mm ?? 0.6 mm PB18 flip chip package and flip chip package (??SiMAF??) with 24 lead-free solder bumps. These two types of flip chip specimens are both nonunderfilled.

From the *Transactions on Electronics Packaging Manufacturing:*

Acid Decapsulation of Epoxy Molded IC Packages With Copper Wire Bonds

Murali, S. Srikanth, N. Issue Date: July 2006 Page(s): 179–183

Epoxy molded IC packages with copper wire bonds are decapsulated using mixtures of concentrated sulfuric acid (20%) and fuming nitric acid in an automatic decapping unit and, observed with minimal corrosion of copper wires (0.8-6 mil sizes) and bond interfaces. To attain maximum cross-linking of the molded epoxies, the post mold cured packages (175 ºC for 4 h) were further, aged at high temperature of 150 ºC for 1000 h. These packages are decapsulated using mixtures of higher ratio of concentrated sulfuric acid (40%) along with fuming nitric acid. The shear strength of copper wire bonds with 1 mil (25 mum) diameter of the decapsulated unit is higher than 5.5 gf/mil^2. The present study shows copper stitch bonds to Au, Cu, Pd, and Sn alloy plated surfaces are less affected on decapping, with a few grams of breaking load on stitch pull test, while stitch bonds on silver plated surfaces reveal lifting of wire bonds on decapping.

The Changing Automotive Environment: High-Temperature Electronics

Johnson, R.W.; Evans, J.L.; Jacobsen, P.; Thompson, J.R.; Christopher, M. Issue Date: July 2004 Page(s): 164–176

The underhood automotive environment is harsh and current trends in the automotive electronics industry will be pushing the temperature envelope for electronic components. The desire to place engine control units on the engine and transmission control units either on or in the transmission will push the ambient temperature above 125°C. However, extreme cost pressures, increasing reliability demands (10 year/241 350 km) and the cost of field failures (recalls, liability, customer loyalty) will make the shift to higher temperatures occur incrementally. The coolest spots on engine and in the transmission will be used. These large bodies do provide considerable heat sinking to reduce temperature rise due to power dissipation in the control unit. The majority of near term applications will be at 150°C or less and these will be worst case temperatures, not nominal. The transition to X-by-wire technology, replacing mechanical and hydraulic systems with electromechanical systems will require more power electronics. Integration of power transistors and smart power devices into the electromechanical actuator will require power devices to operate at 175°C to 200°C. Hybrid electric vehicles and fuel cell vehicles will also drive the demand for higher temperature power electronics. In the case of hybrid electric and fuel cell vehicles, the high temperature will be due to power dissipation. The alternates to high-temperature devices are thermal management systems which add weight and cost. Finally, the number of sensors in vehicles is increasing as more electrically controlled systems are added. Many of these sensors must work in high-temperature environments. The harshest applications are exhaust gas sensors and cylinder pressure or combustion sensors. High-temperature electronics use in automotive systems will continue to grow, but it will be gradual as cost and reliability issues are addressed. This work examines the motivation for higher temperature operation, the packaging limitations even at 125°C with newer package styles and concludes with a review of challenges at both the semiconductor device and packaging level as temperatures push beyond 125°C.

Conference News....

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  - Plenary Session – Photonics: The Next Frontier?
  - CPMT Seminar – Advanced Coreless Package Substrate and Material Technologies
  - Special Tuesday Session – Next Generation Packaging and Integration: The Transformed Role of the Packaging Foundry

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Symposium on Design, Test, Integration & Packaging of MEMS/MOEMS

Cannes, Côte d'Azur, France – 25–27 April 2012

HTTP://CMP.IMAG.FR/CONFERENCES/DTIP/DTIP2012

Chair: Bernard COURTOIS, CMP Grenoble, France
Co-Chair: Jean-Michel KARAM, MEMSCAP, Bernin, France

This Symposium will be a follow-up to the very successful issues held in 1999 and 2000 in Paris and in 2001, 2002 and 2003 in Mandelieu-La Napoule, in 2004 and 2005 in Montreux, Switzerland in 2006, in 2007 in Stresa, Italy, in 2008 in Nice, France, in 2009 in Rome, Italy in 2010 in Seville, Spain and Aix-en-Provence, France in 2011. This series of Symposia is a unique single-meeting event expressly planned to bring together participants interested in manufacturing microstructures and participants interested in design tools to facilitate the conception of these microstructures. Again, a special emphasis will be put on the very crucial needs of MEMS/MOEMS in terms of packaging solutions. The goal of the Symposium is to provide a forum for in-depth investigations and interdisciplinary discussions involving design, modeling, testing, micromachining, microfabrication, integration and packaging of structures, devices, and systems.

TECHNICAL PROGRAMME will include oral talks, poster presentations, a panel discussion and invited speakers. Special Sessions are also expected.

INVITED SPEAKERS:

Using MEMS to Build the Device and the Package – Thomas W. KENNY, Stanford Univ., USA
There has been interest in MEMS Resonators for more than 40 years, including discussion of their uses frequency references. Unfortunately, the performance of MEMS resonators for these applications has always been limited by drift in frequency, which comes from the temperature coefficient of the modulus of Silicon, as well as the role of adsorbed molecules from the environment of the resonator and other nefarious effects. The presentation will discuss a wafer-scale MEMS encapsulation process that enables a solution to many of these problems with MEMS resonators.

Integrated MEMS Using Adhesive Bonding and Other Methods – Masayoshi ESASHI, Tohoku Univ., Japan
Integrated MEMS for multiband wireless systems and so on have been developed by wafer level bonding of MEMS structures as filters and switches on LSI.

MEMS Integration for Smart Medical Devices: Opportunities and Challenges – Martin DETERRE, Sorin Group, France
In the insatiable quest for miniaturization, improved performance, novel sensing and treatment capabilities, implantable medical devices are now required to integrate micronano systems. As they enter the biomedical world, MEMS are facing new challenges such as biocompatibility, perpetual reliability and extended life span. The talk will discuss how these disciplines are now converging to broaden the scope of perspectives for healthcare devices, paving the way to innovative treatments and life-improving implantable smart sensors.

SPECIAL SESSIONS

Special Session of **bio-MEMS/NEMS** – organized by **Gou-Jen WANG**, National ChungHsing Univ., Taiwan.
The Special session of bio-MEMS/NEMS puts together papers on both theoretical analysis and on practical applications of MEMS and NEMS in biomedicine and biochemistry. General topics of interest include design, characterization, modeling, and fabrication of biomedical devices, miniaturized analytic devices, dynamics of fluids in micro channels, Tissue engineering, and others.

Special Session on **Low Temperature Cofired Ceramic for MEMS** – organized by **Marc DESMULLIEZ**, Heriot-Watt Univ., Edinburgh, UK.
Over the years, recent advances have been made in the use of ceramic green tapes for the 3D manufacturing of microsystems. These include microfluidic channels, pressure sensors, actuators alongside their electronic circuitry, all within the same platform. This special session will review the advances made on low temperature cofired ceramic (LTCC) based MEMS and the components, devices and systems built with such a platform in the MEMS area.

The CAD, Design and Test Conference will bring together researchers, engineers and practitioners involved in the development of CAD tools and design methodologies for MEMS and MOEMS. The participants will also have the opportunity to interact with the other Conference by the means of plenary talks.

The Microfabrication, Integration and Packaging Conference will bring together researchers, engineers and practitioners involved in the development of integration technologies and packaging for MEMS and MOEMS. The participants will also have the opportunity to interact with the other Conference by the means of plenary talks.

16th IEEE WORKSHOP ON SIGNAL AND POWER INTEGRITY

http://www.create.unina.it/spi2012/?who=home

Title History (1997–2011): Workshop on Signal Propagation on Interconnects

PRESENTATION

During the last fifteen years, this Workshop has been developed into a forum of exchange on the latest research and developments in the field of interconnect modeling, simulation and measurement at chip, board, and package level. The workshop is also meant to bring together developers and researchers from industry and academia in order to encourage cooperation.

The symposium will include both oral and poster sessions. In addition, a number of prominent experts will be giving keynote lectures and tutorials on areas of emerging interest. The official language is English.

TOPICS

Signal Integrity
High-Speed Interconnects and high-speed channels
Power Integrity/ Ground Noise
Power Distribution Networks
Electronic packages and microsystems
3D technologies for ICs and packages
RF, Microwave packaging and mixed signal systems
Nano-Interconnects and nano-structures
Electromagnetic Theory and Modeling
Transmission Line Theory and Modeling
Macro-Modeling, reduced-order models
Advanced Simulation Tools for Signal and Power Integrity
Electromagnetic Compatibility
Coupling Effects on Interconnects
Radiation & Interference
Testing & Interconnects
Time and Frequency Domain Measurement Techniques

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IMPACT 2012

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Call for Paper until June 15

IMPACT 2012 as the seventh conference, jointly organized by IEEE CPMT-Taipei, ITRI, IMAPS-Taiwan and TPCA and co-organized by SMTA, ISU and TTMA will be held in conjunction with TPCA Show at Taipei Nangang Exhibition Center. To construct a complete spectrum of technology trends, the theme of IMPACT 2012 highlights "IMPACT, Inspiring Innovation" and will present invited talks, workshop, industrial sessions and selected paper presentations. IMPACT conference is acknowledged for its intense connection between industries and academia. You are encouraged to submit your papers to IMPACT online data pool and enjoy the global packaging feast.

Date: October 24 (Tues) – October 26 (Fri), 2012

Venue: Taipei Nangang Exhibition Hall, Taipei, Taiwan

Exhibition: TPCA Show 2012

Theme: ***IMPACT, Inspiring Innovation***

PAPER SUBMISSION

ELECTRONIC SUBMISSION REQUIRED. The 400–500 words **ABSTRACT** should be submitted electronically through the conference website http://www.impact.org.tw/2012/General/by June 15, 2012. The **FULL-PAPER** (4 pages including figures and tables) should be submitted electronically by August 15, in case the abstract has been accepted.

Item	Date	Remark
Abstract Submission	**June 15**, 2011	400–500 words Submit on-line through conference website
Abstract Acceptance Notification	**July 10**, 2011	Notice sent via email
Full Paper Submission (Camera-ready Version)	August 15, 2011	4 pages including figures and tables Submit on-line through conference website
Presentation Material Submission(Oral Presentation)	October 1, 2011	15 minutes presentation plus 3 minutes Q&A (Totals to 18 minutes) Please email to the service@impact.org.tw

QUESTIONS ON PAPER SUBMISSION

Requests for information about the Symposia should be directed to:

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CALL FOR PAPERS

IEEE CPMT Symposium Japan 2012 ***(Formerly VLSI Packaging Workshop in Japan)***

10–12 December 2012 MIYAKO-MESSE, Kyoto, JAPAN http://www.vlsi-pkg-ws.org

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"IEEE CPMT Symposium Japan" is a well-known international symposium for advanced packaging technologies, started as "The VLSI Packaging Workshop in Japan" in 1992 and held every two years. It will provide component, packaging, and manufacturing researchers who are extending their activities beyond borders with opportunities to exchange technical knowledge and perspective. The committee strongly encourages you to attend this symposium and participate in the discussion, to understand the technology trends and find the best targets for your technology / business development.

Bring your latest research results and share with the participants who are experts from the industry and the academia, and discuss with them. Anybody contributing to the achievement of a sustainable society through electronics is very welcome at this symposium.

Topics of Interest include:

- Optoelectronics Packaging and Subsystems
- Packaging for Automobile
- Packaging for Sensors, MEMS, and Bio Devices
- RF Components & Modules / RF Tags
- 3D Packaging & Chip on Chip
- Advanced Fine Pitch Packaging
- Assembly and Packaging Challenges for Cu/Low-k Chips
- Board-Level Integration
- Integrated Substrate
- Micro Bumping Technology, Wafer Level CSP
- Laminated Materials & Processing
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- Nanotechnology, Emerging Technologies
- Electrical Performance and Thermal Management
- Board Level Reliability
- Failure Mechanisms & Reliability Improvement

You are invited to submit a 500-word abstract with figures to the program chairs by e-mail. Acceptance will be noticed by 10 August 2012. You can download the abstract submission form this web. Accepted authors are requested to submit the manuscript by 25 October 2012 for the Technical Digest, which will be referred via IEEE Explore.

Abstract Due: 29 June 2012

Submit to:

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General Chair: Jerry Broz, Ph.D.; (303) 885-1744; jerry.broz@swtest.org

Technical Program Chair: Rey Rincon; (214) 402-6248; rey.rincon@freescale.com

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http://www.semi.org/node/37811

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The 2012 committee, co-chaired by Jennifer Braggin, Entegris and Larry Pulvirent, GLOBALFOUNDRIES, has organized a conference centered around the practical applications of advanced semiconductor manufacturing strategies and methodologies. With its unique focus on the many benefits of collaboration within the manufacturing supply chain, ASMC is one conference not to miss. Register now!

Keynotes:
– Michael Campbell, Sr. Vice President, Engineering, Qualcomm
–Andrea Lati, Principal Analyst, VLSI Research, Inc.

Panel: Competing for R&D Dollars – Funding the Future
Tutorial: Advanced Device Design (FinFets) – E.J. Nowak, Distinguished Engineer, IBM Microelectronics

Workshop: Workforce Development

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E-mail: eurosime@astefo.com
URL: http://www.eurosime.org/

Name: 2012 Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP 2012)
Dates: May 25–27, 2012
Location: Cannes, France
Contact: Chantal Bénis-Morel,
E-mail: chantal.benis@imag.fr
URL: http://cmp.imag.fr/conferences/dtip/dtip2012/

Name: 2012 35th International Spring Seminar on Electronics Technology (ISSE 2012)
Dates: May 9–13, 2012
Location: Bad Aussee, Austria
E-mail: isse2012@tuwien.ac.at
URL: http://isse2012.tuwien.ac.at/

Name: 2012 16th IEEE Workshop on Signal Propagation on Interconnects (SPI 2012)
Dates: May 13–16, 2012
Location: Sorrento, Italy
Contact: Mariella Vetrano,
E-mail: m.vetrano@create.unina.it
URL: http://www.create.unina.it/spi2012/

Name: 2012 SEMI Advanced Semiconductor Manufacturing Conference (ASMC 2012)
Dates: May 15–17, 2012
Location: Saratoga Springs, NY USA
Contact: Margaret Kindling, SEMI
E-mail: mkindling@semi.org
URL: http://www.semi.org/node/37811

Name: 2012 62nd Electronic Components and Technology Conference (ECTC 2012)
Dates: May 29–June 1, 2012
Location: San Diego, CA USA
Contact: Wolfgang Sauter,
E-mail: wsauter@us.ibm.com
URL: www.ectc.net

Name: 2012 Thirteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm 2012)
Dates: May 30–June 1, 2012
Location: San Diego, CA USA
Contact: Sandeep Tonapi
E-mail: sandeep.tonapi@anveshak.com
URL: http://www.ithermconference.org/

Name: 2012 22nd IEEE Semiconductor Wafer Test Workshop (SWTW 2012)
Dates: June 10–13, 2012
Location: San Diego, CA USA
Contact: Maddie Harwood,
E-mail: maddie@cemamerica.com
URL: http://www.swtest.org/index.html

Name: 2012 4th Asia Symposium on Quality of Electronic Design (ASQED 2012)
Dates: July 3–4, 2012
Location: Kuala Lumpur, Malaysia
Contact: Ali Iranmanesh
E-mail: alii@isqed.org
URL: www.isqed.org

Name: 2012 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2012)
Dates: August 13–16, 2012
Location: Guilin, China
E-mail: empt-cie@sohu.com
URL: http://www.icept.org

Name: 2012 57th IEEE Holm Conference on Electrical Contacts (HOLM 2012)
Dates: September 11–14, 2011
Location: Minneapolis, MN USA
Contact: Deidre Zeigler,
E-mail: d.zeigler@ieee.org
URL: http://www.ewh.ieee.org/soc/cpmt/tc1

Name: 4th Electronics System Integration Technology Conferences (ESTC 2012)
Dates: September 17–20, 2012
Location: Amsterdam, The Netherlands
E-mail: estc@medicongress.com

Name: 2012 18th Int'l Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2012)
Dates: September 25–27, 2012
Location: Budapest, Hungary
Contact: Marta Rencz,
E-mail: rencz@bme.eet.hu
URL: http://therminic.eu/therminic2012

Name: 2012 34th Annual Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD 2012)
Dates: September 9–14, 2012

Location:	Tucson, AZ USA
Contact:	Lisa Pimpinella
E-mail:	lpimpinella@esda.org
URL:	http://www.esda.org/symposia.html
Name:	2012 IEEE/CPMT Workshop on Accelerated Stress Testing & Reliability (ASTR 2012)
Dates:	October 17–19, 2012
Location:	Toronto, Canada
Contact:	Kirk Gray
E-mail:	kirk@acceleratedreliabilitysolutions.com
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Name:	2012 7th Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2012)
Dates:	October 24–26, 2012
Location:	Taipei, Taiwan
E-mail:	service@impact.org.tw
URL:	http://www.impact.org.tw/2012/General/
Name:	2012 21st IEEE Electrical Performance of Electronic Packaging (EPEP 2012)
Dates:	October 21–24, 2012
Location:	Tempe, AZ USA
Contact:	Mandy Wisehart
E-mail:	epeps-admin@illinois.edu
URL:	http://epeps.ece.illinois.edu/
Name:	2012 IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS 2012)
Dates:	December 9–11, 2012
Location:	Taipei, Taiwan
E-mail:	ctshih@tl.ntu.edu.tw
URL:	http://edaps2012.ntu.edu.tw/

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2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

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