



Components, Packaging, and Manufacturing Technology Society Newsletter



THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

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President's Column....



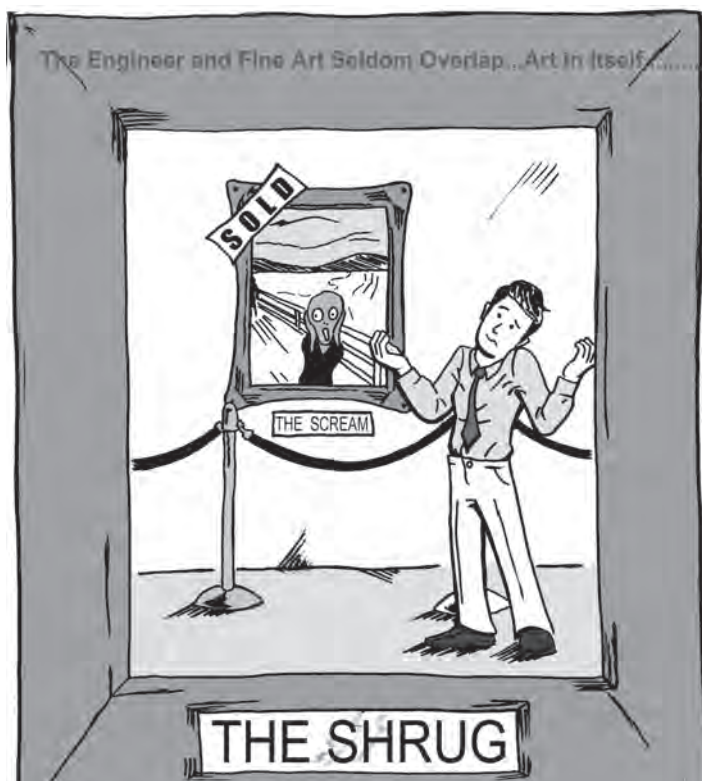
Prof. S. W. Ricky Lee
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During the 62nd ECTC at San Diego, a few friends “complained” to me they were tired of my one-n-only official photo in the ECTC Program, which also appeared in the President’s Column of the last CPMT Newsletter. Therefore, I decided to use a different style of photo in this issue. I hope you like it this way.

In the last President’s Column, I quoted Gautama Buddha “Thousands of candles can be lit from a single candle, and the life of the candle will not be shortened. Happiness never decreases by being shared.” I also said “I look forward to seeing many more candles in our future CPMT events.” Unfortunately, I lost my mother a few days before ECTC. I avoided most of parties and gatherings (except the Gala Reception on Thursday) during the mourning period. Therefore, I was not able to meet with many of you in ECTC. I hope to catch up in the upcoming conferences and identify more *candles* in our community. By the way, I would also like to encourage you to spend as much time as possible with your parents when you still can.

As promised in the last Column, I would like to talk about my **VISIONS** this time. CPMT is one of the 38 technical societies within IEEE, which was established for the advancement of Components, Packaging, and Manufacturing Technology. The official statement for its field of interest covers “*materials, component parts, modules, hybrids and micro-electronic systems for all electronics applications, as they apply in design and manufacturing,*” which can be seen at the IEEE website and in many other CPMT documents. Since the meaning is crystal clear, I think there is no

(continued on page 3)



NEWSLETTER SUBMISSION DEADLINES:

1 August 2012 for Fall issue
1 November 2012 for Winter issue
1 February 2013 for Spring issue
1 May 2013 for Summer issue

Submit all material to nsltr-input@cpmt.org

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Chapters and Student Branches

Refer to cpmt.ieee.org for CPMT Society Chapters and Student Branches list

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President's Column.... (cont.)

need for me to elaborate on these technical terms any further. Therefore, I would like to change the direction and try to envision our CPMT Society from the perspective of secular humanism.

During the President's report in the CPMT Society Board of Governors (BoG) meeting right after ECTC, I proposed a new branding slogan to the BoG members: CPMT – *Connecting People, Mentoring Talents!* This is a tagline coherent to the *Values* (connection, information, publication, and recognition) and the concept of *Candles* that I mentioned last time. I received very good responses from the BoG members on this proposal. One even suggested we might consider putting this tagline on our society webpage. Nevertheless, later on I realized that "Connecting People" has been a business slogan adopted by Nokia since 1993. Obvi-

ously, it is inappropriate to use this one. On the other hand, since CPMT is a technical society for professional peers in the same field of interest, I figured it may be even better to use "Peers" to replace "People." Therefore, I would like to propose the following modified tagline to you: CPMT – *Connecting Peers, Mentoring Talents!* Yes, these are my **VISIONS** about CPMT. I wish CPMT could serve as an effective platform to link professional peers with the same field of interest and to foster talented minds in our community for the purpose of *Advancing Technology for Humanity*, the tagline of IEEE!

Please join me to spread the words and promote CPMT by chanting "*Connecting Peers, Mentoring Talents*" in our future events. Thank you!

CPMT Society News....

E-Mail Alias And IEEE Web Account Needed 2012 CPMT Society Board of Governors Election On-Line

In order to vote in this year's CPMT Board of Governors election, members will need to have a valid e-mail alias on record with IEEE and also have an IEEE Web Account.

Eligible voting members will receive notification by e-mail in the Fall of this year with instructions for voting on-line. You will need an IEEE Web Account to access the ballot and cast your vote. This Web Account is the same one you may use for IEEE services such as renewing membership and accessing IEEE Xplore.

If you do not recall your Web Account username and password, or aren't sure whether you have established an account, please go to <http://www.ieee.org/web/accounts> to recover your password or establish a new account.

Please be sure to update your IEEE membership record with your current e-mail alias. If you DO NOT HAVE AN E-MAIL address or would prefer to receive a paper ballot by mail, please send your name, mailing address and IEEE Member Number by 24 August to:



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New IEEE CPMT Senior Members

The members listed below were recently elevated to the grade of Senior Member.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

Marc Desmulliez
David DiPaola
John W Elmer
Xun Luo

Hasan Sharifi
Katsuyuki Sakuma
Jong-Gwan Yook

Mauro J Walker Receives 2012 IEEE Components, Packaging and Manufacturing Technology Award

The IEEE Components, Packaging and Manufacturing Technology Award, sponsored by the IEEE Components, Packaging and Manufacturing Technology Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies.

The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

The 2012 Award was presented to Mauro J Walker at the 62nd Electronic Components and Technology Conference, May 2012.



Mauro J Walker

Senior Vice President and Director of Manufacturing, Motorola (Retired), Ocean Ridge, FL, USA

For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations.

Mauro J Walker's contributions to advancing electronics manufacturing technology helped place Motorola and the United States as leading high-volume manufacturers of portable electronic devices.

Mr. Walker's leadership during the 1970s and 1980s drove the advanced technology necessary for miniaturization of portable communications such as pagers, two-way radios, and cell phones. At a time when the U.S. electronics industry was lagging Japan, Walker raised Motorola's in-house microelectronics capabilities for packaging and assembly of semiconductor devices, propelling it to an industry leader. He established advanced manufacturing technology centers within Motorola, producing many innovations including high-speed surface-mount chip assembly. Mr. Walker was the founding chairman of the National Electronic Manufacturing Initiative (NEMI), representing over 60 electronic equipment manufacturers to improve the competitiveness of North American electronics manufacturing companies. With Walker's vision, NEMI went international (now known as iNEMI) as the only global organization integrating the roadmap

needs for all major technologies required for electronics manufacturing. An IEEE Life Fellow, Mr. Walker retired from Motorola, Inc. in 1998 as senior vice president and director of manufacturing. He currently resides in Ocean Ridge, Fla.

Mauro Walker joins the following past recipients of this Award.

2011 – Rao R. Tummala

"For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging."

2010 – Herbert Reichl

"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

2009 – George G. Harman

"For achievements in wire bonding technologies."

2008 – Karl Puttlitz Sr. and Paul A. Totta

"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages"

2007 – Dimitry Grabbe

"For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

2006 – C. P. Wong

"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005 – Yutaka Tsukada

"For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004 – John W. Balde

"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit <http://www.ieee.org/awards>

Congratulations to 2012 CPMT Award Winners

The CPMT Society annually recognizes individuals for contributions to the profession through technical achievements, service to the industry and to the Society. The following individuals received their awards at the 62nd Electronic Components and Technology Conference (ECTC), May 2012.

The **David Feldman Outstanding Contribution Award** is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions. The 2012 recipient:



Philip E. Garrou (Consultant, USA)

For a quarter century of strategic and forward-looking leadership of the CPMT Society and key CPMT conferences.

The **Outstanding Sustained Technical Contribution Award** is given to recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society. The 2012 recipient:



Tseung-Yuen Tseng (National Chiao-Tung University, Taiwan)

For outstanding sustained contributions in passive component, electronic ceramic and nanoceramic technologies.

The **Exceptional Technical Achievement Award** is given to recognize an individual, or group of individuals for exceptional technical achievement in the fields encompassed by the CPMT Society. The 2012 recipient:



Andrew A. O. Tay (National University of Singapore, Singapore)

For exceptional contributions to reliability modeling and the understanding of delamination and popcorn failure of IC packages.

The **Electronics Manufacturing Technology Award** is given to recognize major contributions to Electronics Manufacturing Technology in fields encompassed by the CPMT Society. The 2012 recipient:



Chin C Lee (University of California, USA)

For significant enhancements to interconnect manufacturing through research, invention and education.

The **Outstanding Young Engineer Award** is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation. The 2012 recipient:



Mudasir Ahmad (Cisco Systems, Inc., USA)

For exceptional contributions to microelectronics packaging reliability design and assessment, and the CPMT Society.

The **Regional Contributions Awards** are given to recognize significant and outstanding leadership and contributions to the growth and impact of CPMT programs and activities at the Region level.

The **Regions 1-7 and 9 (US, Canada and Latin America) Award** 2012 recipient:



Vasudeva Prasad Atluri (Renavitas Technologies LLC, USA)

For over 20 years of outstanding and dedicated service to, support of and leadership in the CPMT Phoenix Chapter; with an emphasis on workshop and technical program leadership and fund-raising for the IEEE Phoenix Section Student Scholarship Endowment – all contributing to a strong, successful Chapter.

The **Region 8 (Europe, Africa, Middle East) Award** 2012 recipient:



Nihal Sinnadurai (ATTAC, United Kingdom)

For key contributions to establishing a collaboration between the CPMT Society and IMAPS-Europe, leading to the successful establishment of the Electronic System-Integration Technology Conference (ESTC) – the CPMT Society's Flagship Conference in Region 8, of which he was Executive Chair in 2008, as well as for sustained contributions as co-founder and Chair of the CPMT UK&RI Chapter.

The **Region 10 (Asia, Pacific) Award** 2012 recipient:

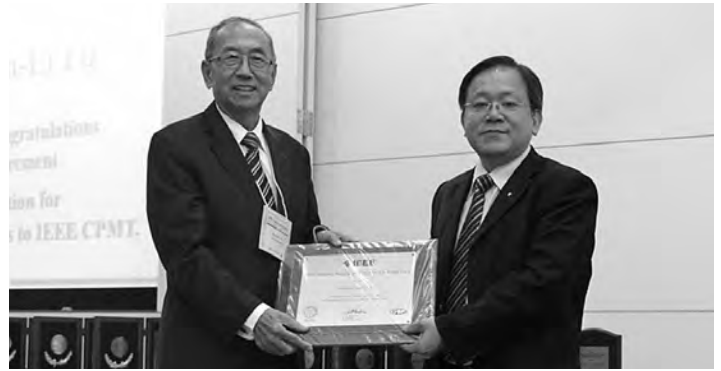


Andrew A. O. Tay (National University of Singapore, Singapore)

For establishing the Electronics Packaging Technology Conference (EPTC) – the CPMT Society's Flagship conference in Region 10, now in its 14th year; as well as for sustained significant contributions and outstanding leadership in the Joint Reliability/CPMT/ED Singapore Chapter and in the EPTC Board.

CPMT Society Honors Shen-Li Fu

In recognition of his recent retirement, as well as his contributions to the CPMT Society, CPMT President Ricky Lee presents Professor Shen-Li Fu (on left in photo) with a plaque, at the International Conference on Electronics Packaging and IMAPS All Asia Conference, 17-20 April 2012, Tokyo, Japan



CPMT TC-12 Electrical Design, Modeling and Simulation Cosponsors Tutorial at 2012 IEEE EMC Symposium

The CPMT Society Technical Committee on Electrical Design, Modeling and Simulation and the EMC Society TC-10 Signal Integrity will cosponsor a half-day tutorial on Advanced Topics in Signal and Power Integrity at the 2012 IEEE International Symposium on Electromagnetic Compatibility, 5 – 10 August 2012, Pittsburgh, Pennsylvania, USA.

The Tutorial, scheduled for Monday, 6 August, 1:30 pm–5:30 pm.

Scope:

The challenges of high-speed channel system design require the electrical engineer to understand signal integrity, power integrity and EMC and make the appropriate decisions so that all electrical constraints are met. This workshop is sponsored by the CPMT TC-12, which sponsors EPEPS Conference, and IEEE EMCS TC-10 to present advanced topics of signal integrity and bridge these topics

with EMC. The requested focus of the presentations will be bridging SI/PI/EMC when developing new technologies such as 3D or Optics, analysis and modeling techniques such as macromodeling, or designing channels to minimize common mode and EMI issues.

Chairs: Dale Becker, IBM Corporation, New York and Giulio Antonini, Università degli Studi dell'Aquila, Italy

Planned Speakers and Topics:

- 1) Fundamentals mechanisms for planar EBG for Power and Signal integrity – F. De Paulis, A. Orlandi
- 2) Parameterized Models for Efficient Design in EMC and SI Applications – F. Ferranti, G. Antonini, A. Ciccomancini Scogna
- 3) Statistical Uncertainty Analysis for High-Speed Designs – F. Canavero
- 4) High-Density Silicon Carrier Transmission Line Design for Chip-to-Chip Interconnects – Kevin Gu
- 5) Signal Integrity and Power Integrity Co-Design – Madhavan Swaminathan

CPMT Santa Clara Valley Chapter Planning Meeting

Following ECTC, the Santa Clara Valley Chapter sets off into the wild of microelectronics technology at their recent planning meeting. Standing, from left: Ed Aoki, chapter chair; Azmat Malik, chapter treasurer; Randall Brynsvold, presentations; Sandra Winkler, noon talks; Mudasir Ahmad, past chair (and CPMT Young Engineer awardee); and Tom Tarter, noon talks. Seated is Paul Wesling, chapter advisor, with the guiding documents for the expedition. He holds ITherm and ECTC programs, and past issues of the Transactions.



IEEE Women in Engineering in Action at 2012 ECTC

For the third consecutive year, the CPMT Society set-up a luncheon table for IEEE Women in Engineering at the ECTC Conference. This year the WIE table was set-up during the ECTC CPMT Luncheon on May 31st. We were fortunate to have Patricia MacLeod, ASE, host the table. While those sitting at the table may not all be IEEE WIE members, all were able to meet other engineering women and learn about their careers.



Publication News....

2011 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among 240 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

The awards were presented at the 62nd Electronic Components and Technology Conference (ECTC), May 2012.

Subscribers to this publication can access the papers on-line in IEEE Xplore at: <http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870>

Members can add the subscriptions to their membership at: <https://www.ieee.org/membership-catalog/productdetail/showProductDetailPage.html?product=MEMCPMT021>

PACKAGING TECHNOLOGIES CATEGORY

In-Situ Sensor-Matrix to Determine Package-Induced Stresses

Christian Djelassi, Thomas Aichinger, Michael Glavanovics, and Manfred Kaltenbacher, *Member, IEEE*; Volume 1 Number 11, November 2011

Abstract—Nearly all microelectromechanical systems nowadays include bipolar or metal oxide semiconductor (MOS) transistors. Those micro-electro-mechanical systems experience many temperature cycles during their life-time and may fail when the damage accumulation due to mechanical stress becomes critical. In this paper, we present a recently developed method to analyze in-situ the mechanical stress for integrated devices. We use a test-chip equipped with stress sensitive on-chip complementary MOS (CMOS) transistors which are arranged in a matrix system without need for an analog multiplexer to improve accuracy. The stress sensitive MOS cells will be calibrated with a beam bending system to obtain the relation between electrical measurement signals and physical stress. A major benefit of our MOS transistor stress cells is that they can be produced in any standard CMOS process. Furthermore, these MOS transistors, in particular their charge carrier mobilities, are much more stress sensitive than resistors. The proposed theoretical explanation is verified by measurements and finite element simulations

ADVANCED PACKAGING CATEGORY

Wafer Scale Integration of CMOS Chips for Biomedical Applications via Self-Aligned Masking

Ashfaque Uddin, *Member, IEEE*, Kaveh Milaninia, Chin-Hsuan Chen, and Luke Theogarajan, *Member, IEEE*; Volume 1 Number 12, December 2011

Abstract—This paper presents a novel technique for the integration of small complementary metal-oxide semiconductor (CMOS) chips into a large area substrate. A key component of the technique is the CMOS chip-based self-aligned masking. This allows for the fabrication of sockets in wafers that are at most 5 μm larger than the

chip on each side. The chip and the large area substrate are bonded onto a carrier such that the top surfaces of the two components are flush. The unique features of this technique enable the integration of macroscale components, such as leads and microfluidics. Furthermore, the integration process allows for microelectromechanical systems micromachining after CMOS die-wafer integration. To demonstrate the capabilities of the proposed technology, a low-power integrated potentiostat chip for biosensing implemented in the AMI Semiconductor's 0.5 μm CMOS technology is integrated in a silicon substrate. The horizontal gap and the vertical displacement between the chip and the large area substrate measured after the integration were 4 and 0.5 μm , respectively. A number of 104 interconnects are patterned with high-precision alignment. Electrical measurements have shown that the functionality of the chip is not affected by the integration process. A CMOS/microfluidic hybrid system is also demonstrated based on the proposed integration technology.

COMPONENTS: CHARACTERIZATION AND MODELING CATEGORY

Phenomenological Study of the Effect of Microstructural Evolution on the Thermal Fatigue Resistance of Pb-Free Solder Joints

Richard Coyle, John Osenbach, Maurice N. Collins, Heather McCormick, Peter Read, Debra Fleming, Richard Popowich, Jeff Punch, Michael Reid, and Steven Kummerl; Volume 1 Number 10, October 2011

Abstract—Unlike SnPb solders, the thermal fatigue reliability of the Sn-Ag-Cu (SAC) solders is believed to be influenced significantly by both the initial and evolving microstructures. This paper presents a phenomenological study of the relationship between the initial SAC solder joint microstructure, the evolving microstructure, and the thermal fatigue performance measured by accelerated temperature cycling (ATC). To reflect the board assemblies that are in field use, commercial surface mount components with multiple geometries and materials and from different package assemblers were joined to the board with different lead free SAC alloys. The initial microstructures of the board level solder joints were altered in a variety of ways including: 1) varying the solder joint cooling rate; 2) varying the number of solder reflow exposures; and 3) exposure to different isothermal temperature exposures. In all cases the solder joint microstructure was exposed to one or more of these treatments prior to exposure to temperature cycling. In addition, some of the test boards were exposed to different cycling dwell times to determine if the microstructural evolution that occurred during ATC testing effected the respective characteristic lifetimes of the joints. The microstructural evolution was tracked and characterized with optical metallography and scanning electron microscopy. These results could have practical implications in terms of limiting the ability to develop acceleration factors and effective strain-based models for predicting Pb-free solder joint life.

ELECTRICAL PERFORMANCE OF INTEGRATED SYSTEMS CATEGORY

Efficient Implicit–Explicit Time Stepping Scheme With Domain Decomposition for Multiscale Modeling of Layered Structures

Jiefu Chen, *Member, IEEE*, Luis Eduardo Tobon, *Student Member, IEEE*, Mei Chai, *Member, IEEE*, Jason A. Mix, and Qing Huo Liu, *Fellow, IEEE*; Volume 1 Number 9, September 2011

Abstract—An efficient time-domain technique is proposed for multiscale electromagnetic simulations of layered structures. Each layer of a layered structure is independently discretized by finite elements, and the discontinuous Galerkin method is employed to stitch all discretized subdomains together. The hybrid implicit-explicit Runge-Kutta scheme combined with subdomain-based Gauss-Seidel iteration is employed for time stepping. The block Thomas algorithm is utilized to accelerate time stepping for block tri-diagonal systems, which are frequently encountered in discretized layered structures. Numerical examples demonstrate that the proposed method is efficient in simulating multiscale layered structures.

ELECTRONICS MANUFACTURING CATEGORY

Influence of Thermal-Cycling-Induced Failures on the RF Performance of Ceramic Antenna Assemblies

Jussi Putaala, Olli Nousiainen, Mikko Komulainen, Tero Kangasvieri, Heli Jantunen, Markku Moilanen; Volume 1 Number 9, September 2011

Abstract—In this paper, the high-frequency behavior of ball grid array solder interconnections during thermal cycling tests (TCTs) was investigated. This interconnection type was used in ceramic antenna modules that were attached to printed wiring boards thermo-mechanically equivalent to commonly used FR-4 material. The tests were carried out in a TCT chamber operating in the 0–100 °C range. To observe TCT-induced failures in the interconnections, scattering parameter measurements (return loss) were performed both during the TCT and at room temperature during cycling breaks. These measurement data were contrasted with imaging results obtained with scanning acoustic microscopy (SAM), and scanning electron microscopy (SEM) was used to verify the failure mechanisms in the interconnections. The results indicate that degradation of interconnection(s) can be seen both during cycling and in room-temperature measurements in a wide frequency band. The degradation was seen best in deteriorating out-of-band characteristics of the antennas. Measurements during cycling gave a more comprehensive picture of the assemblies' electrical response to fractures in interconnections than did off-cycle measurements. SAM imaging showed indications of cracking much earlier than they were observed in S-parameter measurements. SEM results suggested that the main failure mechanism was cracking in solder.

Have You Read Them? The Most Downloaded CPMT Transactions Papers

What might you be missing in the CPMT literature? Following is a list of most downloaded papers in May 2012. Subscribers can access these and other papers on IEEE Xplore.

From Transactions on Components, Packaging and Manufacturing Technology:

Compact High-Gain mmWave Antenna for TSV-Based System-in-Package Application

Sanming Hu; Yong-Zhong Xiong ; Lei Wang ; Rui Li ; Jinglin Shi; Teck-Guan Lim; Volume 2 Number 5

This paper presents a cavity-backed slot (CBS) antenna for millimeter-wave applications. The cavity of the antenna is fully filled by polymer material. This filling makes the fabrication of a silicon CBS antenna feasible, reduces the cavity size by 76.8%, and also maintains the inherent high-gain and wide bandwidth. In addition, a through-silicon via-based architecture is proposed to integrate the 135-GHz CBS antenna with active circuits for a complete system-in-package. Results show that the proposed structure not only reduces the footprint size but also suppresses the electromagnetic interference.

Hybrid Liquid Immersion and Synthetic Jet Heat Sink for Cooling 3-D Stacked Electronics

Kota, K.; Hidalgo, P.; Joshi, Y. ; Glezer, A; Volume 2 Number 5

This paper focuses on the design and parametric numerical study of a hybrid heat sink combining a liquid thermal interface

with an array of synthetic jet actuators for 3-D chip stack cooling. The air-side heat sink exploits enhanced localized heat transfer achieved via a central array of synthetic jet actuators. The key focus of this paper is the numerical simulation of the dielectric liquid interface used to efficiently transmit the heat from the high-power 3-D stacked electronics to the hybrid heat sink base. The coupled natural convection in the fluid and conduction in solid spreaders sandwiched between the tiers of the stack form a novel efficient, passive, and scalable thermal management solution for 3-D stacked die structures. It is shown that this heat sink with a footprint of 76-mm square × 51-mm height can dissipate a total of 41 W of heat/power from the stack for a 44°C average chip temperature rise above ambient (an R_{ja} of ~ 1.06 K/W obtained passively).

Design, Fabrication, and Characterization of Freestanding Mechanically Flexible Interconnects Using Curved Sacrificial Layer

Hyung Suk Yang; Bakir, M.S.; Volume 2 Number 4

Technologies that enable integration of microelectromechanical systems (MEMS) (and sensor) chip with a complementary metal-oxide semiconductor (CMOS) integrated circuit (IC) are becoming increasingly more important as the semiconductor industry explores and tries to encompass “More-than-Moore” solutions for future electronic systems. 3-D integration, stacking of dissimilar chips that have been independently fabricated and optimized, is a promising method to integrate MEMS and its signal processing electronics into a single miniaturized package. Unlike conventional methods of integration, 3-D integration can simultaneously provide high density and high performance

interconnections without the added process complexity resulting from the CMOS and MEMS process reconciliation. Vital to the success of such integration are many novel interconnect technologies such as through-silicon vias, mechanically flexible interconnect (MFI) technology is another vital interconnect technology providing low stress, area array interconnections between a MEMS chip and a CMOS IC. MFIs are batch fabricated freestanding interconnect structures fabricated using two photolithography steps. The stand-off height of MFIs are 20 μm and the dimension can be as small as 100 by 50 μm . In this paper, design, fabrication, and characterization of MFIs are presented, this paper also demonstrates SU-8 ring structures that allow fabrication and confinement of solder ball, so that MFIs can be assembled using a conventional flipchip bonder. Critical technology that enables fabrication of MFIs is the technology that uses reflowed photoresist as a sacrificial layer, development of such process is also discussed.

Characterization of Encapsulants for High-Voltage High-Temperature Power Electronic Packaging

Yiying Yao; Zheng Chen; Guo-Quan Lu; Boroyevich, D.; Ngo, K.D.T.; Volume 2 Number 4

Seven encapsulants with operating temperature up to 250 °C are surveyed for possible use in high-temperature high-power planar packages. Processability is assessed by studying the flow fronts and the cured properties of the surveyed materials between parallel plates. Material B failed in the flow test because it dried out in seconds. Materials A, C, and D failed the curability test because A and C showed volume shrinkage during curing, while D cracked after curing owing to its brittle nature. It is found that elastic materials that usually correspond to low glass transition temperatures (T_g) tend to perform better with regard to large-area planar-structure packages. Materials E-G are confirmed to be comparatively stable with respect to temperature, and both dielectric strength and dielectric permittivity decrease by about 40 and 30%, respectively, as the temperature is increased from 25 to 250°C. The thermal aging test show that the materials harden during the aging process. Meanwhile, cracking starts in the material matrix. The dielectric strength of the sample drops by 60-70% to only around 10 kV/mm once cracking occurs.

Thermal Performance Assessment and Validation of High-Concentration Photovoltaic Solar Cell Module

Tsung-Lin Chou; Zun-Hao Shih; Hwen-Fen Hong; Cheng-Nan Han; Kou-Ning Chiang; Volume 2 Number 4

A high-concentration photovoltaic (HCPV) system with high optic-electric transition efficiency was developed in order to increase the electrical energy generated by a photovoltaic system. However, device temperature rises quickly because of the solar cell operating under concentrated-light operation conditions. Therefore, system output power or energy-conversion efficiency decreases as the temperature of the cell incorporated within the system increases. Consequently, thermal management has become an important issue for HCPV solar cell package. In this paper, the finite element (FE) analysis was used to initially establish a detailed FE model of the HCPV solar cell package as a baseline model. Moreover, the dissipation power of the solar cell obtained by employing a predicted function is

applied. Outdoor experiments were also performed to validate the baseline FE model with the estimated dissipation power. After validation of the simulation, an analysis of the thermal performance variations under different HCPV solar cell package design parameters was performed. Simulation results of different design parameters revealed that the geometry of the heat sink plate played an important role in the thermal management of the HCPV solar cell package.

From Transactions on Advanced Packaging:

High-Temperature Operation of SiC Power Devices by Low-Temperature Sintered Silver Die-Attachment

Guofeng Bai, J.; Jian Yin; Zhiye Zhang; Guo-Quan Lu; van Wyk, J.D.; Volume 30 Number 3

In this paper, we present the realization of high-temperature operation of SiC power semiconductor devices by low-temperature sintering of nanoscale silver paste as a novel die-attachment solution. The silver paste was prepared by mixing nanoscale silver particles with carefully selected organic components which can burn out within the low-temperature firing range. SiC Schottky diodes were placed onto stencil-printed layers of the nanoscale silver paste on Au or Ag metallized direct bonded copper (DBC) substrates for the die-attachment. After heating up to 300degC and dwell for 40 min in air to burn out the organic components in the paste and to sinter the nanoscale silver, the paste consolidated into a strong and uniform die-attach bonding layer with purity >99% and density >80%. Then the die-attached SiC devices were cooled down to room temperature and their top terminals were wire-bonded to achieve the high-temperature power packages. Then the power packages were heated up from room temperature to 300degC for high-temperature operation and characterization. Results of the measurement demonstrate the low-temperature silver sintering as an effective die-attach method for high-temperature electronic packaging. An advanced packaging structure for future SiC transistors with several potential advantages was also proposed based on the low-temperature sintering technology.

From Transactions on Components and Packaging Technologies:

Development of 3-D Silicon Module With TSV for System in Packaging

Khan, N.; Rao, V.S.; Lim, S.; Ho Soon We; Lee, V.; Xiaowu Zhang; Liao, E.B.; Nagarajan, R.; Chai, T.C.; Kripesh, V.; Lau, J.H.; Volume 33 Number 1

Portable electronic products demand multifunctional module comprising of digital, radio frequency and memory functions. Through silicon via (TSV) technology provides a means of implementing complex, multifunctional integration with a higher packing density for a system in package. A 3-D silicon module with TSV has been developed in this paper. Thermo-mechanical analysis has been performed and TSV interconnect design is optimized. Multiple chips representing different functional circuits are assembled using wirebond and flip chip interconnection methods. Silicon carrier is fabricated using via-first approach, the barrier copper via is exposed by the backgrinding process. A two-stack silicon module is developed and module

fabrication details are given in this paper. The module reliability has been evaluated under temperature cycling ($-40/125^{\circ}\text{C}$) and drop test.

From *Transactions on Electronics Packaging Manufacturing*:

Effects of Defects on the Thermal and Optical Performance of High-Brightness Light-Emitting Diodes

Liuxi Tan; Jia Li; Kai Wang; Sheng Liu; Volume 32 Number 4

Defects in terms of voids, cracks, and delaminations are often generated in light-emitting diodes (LEDs) devices and modules. During various manufacturing processes, accelerated testing, inappropriate handling, and field applications,

defects are most frequently induced in the early stage of process development. One loading is due to the nonuniform loads caused by temperature, moisture, and their gradients. In this research, defects in various cases are modeled by a nonlinear finite-element method (FEM) to investigate the existence of interfaces, interfacial open and contacts in terms of thermal contact resistance, stress force nonlinearity, and optical discontinuity, in order to analyze their effects on the LED's thermal and optical performance. The simulation results show that voids and delaminations in the die attachment would enhance the thermal resistance greatly and decrease the LED's light extraction efficiency, depending on the defects' sizes and locations generated in packaging.

Conference News....

“On the Hunt for Novel and Emerging Technologies while on Safari at ECTC”

By Sandra Winkler, Senior Industry Analyst, New Venture Research (newventureresearch.com), and IEEE/CPMT Santa Clara Valley Chapter Luncheon Program Chair

San Diego, home to the world-famous San Diego Zoo and Wild Animal Park, also hosts the annual ECTC (Electronic Component Technology Conference) every three years. Attendance at this year's 62nd ECTC was 1,230 people, who attended 347 presentations, up from 1,002 attendees the year prior. This was the second highest level of attendance since the inception of the ECTC 62 years ago. A total of 359 people attended the 16 professional courses on Tuesday, May 29th, and the conference boasted 81 exhibitors in the technology corner. The program sessions ran from May 30 through June 1, 2012. With so many people in attendance, there was a high level of energy in the air, with attendees on the hunt for new information. There was plenty of that to be found.

Additional sessions at various times provided even more information beyond that of the main conference sessions.

A special session was held on Tuesday morning, titled **“Next-Generation Packaging and Integration: The Transformed Role of the Packaging Foundry.”** Chaired by Raj Pendse of STATS ChipPAC, speakers included Robert Lanzone of Amkor Technology, Bill Chen of Advanced Semiconductor Engineering (ASE), Mike Ma of Siliconware Precision Industries (SPIL), Steve Anderson of STATS ChipPAC, and Dan Tracy of SEMI. Capital expenditures are going up by an order of a magnitude with TSVs in the equation, making it difficult for OSATs to fund their own growth. The need for collaboration was brought up not only here, but in many other conference sessions as well. About 3 percent of the top OSATs' revenue is designated for R&D, which is feeding

new technologies and helping these companies find new ways to reduce costs.

2.5-D is a hot topic, and is already in production in small quantities; bringing costs down will fuel the growth. TOs cost \$35 in 1963 if the purchase price had not been artificially lowered (selling below cost), the industry would not have flourished as it did, when it did. The same will be true of other upcoming technologies—a lower cost will fuel purchasing power. The FOWLP, or fan-out wafer-level package, is opening up new possibilities of new markets. This technology can also enable a TSV stack; a dense interconnect silicon interposer will be needed for this.

In an effort to lower cost, many OSATs are moving to copper wire bonding, as the price of gold has become prohibitive. Because cost is such a strong underlying factor, the “high-end mentality” has to give way to trying the cheapest way first and building performance up from there. Producing something using the highest priced manufacturing technology makes it more difficult to reduce cost later.

The Tuesday night panel session, titled **“Power Electronics—A Booming Market,”** was chaired by Rolf Ashenbrenner of Fraunhofer IZM and Ricky Lee of Hong Kong University of Science and Technology. Speakers included Dan Kinzer of Fairchild Semiconductor, Klaus-Dieter Lang of Fraunhofer IZM, Lionel Cadix of Yole Development, Ljubisa Stevanovic of GE Global Research, and Bernd Roemer of Infineon Technologies AG. This technology is hot primarily in Europe, for renewable energies, power supplies, e-mobility, LED systems, smart power electronics, and network control. New materials and technologies will be needed in this market. Aluminum ribbon, copper aluminum ribbon, or copper wire bonding will replace aluminum wire bonding, and silver sintering or diffusion soldering for die attach will improve device life. The demand for power electronics is very regional.

The Wednesday luncheon keynote speaker was Gregg Bartlett of GLOBALFOUNDRIES. He mentioned the need for collaboration

during design, something that previously didn't occur. This will bring the best minds to the table at the outset. 2.5-D and 3-D really require collaboration to make the whole fit seamlessly together. These technologies offer improved system-level performance and bandwidth with reduced latency and power requirements compared with competing technologies. 2.5-D and 3-D accommodate a smaller bump pitch. 2.5-D enables a "fission" of the CPU, GPU, and memory for high-bandwidth applications, integrating each chip individually into the whole so that each chip can have its own "needs" met, given that each involves different back-end processes. Silicon partitioning will occur with interposers, and increase with complexity, from FPGAs in 2011, memory cubes in 2013, and logic plus memory in 2013–2014 to, ultimately, wide-I/O memory on an application processor for more sophisticated heterogeneous stacking.

The Wednesday evening plenary session on **"Photonics, Expanding Markets, and Emerging Technologies,"** was chaired by Christopher Bower of Semprius, Inc. Speakers included Ashok Krishnamoorthy of Oracle, Jeff Perkins of Yole Development, Shen Liu of Huazhong University of Science and Technology, Alexander Fang of Aurion, Timo Aalto of VTT Technical Research Centre of Finland, and Frank Libsch of IBM Corporation. LEDs, photonics integration on silicon, photonics packaging, and photonics to the processor chip were covered in this broad field.

Packaging is 40 percent of the cost of an LED, or light-emitting diode. The cell phone was the first killer application for LEDs; general lighting—otherwise known as HB (high brightness)—will be the next big thing for the LED market. Currently the cost of an LED light bulb is anywhere from \$15 to \$40 with rebates, compared with less than \$1 for an incandescent bulb, putting LEDs out of reach for most residential customers. There are no standards for HB LEDs, and thermal issues are huge. The cost of an HB LED needs to come down by a factor of 10, which will come about with a lower-cost packaging solution, such as wafer-level packaging.

The photonics industry in general does not have much in the way of standards. Photonics involve using light to carry the signal, rather than an electron. Photonics can be used in large-area data centers and on a single high-powered silicon chip. Uses abound in telecom, datacom, and computers. Because of the current high-cost manual processes to create photonic structures, efforts in recent years have focused on bringing costs down in a number of ways.

In fiber-optic telecom uses, getting the package standardized, as in the IC world, has been up in the air for some time. Connecting the delicate fiber structures to a standardized package such as a butterfly package is difficult. The trick is to accomplish this without breaking the fiber-optic structures. Bringing photonics down to the computer level, either inter-chip or intra-chip, involves lowering the costs significantly by incorporating waveguides on silicon, a low-cost material. This is years away from actual production, and will require a killer application to justify spending the R&D costs to make it a reality. Germanium or some other material would have to be added to the mix, as silicon absorbs light, rather than reflects it, and the light cannot be absorbed if it is to continue carrying the signal down the line.

The final evening session on Thursday night was titled **"Advanced Coreless Package Substrate and Material Technologies."** The co-chairs were Kishio Yokouchi of Fujitsu Interconnect Technologies and Venky Sundaram of Georgia Institute of Technology. Speakers included Yuji Nishitani of Sony Corporation, Tanaka Kuniyuki of Shinko Electric Industries Co., Takeshi Eriguchi of Asahi Glass Co., and Masateru Koide of Fujitsu Advanced Technologies.

Advantages of coreless substrates are several. Wiring capabilities allow direct signaling; all layers can be used as a signal layer. High performance comes from the lowest self-inductance and the highest mutual inductance. A coreless substrate is likely the widest bandwidth substrate structure.

Assembly problems include a higher warpage factor than with a cored substrate. Reflow is more difficult at higher temperatures. A number of options were presented to overcome warpage issues, including:

- Use of a clamp during chip attach
- Use of lower CTE insulator prepreg materials
- Use of a stiffener
- Lower temperature soldering

The program sessions ran for three full days, with six parallel sessions running at all times. Thus the topics to choose among were copious, and included advanced packaging methods such as 2.5-D/3-D, advanced interconnect, wafer-level packaging, LEDs, substrates, optoelectronics, modeling and simulation, materials and processing, RF, applied reliability, and emerging technologies. There was something for just about everyone connected to components, packaging, and manufacturing technologies (CPMT) in this jungle of options.

EPTC 2012

14th Electronics Packaging Technology Conference

5 - 7 December 2012, Resorts World Sentosa, Singapore

CALL FOR PAPERS

ABOUT EPTC

The 14th Electronics Packaging Technology Conference (EPTC 2012) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society.

EPTC 2012 will feature technical sessions, short courses/forums, an exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new development in the following categories:

- ❑ **Advanced Packaging:** Flip chip packaging, Wire-bond packaging, Embedded passives and actives on substrates, 3D System in Packaging
- ❑ **Wafer Level Packaging:** Wafer level packaging (Fan-in, Fan-out), 3D integration, Through Silicon Via, Silicon interposer
- ❑ **Interconnection Technologies:** Wire bonding technology, Solder bump technology, Solder alternatives (ICP, ACP, ACF, NCP), and TSV
- ❑ **Emerging Technologies:** Packaging technologies for MEMS, Biomedical, Optoelectronics, Photo voltaic, Printed electronics, Wearable electronics, etc.
- ❑ **Materials & Processes:** Materials and processes for traditional and advanced microelectronic systems, 3D packages, MEMS, Solar, Green and Biomedical packaging
- ❑ **Electrical Modeling & Simulations:** Power plane modeling, Signal integrity analysis of substrate/package
- ❑ **Mechanical Modeling & Simulations:** Thermo-mechanical / Structural / Moisture modeling, Solder/metal fatigue, Vibration, Drop impact, etc.
- ❑ **Thermal Characterization & Cooling Solutions:** Thermal modeling and simulation, Component and system level thermal management and characterization
- ❑ **Quality & Reliability:** Component, board and system level reliability assessment, Interfacial adhesion, Accelerated testing, Failure characterization, etc.
- ❑ **Wafer/Package Testing & Characterization:** High-speed test architectures and systems, Test methodologies, Probe card design

IMPORTANT DATES

Submission of abstract - Extended	15 th July 2012
Notification of acceptance	1 st August 2012
Submission of manuscript	1 st October 2012

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well. Authors can choose between oral or poster presentation.

Authors must designate two appropriate categories (found under CONFERENCE TOPICS) for abstract review. All submissions must be in English and should be made via the online submission system found at <http://www.eptc-ieee.net>. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by 15th June, 2012. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Authors will be notified of paper acceptance and publication instruction by 1st August 2012. The final manuscript for publication in the conference proceedings is due by 1st October 2012. Selected papers will be published in IEEE/CPMT journals.

OUTSTANDING TECHNICAL PAPERS

The conference proceeding is an official IEEE publication. Author(s) of Best Technical Paper (ORAL/POSTER), Outstanding Technical Paper (ORAL) and Best Student Paper will receive an award at the next conference.

CALL FOR SHORT COURSES

The conference program includes short courses which will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings. Proposals for short courses can be submitted to techchair@eptc-ieee.net

CALL FOR EXHIBITION/SPONSORSHIP PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference. Potential exhibitors and sponsors may email eptc2012.secretariat@atenga.sg for details.

Organized by



General Chair:

Mr. Navas Khan, Freescale

Technical Chair:

Mr. Ashok Anand, AMD

Program Chair:

Mr. Alfred Yeo, Infineon

Sponsored by



Conference information & contacts: Website: <http://www.eptc-ieee.net> Email: eptc2012.secretariat@atenga.sg

**IEEE Workshop on
Chip-Packaging Co-Design for
High Performance Electronic Systems**

September 24-25, 2012 – Techmart, Santa Clara, CA, USA

The purpose of the IEEE **Chip-Packaging Co-Design Workshop for High Performance Electronic Systems (CPCW)** is to provide a forum for technical education and research interchange on the topic of chip-packaging co-design, and co-design manufacturing and reliability impacts. The workshop will be organized around tutorials, invited papers, contributed papers and posters.

The workshop is aimed at systems, signal integrity, power integrity, circuit design, and reliability engineers/managers wishing to better understand challenges and solutions in system design, manufacturing, and qualification.

**Abstracts and papers may now be submitted --
300-word abstracts by July 20th, 2012.**

Sponsored by: IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society

Workshop Committee

General Chair: Lei Shan, IBM Research

leis@us.ibm.com +1-914-945-2304

Advisory Chair: Paul Franzon, ECE, NCSU

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Technical Chair: Peng Su, Cisco Systems, Inc.

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Paper submission:

Email: pensu@cisco.com and leis@us.ibm.com

Topical areas include the following:

- Design practices and methods including chip-package interactions:
 - Holistic power integrity and signal integrity involving both chip and packaging
 - Thermal/mechanical design of chip and packaging
 - Design for 3D chip stacking and packaging
 - Modeling tools and elements that allows chip-package co-design
- Manufacturing limitations/errors and their impacts on system specifications:
 - Chip-level manufacturability including:
 - 3D chip stacking and TSV
 - Flip Chip s and wire bonds
 - Packaging-level manufacturability including:
 - 3D packaging and assembly including interposers
 - Substrate, PCB, connector/socket, and assembly, etc.
- System reliability and qualification including chip-packaging interaction (CPI) for advanced Si nodes and impact of system application conditions.

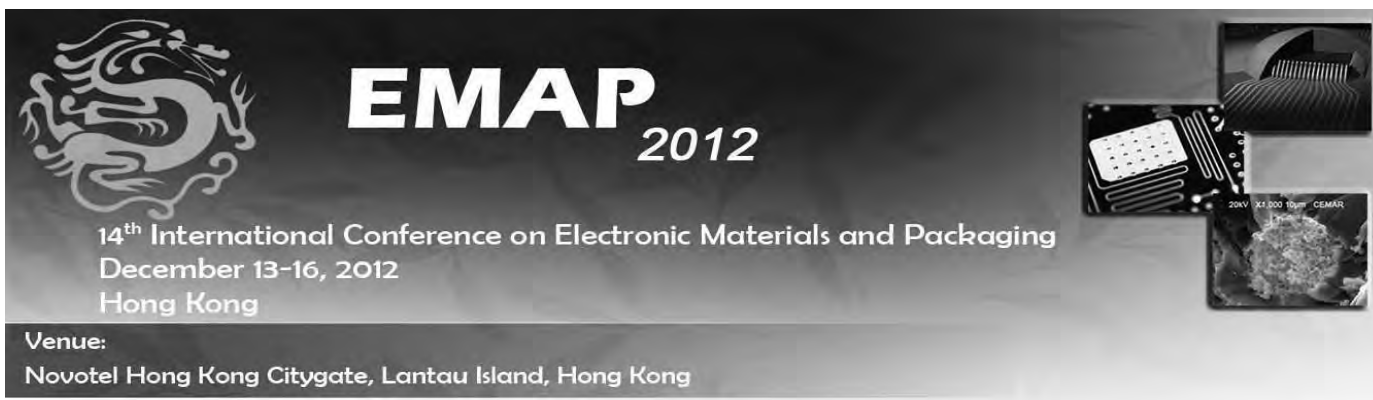
Only abstracts are required, for this Workshop.

- Technical talks: **30 minutes including Q&A**
- Keynote lectures and tutorials: 60 minutes including Q&A

Industrial sponsorship contact: Paul Wesling
p.wesling@ieee.org +1 408 331 0114

Full information:

www.ieee-cpcw.org



FIRST CALL FOR PAPERS

It is our pleasure to announce that the 14th International Conference on Electronic Materials And Packaging (EMAP2012) will be held at Novotel Hong Kong Citygate, Lantau Island, Hong Kong, on December 13–16, 2012. This international conference is co-organized by the Hong Kong University of Science and Technology (HKUST) and IEEE-CPMT Hong Kong Chapter. It is co-sponsored by the HKUST, IEEE-CPMT Hong Kong Chapter, and IEEE-CPMT Society.

EMAP2012 aims to provide a comprehensive coverage of recent advances in materials and packaging for different microsystems. This will also provide an excellent opportunity for researchers and engineers to identify and discuss recent advances and new promising research directions. We aim to strengthen R&D activities on electronic materials and packaging technologies in Asia and other regions in the world, to bridge academic scholars with industrial researchers, and to promote EMAP as a major international forum in this increasingly important area. Scientists, engineers, researchers, and students from universities, research institutes, and related industrial companies are cordially invited to submit abstracts and to participate in the conference.

CONFERENCE TOPICS

The conference will include all fundamental and applied sciences and technologies related to the fields of electronic materials, devices, and packaging. Topics may include from, but are not limited to, the following areas:

- ☐ Materials and Processing
- ☐ Passive and Active Components
- ☐ Optoelectronics / Photonics
- ☐ Sensor, Actuator, and Transducer Technologies
- ☐ Advanced Packaging
- ☐ Emerging Packaging Technologies
- ☐ Interconnection Technologies
- ☐ System-in-Package (SiP) and 3D Stacked Die Packaging
- ☐ Electrical Modeling, Characterization, and Signal Integrity
- ☐ Thermal-Mechanical Modeling and Characterization
- ☐ Packaging Technologies for High Brightness LEDs
- ☐ Quality and Reliability

IMPORTANT DATES

Submission of Abstract	August 10, 2012
Notification of Acceptance	September 15, 2012
Pre-registration	October 18 – November 30, 2012
Submission of Final Manuscript	November 20, 2012

CONFERENCE LANGUAGE

The official language of the conference is English.

ABSTRACT AND PUBLICATION

You are invited to submit a 300-word abstract that include title of the paper, authors, affiliations, abstract body, and area of interest by e-mail to emap2012s@ust.hk by August 10, 2012. The presenter must be one of the authors and a registered Conference participant. The name of the person who is to present the paper should be underlined and the full contact information should be included. The one-page abstract should be submitted in MS Word format. After a peer review, the accepted papers will appear in the Conference Proceedings published by the IEEE provided that the submitted papers are original.

Please visit the <http://www.ust.hk/emap2012/> for full abstract format instructions.

2012 IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS)

Call for Papers

December 9-11, 2012, Taipei, Taiwan

<http://edaps2012.ntu.edu.tw>

The IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium has been one of main events in Asia Pacific region that attract world class designers and researchers to share their state-of-the-art results related to modeling, simulation, and measurement for the electrical design issues on chip, package and system levels. The symposium consists of paper presentations, industry exhibitions, workshops, and tutorials. The technical program of the symposium not only addresses the current technical issues but also brings out the challenges facing IC design, SiP/SoP packaging, EMI/EMC, EDA tools, and most importantly the challenges in next generation 3DIC and packaging design.

Taiwan is famous as a Silicon Island, which has been playing a leading role in the design and fabrication service in chips, packages, and boards. A knowledge sharing platform with strong interaction between academia and industry will be highly expected in EDAPS 2012.

Dr. Shang-yi Chiang

Executive Vice President and Co-Chief
Operating Officer, TSMC
Taiwan

Dr. Mitsumasa Koyanagi

Professor, New Industry Creation
Hatchery Center (NICHe)
Tohoku University
Japan

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Topics

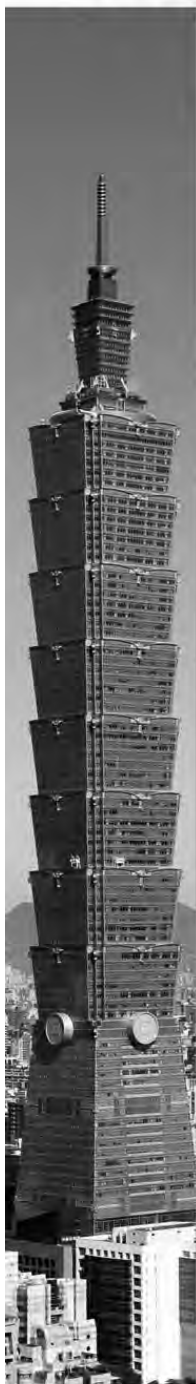
- 3DIC / 3D-Stacked IC
- Testing on 3DIC and SiP
- Signal Integrity
- Power Integrity / Ground Noise
- Time/Frequency Domain Measurement Techniques
- SiP/SoP
- Embedded Passives
- Electromagnetic Compatibility (EMC)
- Design and Modeling for High-speed Channels and Interconnects
- Package Reliability
- RF/mmW Circuit Package
- Advanced Simulation Tools and CAD
- Substrate Technology
- Others

Important Dates

Deadline for Regular Paper Submission:
Sept. 1, 2012

Tutorial/Workshop Proposal Submission:
Sept. 1, 2012

Acceptance Notice:
Oct. 5, 2012



63rd ECTC Call for Papers

First Call For Papers 63rd Electronic Components and Technology Conference

www.ectc.net

To be held May 28 - May 31, 2013

Cosmopolitan of Las Vegas, Las Vegas, Nevada, USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:

3D integration, embedded, and wafer level packaging, flip chip, advanced substrates, novel assembly technologies, interposers, TSVs, MEMS & sensors, optoelectronic & photovoltaic device packaging.

Applied Reliability:

3D package reliability, characterization and test methods, interconnection reliability; solder and material characterization, and next generation/novel packaging reliability.

Assembly and Manufacturing Technology:

Assembly challenges and solutions, manufacturing aspects of 3D/TSV, manufacturing challenges of wafer thinning and flip chip processing.

Electronic Components & RF:

Components (including embedded components) and modules for RF/THz systems and bio applications, metamaterials, wireless sensors, RFID, RF MEMS, flexible & printed electronics, "green" RF electronics, wireless power transmission, power scavenging components, nano-based RF structures, and low-power RF designs.

Emerging Technologies:

Emerging packaging concepts and technologies, emerging 3D packaging concepts, novel approaches to packaging, organic IC & TFT, microfluidics and MEMs, anti-counterfeiting packaging, and packaging for biosensing.

Interconnections:

Design, structure, processes, performance, reliability (including electromigration), and test of first- and second-level interconnections. Interconnections for 3D integration including TSV and silicon interposers; interconnections in substrates, PCBs and systems. Solder bumping and Cu-pillar for flip chip packaging.

ing, wafer-level packaging, advanced wirebond interconnections, non-solder interconnections and connectors.

Materials & Processing:

Adhesives and adhesion, lead free solder, novel materials and processing; underfills, mold compounds, and dielectrics, emerging materials and processing for 3D.

Modeling & Simulation:

Thermal, mechanical, electrical modeling and related measurements, 3D/TSV design and modeling, fracture and warpage in packages, and high-speed interconnects.

Optoelectronics:

Optical system integration and photonic system-in-package, power efficient optical subsystems, fiber optical interconnects, optical-PCB, active optical cables, optical transceivers, optoelectronic assembly and reliability, high-efficiency LEDs and high power lasers, integrated optical sensors, silicon photonics, polymer and thin glass based waveguide technology.

Interactive Presentations (formerly Posters):

Papers may be submitted on any of the listed major topics and presentation of papers in an interactive format is highly encouraged at ECTC. Interactive presentation papers allow significant interaction between the presenter and attendees, and are especially suited for material that benefits from more explanation than is practical for oral presentations. Highly rated abstracts not fitting into topic of an oral session, highly rated abstracts that are submitted specifically for interactive presentation, or abstracts that are selected at the discretion of the program chair are included in the Interactive Presentation sessions.

You are invited to submit a <750-word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have any questions, contact:

Beth Kesar, 63rd ECTC Program Chair
Qualcomm, Inc.
5775 Morehouse Road
San Diego, CA, USA
Phone: +1-858-658-3332
Email: beth@qualcomm.com

Abstracts must be received by October 8, 2012. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 8, 2012. If you have any questions, contact

Kitty Pearsall, 63rd ECTC Professional Development Courses Chair
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The 2012 IEEE-CPMT / IMAPS Advanced Technology Workshop on Optoelectronic Packaging and Assembly



Advance Announcement

The Institute of Electrical and Electronics Engineers - Components, Packaging and Manufacturing Technology Society (IEEE-CPMT) and the International Microelectronics and Packaging Society (IMAPS) jointly announce the 2012 Advanced Technology Workshop on Opto-electronic Packaging and Assembly. This workshop will feature an ITRS Assembly and Packaging Roadmap working session as well.

Dates: **September 6 & 7, 2012**

Location: **Embassy Suites, 3100 East Frontera Street, Anaheim, CA 92806**

Thursday, September 6, 2012

8:00 am – 5:00 pm

Optoelectronic Packaging & Assembly

Invited technical experts will be presenting on the advances and trends in Optoelectronic Packaging and Assembly Technology areas for applications such as **Optical Interconnects & Semiconductor Photonics, Optical Transceivers & Networks, High Brightness LED and CMOS Image Sensors.**

Featured Speakers:

Keynote Address: **Prof. Ricky Lee, President, IEEE CPMT Society**

Dr. Mehdi Asghari, Kotura

Dr. Daniel Van Blerkom, Forza Silicon

Ron Bonne, Philips Lumileds

Dr. Jack Cunningham, Oracle Labs

Dr. Peter De Dobbelaere, Luxtera

Dr. Ali Ghiasi, Broadcom

Dr. Radha Nagarajan, Infinera

Dr. Adit Narasimha, Molex

Prof. George Papen, UCSD

Jeff Perkins, Yole Developpment

Dr. Mark Verdiell, Samtec

Friday, September 7, 2012

8:00 am – 12:00 pm



ITRS Assembly & Packaging Roadmap Working Session

The International Technology Roadmap for Semiconductors (ITRS) Organization will hold an assembly and packaging roadmap working session for the workshop participants, with a presentation on the ITRS working process and an interactive discussion about their optoelectronic packaging activities.

Platinum Sponsor



Silver Sponsor



For Sponsorship & Vendor Exhibition inquiries, please contact:

Lawrence Williams – larry.williams@ansys.com, 714-417-9311 x449

Jaydutt Joshi – jaydutt@gmail.com, 949-697-9814

Registrations:

Early-Bird Registration Fees: IEEE / IMAPS Members - \$200; Non-Members - \$250; Students - \$75
Registration options are available for attending only one of the days as well. Prices will increase for each category, after July 31, 2012.

Registration Instructions at https://meetings.vtools.ieee.org/meeting_view/list_meeting/12685

Workshop Organizing Committee

General Chairs

Robert Warren, Conexant Systems, Inc. robert.warren@conexant.com

John Mazurowski, Penn State Electro-Optics Center, jmazurowski@eoc.psu.edu

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Paul Wesling, Communications Director - IEEE, p.wesling@ieee.org

Vendor Exhibits & Sponsorships:

Lawrence Williams, Ansys Corporation, larry.williams@ansys.com

Jaydutt Joshi, Skyworks Solutions, Inc., jaydutt@gmail.com

Local Arrangements:

Hossein Ahmad, Boeing, hossein.ahmad@boeing.com

University Relations:

Mark Bachman, Univ. of California – Irvine, mbachman@uci.edu

Workshop Website: <http://www.cpmt.org/opto2012>



The International Electronics Manufacturing Technology (IEMT) Conference is the premier IEEE event devoted to the manufacture of electronic, opto-electronic and MEMS/sensors devices and systems. IEMT is an established International conference of long standing organized by the Components Packaging and Manufacturing Technology (CPMT) Society of IEEE. IEMT 2012 is organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from CPMT's Santa Clara Valley Chapter.

IEMT 2012 will feature short courses, technical sessions, and exhibitions. It aims to provide good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation. IEMT 2012 is an international forum, providing opportunities to network and meet leading experts. Since the 1980's and 1990's, IEMT has gained a reputation as a premier electronics materials and packaging conference and is well attended by experts in the field of electronic packaging from all over the world.

Date : 6th Nov (Tuesday) to 8th Nov (Thursday), 2012

Venue : Kinta River Front Hotel, Ipoh, Perak, Malaysia.

Conference web-site : <http://ewh.ieee.org/r10/malaysia/cpmt/>

ORGANISER: IEEE COMPONENTS, PACKAGING & MANUFACTURING TECHNOLOGY SOCIETY (CPMT – Malaysia/Santa Clara)

MAIN HOST: Carsem (M) Sdn. Bhd.

CO-ORGANISERS: FairChild Semiconductor
FreeScale Semiconductor
Infineon Technologies (M) Sdn. Bhd.
Intel Technology (M) Sdn. Bhd.
ON Semiconductor (M) Sdn. Bhd.

StatsChippac (M) Sdn. Bhd.
Texas Instruments (M) Sdn. Bhd.
UniSem (M) Bhd.
Universiti Malaya
Universiti Sains Malaysia

Universiti Teknologi Malaysia



Conference Website: <http://www.icept.org> **Conference Email:** icept2012@vip.163.com

The 13th International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2012) will be held in Guilin, China, from August 13 to 16, 2012. The ICEPT-HDP 2012 is organized by Electronic Manufacturing and Packaging Technology Society (EMPT) of Chinese Institute of Electronics (CIE) and co-organized by Guilin University of Electronic Technology. As one of the most famous international conferences on electronic packaging technology, the conference has received strong support from IEEE CPMT and active involvement from IMAPS, ASME and iNEMI, and was highly appreciated by China Institute of Electronics and China Association for Science and Technology (CAST).

ICEPT-HDP 2012 is a four-day event, featuring technical sessions, invited talks, professional development courses/forums, exhibition, and social networking activities. It aims to cover the latest technological developments in electronic packaging, manufacturing and packaging equipment, and provide opportunities to explore the trends of research and development, as well as business in China



IEEE CPMT Society Sponsored and Cosponsored Conferences 2012

- Name: 2012 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2012)
Dates: August 13–16, 2012,
Location: Guilin, China
URL: <http://www.icept.org>
Contact: empt-cie@sohu.com
- Name: 2012 IEEE/IMAPS Workshop on Optoelectronic Packaging
Dates: September 6–7, 2012
Location: Orange County, CA, USA
URL: <http://www.cpmc.org/opto2012/>
Contact: Sam Karikalan
- Name: 2012 34th Annual Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD 2012)
Dates: September 9–14, 2012,
Location: Tucson, AZ USA
URL: <http://www.esda.org/symposia.html>
Contact: [Lisa Pimpinella lpimpinella@esda.org](mailto:Lisa.Pimpinella@esda.org)
- Name: 2012 57th IEEE Holm Conference on Electrical Contacts (HOLM 2012)
Dates: September 11–14, 2011,
Location: Minneapolis, MN USA
URL: <http://www.ewh.ieee.org/soc/cpmc/tc1>
Contact: [Deidre Zeigler, d.zeigler@ieee.org](mailto:Deidre.Zeigler@ieee.org)
- Name: 4th Electronics System Integration Technology Conferences (ESTC 2012)
Location: September 17–20, 2012
Location: Amsterdam, The Netherlands
Contact: estc@medicongress.com
- Name: 2012 IEEE Workshop on Chip-Packaging Co-Design for High Performance Electronic Systems
Dates: September 24–25, 2012
Location: Santa Clara, CA USA
URL: <http://ieee-cpcw.org/>
- Name: 2012 18th Int'l Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2012)
Name: September 25–27, 2012,
Location: Budapest, Hungary
URL: <http://therminic.eu/therminic2012>
Contact: [Marta Rencz, rencz@bme.eet.hu](mailto:Marta.Rencz@bme.eet.hu)
- Name: 2012 IEEE/CPMT Workshop on Accelerated Stress Testing & Reliability (ASTR 2012)
Dates: October 17–19, 2012
Location: Toronto, Canada
URL: <http://www.ieee-astr.org/default.htm>
Contact: [Kirk Gray kirk@acceleratedreliabilitysolutions.com](mailto:Kirk.Gray.kirk@acceleratedreliabilitysolutions.com)
- Name: 2012 7th Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2012)
Dates: October 24–26, 2012
Location: Taipei, Taiwan
URL: <http://www.impact.org.tw/2012/General/>
Contact: service@impact.org.tw
- Name: 2012 21st IEEE Electrical Performance of Electronic Packaging (EPEP 2012)
Dates: October 21–24, 2012
Location: Tempe, AZ USA
URL: <http://epeps.ece.illinois.edu/>
Contact: [Mandy Wisheart epeps-admin@illinois.edu](mailto:Mandy.Wisheart@illinois.edu)
- Name: 2012 14th Electronics Packaging Technology Conference (EPTC 2012)
Dates: December 5–7, 2012
Location: Singapore
URL: <http://www.eptc-ieee.net/>
Contact: [EPTC Secretariat eptc2011.secretariat@atenga.sg](mailto:EPTC.Secretariat@atenga.sg)
- Name: 2012 IEEE Electrical Design of Advanced Packaging & Systems Symposium (EDAPS 2012)
Dates: December 9–11, 2012
Location: Taipei, Taiwan
URL: <http://edaps2012.ntu.edu.tw/>
Contact: ctshih@tl.ntu.edu.tw
- Name: 2012 CPMT Symposium Japan 2012 (Formerly VLSI Packaging Workshop in Japan)
Dates: December 10–12, 2012
Location: Kyoto, JAPAN
URL: <http://www.vlsi-pkg-ws.org/committee.html>
- Name: 2012 4th International Conference on Electronics Materials and Packaging (EMAP2012)
Dates: December 13–16, 2012
Location: Lantau Island, Hong Kong
URL: <http://ihome.ust.hk/~emap2012//index.html>
Contact: [Dr. Zheming Zhang emap2012s@ust.hk](mailto:Dr.Zheming.Zhang@ust.hk)

**IEEE Components, Packaging and Manufacturing
Technology Society**

Marsha Tickman, Executive Director
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Piscataway, NJ 08854 USA



<http://www.estc2012.eu>

We are honored to announce the ESTC 2012 Conference which is to take place at the RAI Conference and Exhibition Centre of Amsterdam, The Netherlands, 17-20 September 2012.

Organized by IEEE-CPMT since 2006, in association with IMAPS-Europe, the Electronics System Integration Technology Conferences (ESTC) conference series is the premier global European event that brings together key researchers, innovators, decision-makers, technologists, businesses, and professional associations working in interconnect and packaging technologies for electronic system integration in order to present, demonstrate, and discuss the latest developments in assembly and interconnection technology and new innovative applications.

Just like its highly successful predecessor events in Dresden (2006), Greenwich (2008) and Berlin (2010), ESTC 2012 will again feature a powerful technical program, as well as professional short courses on various microelectronic packaging technologies. The concurrent exhibition will facilitate the presentation of state-of-the-art technological services and equipment to an interested audience of international decision-makers from science and industry.

