Components, Packaging, and Manufacturing Technology Society Newsletter

THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

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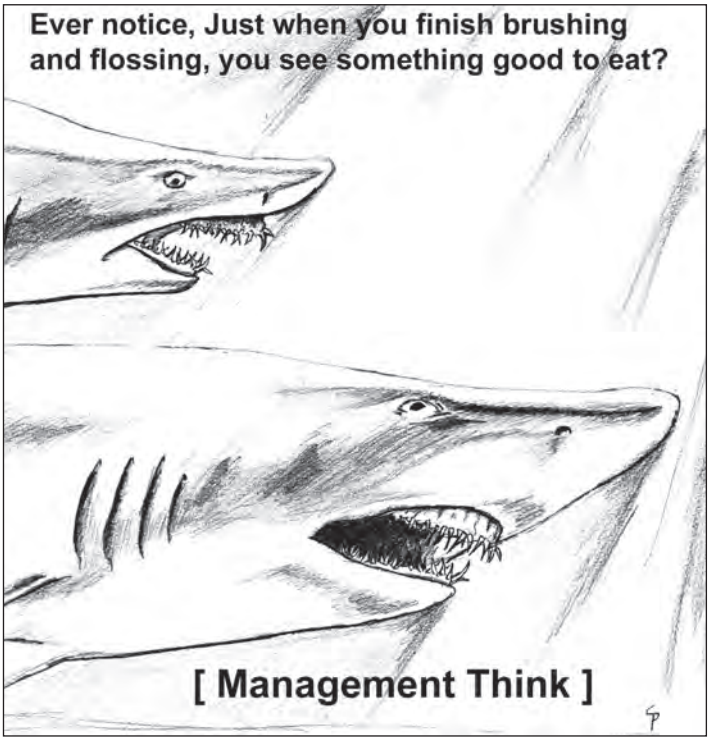
President's Column....

In the last Newsletter, I fabricated a scenario of "*Cracking the Da Vinci Code of 3D-IC*". The tune was based on Moore's Law and then extended to Miniaturization and Integration. In this column, I would like to go one step further to promote a new term "LEDification", which may be considered a variation from "MOOREfication".

Light-emitting diode (LED) is a semiconductor device with a p-n junction which can emit photons under forward bias. That's why LED is called a solid-state lighting (SSL) source. Although the electroluminescence effect was discovered in early 20th century, LED did not become industrialized until 1960s. Before the turn of the millennium, LED was mainly used for signaling and display applications. That was because LED had not completed its full color spectrum and the luminous flux of LED was still low at that time. Similar to integrated circuits (IC), the evolution of LED in the past two decades is indeed more than impressive. With the substantial progress of blue LED, phosphor materials, and power wattage in 1990s, white light illumination by blue LED together with yellow phosphor for general lighting applications became possible at the dawn of the 21st century. In the *Strategies in Light* 2000 conference, Dr. Roland Haitz of Agilent Technologies presented his observation and prediction on LED: "for a given wavelength (color), the amount of light generated per LED package increases by a factor of 20 every decade and, at the same time, the cost per lumen (unit of useful light emitted) falls by a factor of 10." These two trends are typically plotted in the format as shown above. The previous statement has been known as Haitz's Law since then and is also considered the LED counterpart to Moore's Law for IC. In recent years, commercial SSL products started to appear in the consumer markets around the world. Nowadays, people can easily buy LED lamps at Office Depot in the US and even at 7–11 stores in Taiwan!

The famous rock band Red Hot Chili Peppers released an album and hit single entitled "Californication" in 1999. This is also the title of an American dramedy TV series that debuted

(continued on page 3)



NEWSLETTER SUBMISSION DEADLINES:

1 August 2013 for Fall issue 2013
1 November 2013 for Winter issue 2014
1 February 2014 for Spring issue 2014
1 May 2014 for Summer issue 2014

Submit all material to nsltr-input@cpmt.org

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2015 term-end: Regions 1–6,7,9—Steve Bezuk, Patrick Thompson, Region 8—Chris Bailey; Region 10—Kuo-Ning Chiang, Charles W. Lee, Daniel Lu

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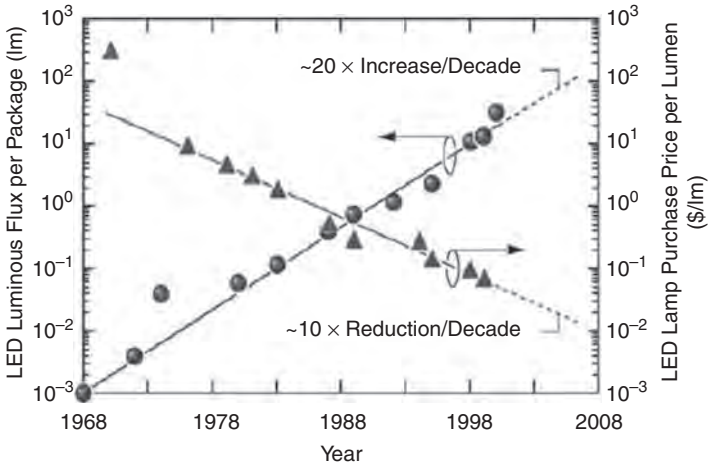

(based on Roland Haitz)

(Example of LEDification: a hotel toilet seat with LED night light)

on Showtime in 2007. According to Urban Dictionary, "Californication" implies *the process whereby the subject or object is enveloped in a California-esqe hold*. In my opinion, while "MOOREfication" continues to search for its bottom line (22 nm and beyond), the phenomenon of "LEDification" has started to creep in. In addition to high profile mega-events/projects such as the Olympic Games and the World Expo in China, people can see more and more applications of LED in our daily life. Typical examples include LED-backlit TVs/monitors, LED street lamps, LED car headlights and so on and so forth. Believe it or not, a hotel that I once stayed at had a toilet seat equipped with LED for night lighting! (see pictures above) Next time when you take an airplane, you may want to check to see if the cabin lighting and the toilet lighting are by LED.

Despite the increasingly innovative applications of LED, the propagation of SSL is not always that smooth. Many LED companies have been facing very severe financial challenges in the past eighteen months. This is not only due to the economic downturn, but also because of the imbalance between supply and demand. You may notice that most aforementioned examples are not in the average household. The main difficulty in bringing LED lighting into households is the rather high start-up cost. With the current average selling price at more than fifteen US dollars per LED lamp (for 60 W incandescent light bulb retrofitting), it is indeed extremely difficult to convince the general public to go for SSL in their homes for the moment. Nevertheless, most major countries in the world are developing and/or implementing policies to ban the production and installation of incandescent light bulbs due to their poor efficiency. By the year 2018, it is expected that most conventional light bulbs will have to be replaced. With the impetus from government policies for energy saving and proper promotion of the concept of "cost of ownership", people should be more willing to embrace SSL starting from 2015. Some industrial reports have predicted that the overall market penetration of LED in general lighting may reach 80% by 2020. It is my true belief that there exists a huge SSL market potential ahead of us.

With all above rationale, I proposed to organize a panel session in ECTC 2013 on "*LED for Solid-State Lighting—For a Brighter Future*". A panel of distinguished experts in relevant industries covered a wide range of issues with LED for SSL. In particular, an overview on the SSL industrial trends and market development in China was presented. This panel was well received and triggered many post-event inquiries. I consulted with the panelists and got their consent to post their presentation files at the ECTC website. As I highlighted in my previous column: "Knowledge grows only by being shared"! Please come join us in pushing "LEDification"!

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CPMT Society News....

E-Mail Alias and IEEE Web Account Needed

2013 CPMT Society Board of Governors Election On-Line

In order to vote in this year's CPMT Board of Governors election, members will need to have a valid e-mail alias on record with IEEE and also have an IEEE Web Account.

Eligible voting members will receive notification by e-mail in the Fall of this year with instructions for voting on-line. You will need an IEEE Web Account to access the ballot and cast your vote. This Web Account is the same one you may use for IEEE services such as renewing membership and accessing IEEE Xplore.

If you do not recall your Web Account username and password, or aren't sure whether you have established an account, please go to http://www.ieee.org/web/accounts to recover your password or establish a new account.

Please be sure to update your IEEE membership record with your current e-mail alias. If you DO NOT HAVE AN E-MAIL address or would prefer to receive a paper ballot by mail, please send your name, mailing address and IEEE Member Number by 23 August to:

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Jie Xue, Cisco Systems, Inc. Elected 2014–2015 CPMT Society President

Every two years, the CPMT Society Board of Governors (BoG) elects a President and Vice Presidents to serve for a two-year term. The term for the current Officers ends on 31 December 2013.

This year's election will take place in two parts—with the President elected mid-year and the Vice Presidents elected in the Fall. The elected President and Officers will take office on 1 January 2014 for a two-year term that runs to 31 December 2015.

The BoG elected Jie Xue as 2014–2015 CPMT Society President.

Jie is currently the Sr. Director of Component Quality and Technology Group at Cisco Systems, Inc., San Jose, California. Her team is responsible for component technology development and qualification of ASIC, network processors and optical modules, as well as the development of advanced semiconductor and packaging technologies. Since joining Cisco in 2000, she has been working on developing high performance flip chip packaging, system-in-package, multi-chip modules, chip-scale-packaging for high reliability networking products. Prior to joining Cisco, Jie held several management and engineering positions in Motorola Inc., working on R&D and product development.

Jie received a BS degree from Tsinghua University, a MS and Ph.D. from Cornell University. Her research has resulted in over 80 technical publications and conference presentations and 8 patents. She is an IEEE Fellow as well as IMAPS Fellow. She was the VP of Conferences in IEEE CPMT (2010–2011) and is VP of Technology in IEEE CPMT since 2012.

John H. Lau Receives 2013 IEEE Components, Packaging and Manufacturing Technology Award

John H. Lau
ITRI Fellow, Industrial Technology Research Institute, Hsinchu, Taiwan

"For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging."

The IEEE Components, Packaging and Manufacturing Technology Award, sponsored by the IEEE Components, Packaging and Manufacturing Technology Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies.

The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

The 2013 Award was presented to John H. Lau at the 63rd Electronic Components and Technology Conference, May 2013.

One of the most well-known authors in electronics packaging, John H. Lau's leading-edge research has driven reliability improvements and advancements with his extensive research on solder-joint reliability, environmentally friendly solder alternatives, and advanced interconnect techniques. Dr. Lau led an international team to study solder-joint reliability issues and published the first book on the subject in 1991. He published additional influential research addressing reliability in lead-free solder processes and advanced interconnect methods such as flip-chip technology. Dr. Lau has influenced the adoption of lead-free solder processes as the industry shifts to more environmentally friendly interconnect methods, publishing a book providing manufacturing guidelines and parameters in 2003. He was also responsible for converting Agilent Technologies' entire

product line to lead-free. Dr. Lau's recent work has provided extensive publications on advanced interconnect methods that have helped shape the landscape of 3D integrated-circuit integration technologies.

An IEEE Fellow, Dr. Lau is an ITRI Fellow with the Industrial Technology Research Institute, Hsinchu, Taiwan.

John Lau joins the following past recipients of this Award.

2012 – Mauro J Walker

"For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations."

2011 – Rao R. Tummala

"For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging."

2010 – Herbert Reichl

"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

2009 – George G. Harman

"For achievements in wire bonding technologies."

2008 – Karl Puttlitz Sr. and Paul A. Totta

"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages"

2007 – Dimitry Grabbe

"For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

2006 – C. P. Wong

"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005 – Yutaka Tsukada

"For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004 – John W. Balde

"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www.ieee.org/awards

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Congratulations to 2013 CPMT Award Winners

The CPMT Society annually recognizes individuals for contributions to the profession through technical achievements, service to the industry and to the Society. The following individuals received their awards at the 63rd Electronic Components and Technology Conference (ECTC), May 2013.

The **David Feldman Outstanding Contribution Award** is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.

Rolf Aschenbrenner, Fraunhofer IZM, Germany

For over 13 years of leadership, including serving as the CPMT Society's first President from Europe, and extending CPMT's global technical reach through strategic collaborations and establishment of new conferences.

The **Outstanding Sustained Technical Contribution Award** is given to recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society. The 2013 recipient:

Dongkai Shangguan, National Center for Advanced Packaging, China

For 20 years of technical leadership, especially in the areas of of lead-free and environmentally conscious electronics and advanced microelectronics packaging and assembly technologies for product miniaturization and functional densification.

The **Exceptional Technical Achievement Award** is given to recognize an individual, or group of individuals for exceptional technical achievement in the fields encompassed by the CPMT Society. The 2013 recipient:

Yong Liu, Fairchild Semiconductor, USA

For extensive contributions to analog and power packaging, focusing primarily on manufacturing assembly process modeling, reliability prediction, and innovations in analog and power packaging.

The **Electronics Manufacturing Technology Award** is given to recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society. The 2013 recipient:

Wen-Pin (Louie) Huang, ASE Group, Taiwan, ROC

For contributions to the development and implementation of copper wire bond technology in high volume production.

The **Outstanding Young Engineer Award** is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation. The 2013 recipient:

Dong Gun Kam, Anjou University, Korea

For development of a low-cost 60-GHz antenna-in-package solution that uses standard organic printed circuit board processes, and contributions to system-level signal integrity analysis, high-speed package design and signal integrity and EMI/EMC research.

Congratulations to IEEE CPMT Fellows Class of 2013

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Ramachandra Achar (Canada)
For contributions to interconnect and signal integrity analysis in high-speed designs

Rolf Aschenbrenner (Germany)
For contributions to microelectronic packaging

Kuo-Ning Chiang (Taiwan)
For contributions to design and reliability of electronic packaging

Paul Coteus (USA)
For contributions to packaging for high performance computing systems

Kenneth Goodson (USA)
For contributions to thermal management of electronic packaging

Wei Koh (USA)
For development of three-dimensional multichip modules and flip chip interconnects

James Libous (USA)
For contributions to switching noise minimization in CMOS technology

Ravi Mahajan (USA)
For contributions to electronic packaging technology and thermal management of microprocessors

Cian Ó Mathúna (Ireland)
For leadership in the development of power supply using micromagnetics on silicon

Arthur Morris (USA)
For development and commercialization of CMOS radio frequency micro electro-mechanical systems

Alton Romig (USA)
For leadership in management of research and development for defense systems

Subhash Shinde (USA)
For contributions to thermal management and 3D electronics packaging technologies

Tzong-Lin Wu (Taiwan)
For contributions to noise mitigation technologies and electromagnetic compatibility design on printed circuit boards

Wen-Yan Yin (PR China)
For contributions to multi-physics solutions for intentional electromagnetic interference and nanostructure electromagnetic compatibility

Chen-Hua Yu (Taiwan)
For leadership in development of interconnect technology for integrated circuits

New IEEE CPMT Senior Members

The members listed below were recently elevated to the grade of Senior Member.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

Devarajan Balaraman	Deepak Chodankar	Lang Klaus	Steve Lytle	Peter Silbermann
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Kalyan Biswas	Laurent Dellmann	Chethan Kumar Y B	Garrett Mccormick	Zheyao Wang
Thomas Brunschwiler	Shomir Dighe	Guo-Quan Lu	Narasim Murthy	Andres Wereszczak
Weng Yew, Richard Chang	Gruber Hermann	Xiaobing Luo	Bahgat Sammakia	Mei-Ling Wu

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The CPMT Society Welcomes New and Returning Members

The Members listed below either joined or rejoined the CPMT Society since 1 March 2013. Join us in welcoming them to the CPMT Community.

Seungho Ahn	Phoenix Section
Chris Alberg	Baltimore Section
Sergio Alcala Alcaraz	Mexico Section
Andrew Alduino	Santa Clara Valley Section
Douglas Alexander	Santa Clara Valley Section
Homoud Alsohaibi	Malaysia Section
Julio Ancalle De La Cruz	Peru Section
Chetan Angadi	Santa Clara Valley Section
Sudaporn Aramroon	Thailand Section
Marina Barroso	South Brazil Section
Sanjeewa Batawala Arachchige	Sri Lanka Section
Benarji Batsala	Hyderabad Section
Chris Baxter	San Diego Section
Reinhold Bayerer	Germany Section
Michael Belaousov	Israel Section
Dominik Boesl	Germany Section
Dan Boyne	Central Texas Section
Tung Bui	Tokyo Section
Andrew Cao	Santa Clara Valley Section
Fernando Carvalho	South Brazil Section
Jean-Pierre Cazenave	France Section
Saeed Chaleepa	North Jersey Section
Saravanan Chandrabalu	Bangalore Section
Nicolas Chantier	France Section
Sihai Chen	Mohawk Valley Section
Teng-Kai Chen	Santa Clara Valley Section
Hsien-Chie Cheng	Taipei Section
Deepak Chodankar	Bombay Section
Baratunde Cola	Atlanta Section
Carlos Cuellar	France Section

Flavio Dell'orto	Italy Section
Kiran Deshpande	Pune Section
Ognian Dimov	Providence Section
Xiaomin Duan	Germany Section
John Dunklee	Oregon Section
Francis Dupouy	Houston Section
Brian Durbin	Houston Section
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Wei Feng	Beijing Section
Jorge Filho	South Brazil Section
Benjamin Firestone	Pikes Peak Section
Ernest Fokoue	Rochester Section
Anthony Francis	Ozark Section
Ioannis Galanakis	Greece Section
Rodolfo Galutera	Coastal South Carolina Section
Mark Gerber	Dallas Section
Jennifer Giang	Orange County Section
Liang Gong	Beijing Section
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Mindaugas Greibus	Lithuanian Section
Qilin, Gu,	Oregon Section
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Tze Yang Hin	Malaysia Section
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Darren Ho	Orange County Section
Jeffrey Honeycutt	Boise Section
Uly Hong	Nanjing Section
Fazla Rabbi M Hossain	Phoenix Section

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Jun Inasaka	Tokyo Section
Shoya Iuchi	Kansai Section
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David Komma	Boise Section
Arpit Kothari	Santa Clara Valley Section
Abdul Koya	Charlotte Section
Ravin Krishnan	Malaysia Section
Michael Krueger	Germany Section
Huinan Kuah	Singapore Section
Takahiro Kurahashi	Tokyo Section
Tom Kwa	Santa Clara Valley Section
Bernardo Kyotoku	South Brazil Section
Damien Lambert	France Section
Stephen Lamotte	Milwaukee Section
John Leduc	Red River Valley Section
Jong Lee	Santa Clara Valley Section
Paul Lee	Tainan Section
Sylvie Lefloch Dubois	France Section
Marcial Leon	Costa Rica Section
Eng Hoo Leow	Malaysia Section
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Yifan Li	Santa Clara Valley Section
Kezhou Li	Shanghai Section
Weijia Li	Shanghai Section
Jiseok Liew	Houston Section
Jui Lim	Phoenix Section
Alexandre Lima	South Brazil Section
Tracy Lindsay	Boston Section
James Litton	San Fernando Valley Section
Christopher Lowe	Houston Section
Toru Maeda	Tokyo Section
Srinagesh Maganty	Hyderabad Section

Donaldi Mancelli	Greece Section
Dionysios Manessis	Germany Section
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Motonori Morizumi	Tokyo Section
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Nick Renaud-Bezot	Austria Section
Brian Reuter	Central Texas Section
Jean-Marc Rollin	Virginia Mountain Section
Sudipto Roy	Santa Clara Valley Section
Gerardo Ruiz	Monterrey Section
Yasser Sabry	Egypt Section

Assel Sakanova	Singapore Section
Hans Schiesser	Oakland-East Bay Section
Glen Schilling	Houston Section
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Akitsu Shigetou	Tokyo Section
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Sharleen Song	Shanghai Section
Ehsan Sooudi	U.K. & Rep of Ireland Section
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Raymond Spiewak	Worcester County Section
Edward Stoneham	Santa Clara Valley Section
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Stone Tang	Shanghai Section
James Taylor	Albuquerque Section
Hong The	Malaysia Section
Takeshi Terasaki	Tokyo Section
John Testtwo	Princeton/Central Jersey Section

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Daniel Tracy	Oakland-East Bay Section
Yu-Kai Tseng	Taipei Section
Steven Tu	Fort Worth Section
James Udo	Southern Minnesota Section
Kiran Vadlapati	Madras Section
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Ken Wang	Santa Clara Valley Section
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Laurens Weiss	Germany Section
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Tonglong Zhang	Nanjing Section
Zongmin Zhang	Shanghai Section
Xuemei Zheng	Washington Section
Jing Zou	Metropolitan Los Angeles Section

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Chapter News....

Students Form First CPMT Student Branch Chapter In Region 9 In Universidade Federal DO ABC

IEEE and CPMT Society Student Members at the UFABC (Federal University of ABC—São Paulo/Brazil) have worked together to form the first CPMT Student Branch Chapter in Region 9.

The members, mostly Materials Engineering students, are already at work on projects, including:

- Build a GemaSolar Thermosolar Plant using PCR aluminum as a low cost alternative source of energy.
- First UFABC Engineering Week
- Event called "UFABC para todos", when kids and teenagers from public schools are invited to know the UFABC courses and installations.
- Participating on a challenge from the Natura Company, in order to improve a stand-up pouch package.
- Integration week for Science & Technology Bachelor students
- Participating on 68th ABM International Congress (ABM – Metallurgy, Materials and Mining Brazilian Association).

Interim Student Branch Chapter Chair: Jorge Costa Silva Filho
Branch Chapter Advisor: Everaldo Carlos Venancio

Members:
Ana Clara Costa Chaves
Matheus Carmine Ferreira Fedele
Caio Costa Ramires
Fernando Luiz de Carvalho
Daniel Hideki Thoma
Raquel Domingues Paulucci
Barbara Souza de Paula
Tamara Santos F. Oliveira
Carlos Santos Batista
Carina Miyuki Nagai
Patricia Pereira Nogueira e Silva
Alexandre de Moura Lima
Isabela Cordeiro

18th IEEE International Symposium for Design and Technology of Electronics Packages – SIITME 2012

submitted by Cristina Marghescu, IEEE SBC of Politehnica University of Bucharest, Romania

The International Symposium for Design and Technology in Electronic Packaging (www.siitme.ro) is an annual Central European event in the field of electronics industry; SIITME event is technically sponsored and organized by IEEE CPMT Society Hu&Ro Joint Chapter.

The IEEE-CPMT Hu&Ro Joint Chapter is involved, through Prof. Pitică (Chair) and Prof. Illyefalvi-Vitez (Vice-Chair), in organizing the SIITME Conference. Since its first edition in 1995 it represented a scientific forum for exchanging information between academia and industry from Central and Eastern Europe on the topics related to their experimental and theoretical work in the field of electronics and micro-systems, manufacturing technologies and advanced packaging.

The beautiful town of Alba Iulia, situated in the heart of Transylvania, Romania hosted the 18th Edition. SIITME 2012 took place between the 25th–28th October 2012. The conference covered a variety of topics related to packaging, assembly and manufacturing technology, microsystems, advanced materials, communications, education and power electronics.

SIITME is a conference that gives the opportunity to young scientists to present their work. Many of the participants were Ph.D. students who took this opportunity to present and discuss results they obtained to other researchers. Research teams from all over Romania presented their results. Long-established universities such as Cluj, Iasi, Timisoara and Bucharest, as well as emerging young universities such as Alba Iulia, Baia Mare, Galati, Brasov, Pitesti, Suceava and Sibiu were present through the papers of nationally and internationally renowned professors and professionals. At the event also participated specialists from Czech Republic, France, Germany, Hungary, Serb Republic, Switzerland and Turkey.

The conference commenced with the presentations given by the keynote speakers in the opening plenary, who provided an "up to date" overview of three areas of actuality: manufacturing and characterization of transparent conductive layers for flexible optoelectronic devices presented by prof. dr. Klaus-Jürgen Wolter, simulation of electromagnetic fields, of high performance electronic applications presented by Alain Michel from ANSYS Inc., Europe and quality assurance—setup for optimum soldering

Animated discussions with researchers at evaluation during Poster Session

SIITME 2012 Participants

quality presented by Dr. Heinz Wohlrabe, Dresden University of Technology, Dresden, Germany.

The conference included an application presentation of ANSYS 3D Simulation as well as a Panel Discussion concerning EUR ACE-the European quality label for engineering degree programs. The panel discussion was moderated by Alexandru Borcea, President of the Employers Commission ARACIS (Romanian Agency for Quality Assurance in Higher Education) and President of the Romanian Association for Electronic and Software Industry and Marian Vladescu, Member of the Employers Commission ARACIS.

Three oral sections followed, chaired by Ismail Tavman, Dorel Aiordachioaie, Ioan Ileana, Carmen Gerigan, and Detlef Bonfert, Vlad Cehan along with four poster sessions supervised by Dr. Heinz Wolhrabe, Dresden University of Technology. As General Poster Session Chair, Dr. Wohlrabe was involved in organizing posters evaluation criteria as well as the heterogeneous review teams. More than 20 evaluators were involved in the evaluation process. Each poster was evaluated by three evaluators' team, one for the short oral presentation (3 minutes), one for the poster layout impact and one for the discussion with the author.

SIITME 2012 was an IEEE Hu&Ro Joint Chapter Conference and, after the evaluation, the papers of the highest scientific value are included in the IEEE Xplore database. The members of the Steering and the scientific committees have participated at evaluation process.

The closing ceremony coincided with the birthday of Prof. Illyefalvi-Vitez, vice-chair of CPMT Hu&Ro Joint Chapter and long standing organizer of SIITME. It was a possibility to underscore his long involvement, as organizer and participant, in SIITME conference.

At the closing ceremony, the best scientists were awarded. The General Chair of the Conference, Prof. Paul Svasta, the initiator of SIITME event, presented the awards to the participants. *Excellent presentation award for senior scientist* was given to Nelu Blaz, Faculty of Technical Sciences Novi Sad, *best presentation award for senior scientist* was given to Mihai Daraban, Technical University of Cluj Napoca. *Excellent poster award for senior scientists* was given to David Busek, Czech Technical University in Prague and Ovidiu Pop, Technical University of Cluj Napoca. *Best poster award* was given to Reka Batorfi, Budapest University of Technology and Economics. *Excellent poster award for young scientists* was given to Attila Bonyar, Budapest University of Technology and Economics, Tamas Hurtony, Budapest University of Technology and Economics and Vinu Venkatraman, École Polytechnique Federale de Lausanne.

During the cultural program of the conference, the organizers made their best efforts to give an insight into the local specialties and to present some of the surrounding sites and events including the Alba Iulia Fortress and the changing of the guard ceremony. The program presented a good opportunity for networking which forecasts future scientific collaborations.

We are eagerly anticipating the next edition held in Galati, Romania, 24–27 October 2013!

Celebrating the birthday of Prof. Zsolt Illyefalvi-Vitez. First row from left to right, Prof Paul Svasta, Prof Zsolt Illyefalvi-Vitez

Awarding ceremony of SIITME 2012 (from left to right Prof. Paul Svasta, Dr. Heinz Wohlrabe, Prof. Dan Pitica, Attila Bonyar, Reka Batorfi, Prof. Illyefalvi-Vitez, Tamas Hurtony, David Busek, Nelu Blaz, Mihai Daraban)

Publication News....

2012 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among 240 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

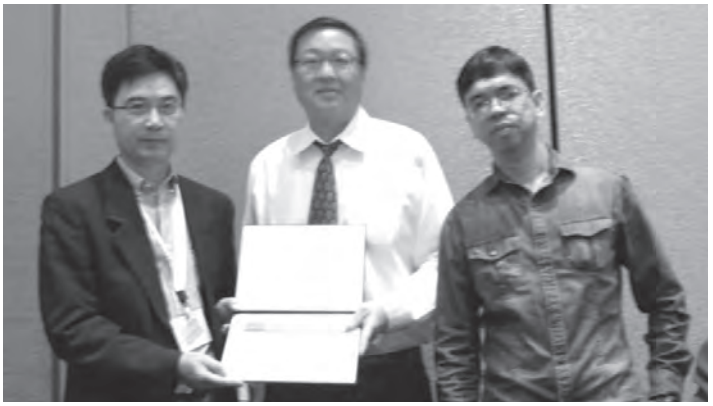
The awards were presented at the 63rd Electronic Components and Technology Conference (ECTC), May 2013.

Subscribers to this publication can access the papers on-line in IEEE Xplore at: http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870

Packaging Technologies Category

"Silicon Carbide Power Modules for High-Temperature Applications," Palmer, M.J.; Johnson, R.W.; Autry, T.; Aguirre, R.; Lee, V.; Scofield, J.D., *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 2, no. 2, pp. 208, 216, Feb. 2012 doi: 10.1109/TCPMT.2011.2171343

Abstract: A hermetic multichip power package for silicon carbide devices that will operate at 200°C ambient and switch 50–100 A has been developed. The Al_2O_3/MoCu structure, in which the SiC junction field-effect transistors and diodes are attached, was designed to hermetically seal the device areas. Details of the materials and processes used to fabricate the package are discussed. Die attach, ribbon bonding, and lid attach, as well as thermal modeling, electrical testing, and thermal cycling results are also described. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6081910&isnumber=6142639



(left to right) Editor-in-Chief Kuo-Ning Chiang, authors Rizal Aguirre and Victor Lee

Advanced Packaging Category

"Compact High-Gain mmWave Antenna for TSV-Based System-in-Package Application," Sanming Hu; Yong-Zhong Xiong; Lei Wang; Rui Li; Jinglin Shi; Teck-Guan Lim, *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 2, no. 5, pp. 841, 846, May 2012 doi: 10.1109/TCPMT.2012.2188293

Abstract: This paper presents a cavity-backed slot (CBS) antenna for millimeter-wave applications. The cavity of the antenna is fully filled by polymer material. This filling makes the fabrication of a silicon CBS antenna feasible, reduces the cavity size by 76.8%, and also maintains the inherent high-gain and wide bandwidth. In addition, a through-silicon via-based architecture is proposed to integrate the 135-GHz CBS antenna with active circuits for a complete system-in-package. Results show that the proposed structure not only reduces the footprint size but also suppresses the electromagnetic interference. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6175932&isnumber=6194283

Components: Characterization and Modeling Category

"Microstructurally Adaptive Model for Primary and Secondary Creep of Sn-Ag-Based Solders," Kumar, P.; Zhe Huang; Chavali, S.C.; Chan, D.K.; Dutta, I.; Subbarayan, G.; Gupta, V., *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 2, no. 2, pp. 256, 265, Feb. 2012 doi: 10.1109/TCPMT.2011.2173494

Abstract: Sn-Ag-based solders are susceptible to appreciable microstructural coarsening due to the combined effect of thermal and mechanical stimuli during service and storage. This results in evolution of the creep properties of the solder over time, necessitating the development of a thermo-mechanical history-dependent creep model for accurate prediction of the long-term reliability of microelectronic solder joints. In this paper, the coarsening behavior of Ag_3Sn and Cu_6Sn_5 precipitates in ball grid array-sized joints of Sn-3.8Ag-0.7Cu solder attached to Ni bond-pads with

(left to right) Editor-in-Chief Kuo-Ning Chiang, authors Sri Chaitra Chavali and Vikas Gupta

four different thermo-mechanical histories is reported. Because of the substantial numerical superiority of Ag_3Sn over Cu_6Sn_5, it was inferred that the evolution of mechanical properties during aging is controlled largely by the coarsening of Ag_3Sn. An effective diffusion length ($\bar{x}$) for Ag diffusion in Sn was defined, and it is shown to adequately describe the thermo-mechanical history dependence of Ag_3Sn particle size. The shear creep behavior of these joints was experimentally characterized, and the entire creep data were fitted to a unified model combining exponential primary creep and power-law steady state creep. The parameter $\bar{x}$ was then incorporated into the creep equation to produce a unified creep model, which can adapt to thermo-mechanical history-dependent microstructural coarsening in the solder. Predictions using this creep law show very good agreement with experimental creep data for several different test and microstructural conditions. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6095338&isnumber=6142639

(left to right) Editor-in-Chief Kuo-Ning Chiang, author Xiaomin Duan

Electrical Performance of Integrated Systems Category

"Extension of the Contour Integral Method to Anisotropic Modes on Circular Ports," Xiaomin Duan; Rimolo-Donadio, R.; Bruns, H.; Schuster, C., *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 2, no. 2, pp. 321, 331, Feb. 2012 doi: 10.1109/TCPMT.2011.2174823

***Abstract*:** In the analysis of power/ground planes in multilayer substrates, circular ports are often used for modeling of via transitions. The electric and magnetic fields on excited ports are usually assumed to be isotropic. This assumption may not hold in certain scenarios such as vias in very close proximity, where anisotropic modes can be excited. This paper first extends voltage and current definitions of circular ports to account for the non-uniform field distribution along the port perimeter and the anisotropic propagating modes. The effect of these modes on the parallel-plate impedance can be captured in the contour integral method (CIM) by discretizing the port perimeter with line segments. However, the computation time grows rapidly as the number of modeled ports increases. Therefore, the CIM is extended here to incorporate analytical modal expressions to improve the computational efficiency based on the new port definition. The derivation starts with solutions under the assumption of infinite planes, and then is expanded to take finite plane boundaries into consideration. Application examples using the extended CIM will be demonstrated and validated against the conventional CIM with ports modeled numerically. The significance of anisotropic propagating modes for dense via arrays will also be discussed. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6095337&isnumber=6142639

Electronics Manufacturing Category

"Testing of Copper Pillar Bumps for Wafer Sort," Tunaboylu, B., *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 2, no. 6, pp. 985, 993, June 2012 doi: 10.1109/TCPMT.2011.2173493

Abstract: Using a copper pillar interconnect in flip chip packaging provides a lead-free solution that is more reliable, and also scalable to very fine pitch. Vertical probe card technology, also called buckling beam technology, was used in characterization of wafer probe process and electrical contact on solder bumps and copper pillars at 150 μm pitch arrays. Probe contact was investigated by modeling the scrub, penetration or deformation on a bump under various conditions of wafer probe and experimentally tested on wafers on copper pillars, solder bumps of different metallurgies or sheet wafers. A single-probe contact test system was devised to study the contact behavior of a probe on a bump. Various probe tip geometries including wedge, pointed and flat, were studied. Probing procedures were investigated for achieving reliable electrical contact for large pitch area array bumps as well as fine pitch, 50 µm, copper pillar array bumps using two different wafer test technologies. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6085599&isnumber=6205691

Have You Read Them? The Most Downloaded CPMT Transactions Papers

What might you be missing in the CPMT literature? Following is a list of most downloaded papers in First Quarter 2013. Subscribers can access these and other papers in IEEE Xplore.

"Die Attach Materials for High Temperature Applications: A Review," Manikam, V.R.; Kuan Yew Cheong**,** *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, no. 4, pp. 457, 478, April 2011. doi: 10.1109/TCPMT.2010.2100432

Abstract: The need for high power density and high temperature capabilities in today's electronic devices continues to grow. More robust devices with reliable and stable functioning capabilities are needed, for example in aerospace and automotive industries as well as sensor technology. These devices need to perform under extreme temperature conditions, and not show any deterioration in terms of switching speeds, junction temperatures, and power density, and so on. While the bulk of research is performed to source

and manufacture these high temperature devices, the device interconnect technology remains under high focus for packaging. The die attach material has to withstand high temperatures generated during device functioning and also cope with external conditions which will directly determine how well the device performs in the field. This literature work seeks to review the numerous research attempts thus far for high temperature die attach materials on wide band gap materials of silicon carbide, gallium nitride and diamond, document their successes, concerns and application possibilities, all of which are essential for high temperature reliability. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5732748&isnumber=5746823

"High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)," Joohee Kim; Jun So Pak; Jonghyun Cho; Eakhwan Song; Jeonghyeon Cho; Heegon Kim; Taigon Song; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Min-Suk Suh; Kwang-Yoo Byun; Joungho Kim, *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, no. 2, pp. 181, 195, Feb. 2011, doi: 10.1109/TCPMT.2010.2101890

Abstract: We propose a high-frequency scalable electrical model of a through silicon via (TSV). The proposed model includes not only the TSV, but also the bump and the redistribution layer (RDL), which are additional components when using TSVs for 3-D integrated circuit (IC) design. The proposed model is developed with analytic *RLGC* equations derived from the physical configuration. Each analytic equation is proposed as a function of design parameters of the TSV, bump, and RDL, and is therefore, scalable. The scalability of the proposed model is verified by simulation from the 3-D field solver with parameter variations, such as TSV diameter, pitch between TSVs, and TSV height. The proposed model is experimentally validated through measurements up to 20 GHz with fabricated test vehicles of a TSV channel, which includes TSVs, bumps, and RDLs. Based on the proposed scalable model, we analyze the electrical behaviors of a TSV channel with design parameter variations in the frequency domain. According to the frequency-domain analysis, the capacitive effect of a TSV is dominant under 2 GHz. On the other hand, as frequency increases over 2 GHz, the inductive effect from the RDLs becomes significant. The frequency dependent loss of a TSV channel, which is capacitive and resistive, is also analyzed in the time domain by eye-diagram measurements. Due to the frequency dependent loss, the voltage and timing margins decrease as the data rate increases. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5739019&isnumber=5739011

"3-D Packaging With Through-Silicon Via (TSV) for Electrical and Fluidic Interconnections," Khan, N.; Li Hong Yu; Tan Siow Pin; Soon Wee Ho; Kripesh, V.; Pinjala, D.; Lau, J.H.; Toh Kok Chuan *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, no. 2, pp. 221, 228, Feb. 2013, doi: 10.1109/TCPMT.2012.2186297

Abstract: In this paper, a liquid cooling solution has been reported for 3-D package in package-on-package format. A high heat dissipating chip is mounted on a silicon carrier, which has copper through-silicon via (TSV) for electrical interconnection and hollow TSV for fluidic circulation. Heat transfer enhancement structures have been embedded in the chip carrier. Cooling liquid, de-ionized water is circulated through the chip carrier and heat from the chip is extracted. The fluidic channels are isolated from electrical traces using hermetic sealing. The research work has demonstrated liquid cooling solution for 100 W from one stack and total of 200 W from two stacks of the package. The fluidic interconnections and sealing techniques have been discussed. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6410399&isnumber=6428681

"Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring," Jonghyun Cho; Eakhwan Song; Kihyun Yoon; Jun So Pak; Joohee Kim; Woojin Lee; Taigon Song; Kiyeong Kim; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Minsuk Suh; Kwangyoo Byun; Joungho Kim, *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 1, no. 2, pp. 220, 233, Feb. 2011, doi: 10.1109/TCPMT.2010.2101892

Abstract: In three-dimensional integrated circuit (3D-IC) systems that use through-silicon via (TSV) technology, a significant design consideration is the coupling noise to or from a TSV. It is important to estimate the TSV noise transfer function and manage the noise-tolerance budget in the design of a reliable 3D-IC system. In this paper, a TSV noise coupling model is proposed based on a three-dimensional transmission line matrix method (3D-TLM). Using the proposed TSV noise coupling model, the noise transfer functions from TSV to TSV and TSV to the active circuit can be precisely estimated in complicated 3D structures, including TSVs, active circuits, and shielding structures such as guard rings. To validate the proposed model, a test vehicle was fabricated using the Hynix via-last TSV process. The proposed model was successfully verified by frequency- and time-domain measurements. Additionally, a noise isolation technique in 3D-IC using a guard ring structure is proposed. The proposed noise isolation technique was also experimentally demonstrated; it provided –17 dB and –10dB of noise isolation between the TSV and an active circuit at 100 MHz and 1 GHz, respectively. URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5739017&isnumber=5739011

"Substrate-Integrated Waveguide Bandpass Filters With Planar Resonators for System-on-Package," Wei Shen; Wen-Yan Yin; Xiao-Wei Sun; Lin-Sheng Wu, *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, vol. 3, no. 2, pp. 253, 261, Feb. 2013, doi: 10.1109/TCPMT.2012.2224348

Abstract: This paper proposes some novel substrate-integrated waveguide (SIW) bandpass filters combined with planar resonators. According to specific topologies, microstrip lines with different electrical lengths are introduced into their designs. Their corresponding phase-shift characteristics are used to obtain the desired couplings between SIW cavities and the microstrip resonator. Two third-order filter samples are realized. One has a single transmission zero below the passband and the other possesses a quasi-elliptic response. Further, a fourth-order filter is developed by effectively superpositing two individual third-order topologies. It shows better frequency selectivity and flat in-band group delay, with good agreement between the measured and the simulated S-parameters. Their compactness and high rejection in the stopbands make them very suitable for system-on-package URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=6397590&isnumber=6428681

Conference News....

63rd Electronic Components and Technology Conference (ECTC): A True Banner Year

Submitted by Henning BraunischAssistant Program Chair, IEEE ECTC 2014

The 63rd Electronic Components and Technology Conference held May 28–31, 2013 for the first time at The Cosmopolitan of Las Vegas, Nevada, USA, set new records for this annual event in terms of number of attendees, abstracts received, presentations, exhibitors, and sponsorship. Widely considered to be the premier global conference for electronic packaging and interconnect technologies, this year's technical program featured 36 oral presentation sessions, four interactive presentation sessions, one student poster session, 16 professional development courses (PDCs), two special Tuesday sessions, and three evening panel and plenary sessions. In addition to daily luncheons, nightly receptions, a raffle drawing, and 95 exhibitors, the 63rd ECTC provided a multitude of options for technical engagement, networking, and business development.

Based on the increased number of attendees this year, the microelectronic packaging industry continued to show it is in a growth mode. Over 1300 attendees participated in ECTC this year, an increase of about 100 over last year's attendance. 646 abstracts were submitted for this year's conference from authors in 31 U.S. states and 26 countries, reflecting ECTC's global reach. 43% of the submitted abstracts were from universities and educational institutions, 43% were from corporations, and 14% from research institutes. 377 of these abstracts were accepted for presentation in oral, interactive presentation, and student poster sessions, reflecting a total acceptance rate of 58%. Once again this year, the Executive Committee formed a 3D/TSV workgroup to coordinate the 12 sessions dedicated to this important technology area. Chris Bower of Semprius led the workgroup comprised of members from all of the technical subcommittees to create topically-focused sessions on interposers, TSV fabrication, and design, modeling, and characterization of 3D systems. After successful introduction last year as a replacement of traditional poster sessions, Interactive Presentations continued to reflect the importance of the one-on-one interaction with authors that these presentations can provide. The four Interactive Presentation sessions also featured large video screens displaying quad chart summaries that provided at-a-glance information about the author's works. Once again, the technical subcommittees did an outstanding job in creating the technical program for ECTC, and their tireless efforts are very much appreciated!

On Tuesday, ECTC's PDCs were held, with 333 attendees participating in the 16 courses with topics ranging from 3D integration to multi-physics modeling. Participants in PDCs were eligible for Continuing Education Units at no additional cost. The courses were organized by the PDC Committee chaired by Kitty Pearsall of IBM.

The International Electronics Manufacturing Initiative (iNEMI) held their North American Workshop at ECTC again this year. This meeting, intended to solicit input for the 2013 iNEMI Research Priorities, was open to all conference attendees.

The special technical session chaired by Sam Karikalan of Broadcom on "The Role of Wafer Foundries in Next Generation Packaging" drew a large audience to hear representatives from several major wafer foundries to discuss the changes and challenges for their entry into the packaging world. Jerry Tzou (TSMC), David McCann (GLOBALFOUNDRIES), Kurt Huang (UMC), Jon Casey (IBM), and Herb Huang (SMIC) were the invited speakers.

A special modeling session held Tuesday afternoon and co-chaired by Yong Liu of Fairchild Semiconductor and Dan Oh of Altera on "Modeling and Simulation Challenges in 3D Systems" was also well attended. It included interesting technical paper

The 63rd ECTC Executive Committee

General Chair Wolfgang Sauter congratulates Maciej Wojnowski of Infineon, winner of the 62nd ECTC Outstanding Session Paper award

The 2013 Technology Corner was the largest in ECTC history in terms of number of exhibitors

presentations by Cielution, IMEC, Rambus, and Georgia Tech, as well as top notch keynotes by Eric Beyne (IMEC) and Vikram Jandhyala (University of Washington & Nimbic).

Tuesday evening, students were invited to participate in the annual ECTC Student Reception, hosted by Eric Perfecto of IBM. Students had the opportunity to interact with technical subcommittee chairs to learn about the abstract selection process and network with industry professionals. Session chairs and speakers attended the General Chair's Reception to welcome them to ECTC.

Rounding out the opening day, Ricky Lee of the Hong Kong University of Science and Technology and Kouchi Zhang of TU Delft & Philips Lighting co-chaired the ECTC Panel Session on "LED for Solid-State Lighting—For a Brighter Future". Ling Wu (China Solid-State Lighting Alliance), Mark McClear (Cree Components), Ron Bonne (Philips Lumileds), Nils Erkamp (TNO), and Michael McLaughlin (Yole Development) were the invited speakers.

Regular technical sessions began on Wednesday, starting at 8 AM each day with six parallel sessions running each morning and afternoon, for a total of 36. Each day started with a Speaker's Breakfast where session chairs and speakers gathered for a welcome message from ECTC Program Chair Beth Keser of Qualcomm.

The ECTC Plenary Session chaired by Lou Nicholls of Amkor

3D technologies proved to be the hot topic again this year. Up to 200 attendees packed the conference halls to hear about the latest developments in 3D bonding and assembly, interposer technology, and TSV manufacturing. Flip chip and wafer level packaging sessions also continued to draw a significant number of attendees. Sessions on package reliability, solder and material characterization, innovative testing, and optoelectronics were also popular and illustrate the breadth of technologies that were presented this year.

Chris Welty of IBM was Wednesday's ECTC Luncheon keynote speaker, where he spoke about engineering challenges in building Watson, a question answering computer system designed to compete against humans on the American TV show "Jeopardy!" As demonstrated in the presentation, ultimately the system was able to defeat the best players of the game's history, inspiring the audience in attendance to take on today's diverse challenges in microelectronic packaging. The 2012 ECTC best paper awards were also presented.

Wednesday evening's events began with the Exhibitor Reception held in the Technology Corner exhibit. This year's Technology Corner consisted of 95 exhibitors, by far the most ever at ECTC, and the exhibition hall was a great setting for networking and for exhibitors to present the most recent advances in services, equipment, and materials.

That night's ECTC Plenary Session, "Packaging Challenges Across the Wireless Market Supply Chain", was chaired by Lou Nicholls of Amkor. Speakers Timo Henttonen (Nokia), Steve Bezuk (Qualcomm), Waite Warren (RFMD), Roger St. Amand (Amkor), and Soonjin Cho (SEMCO) discussed wireless markets, applications, and technologies and the challenges posed by the advanced design of handheld devices such as smartphones.

CPMT sponsored the Thursday luncheon where the Society presented its 2013 awards. Among others, John Lau of ITRI was honored with the 2013 CPMT Award for his contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education

Plenty of networking during the Gala Reception

in advanced packaging. Rolf Aschenbrenner of Fraunhofer IZM received the 2013 CPMT David Feldman Outstanding Contribution Award.

The 64th ECTC planning meeting was held Thursday afternoon, chaired by Alan Huffman of RTI International who will serve as the Program Chair for next year's ECTC. Alan detailed the 63rd ECTC statistics and presented the timeline for the 64th ECTC which will be held May 27–30, 2014 at the Walt Disney World Swan & Dolphin resort in Lake Buena Vista, Florida, USA. CPMT Representative C. P. Wong introduced Henning Braunisch of Intel as the Assistant Program Chair for the 64th ECTC.

The traditional Gala Reception was held Thursday evening. Attendees and volunteers enjoyed great food and great conversation with friends and colleagues. General Chair Wolfgang Sauter thanked attendees, exhibitors, sponsors, and volunteers for helping to make the 63rd ECTC one of the most successful conferences to date.

Thursday night was the CPMT Seminar, "Advanced Low Loss Dielectric Materials for High Frequency and High Bandwidth Applications", co-chaired by Kishio Yokouchi of Fujitsu Interconnect Technologies and Venky Sundaram of Georgia Tech and with invited speakers Yuya Suzuki (Zeon), Yasuyuki Mizuno (Hitachi Chemical), Shin Teraki (NAMICS), and Hirohisa Narahashi (Ajinomoto).

Although Friday was the last day of the conference, both morning and afternoon sessions were very well attended, a testament to the strength of the technical program from beginning to end. The Friday ECTC Program Chair's luncheon was a fun-filled event, as always, with ECTC Treasurer Tom Reynolds overseeing the annual raffle drawing where many prizes were given out including an Xbox with Kinect and a Surface tablet computer. C. P. Wong awarded Wolfgang Sauter the General Chair award in recognition of his leadership of the 63rd ECTC.

The first Call for Papers for the 64th ECTC and a link to ECTC's LinkedIn site are available at www.ectc.net. There you can also find a link to a Flickr site with pictures from ECTC. This year's abstract deadline is October 14, 2013. In addition to abstracts for papers, proposals are also welcomed from those interested in teaching PDCs. We look forward to seeing you next year in Lake Buena Vista, Florida, USA (Disney World) for the 64th ECTC!

IEEE Xplore® Table of Contents Alert

Any technologist – **member or non-member** – is welcome to receive alerts when upcoming issues of our CPMT *Transactions* are posted to the IEEE's Xplore database and all the papers are available for downloading. This is a handy way to scan the issue's Table of Contents and quickly learn about novel approaches to packaging, modeling, reliability, materials, assembly and other topics.

The website link is:ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

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Here are the journals we suggest you select for monitoring:

Transactions on Components, Packaging and Manufacturing Technology
Transactions on Semiconductor Manufacturing

Home

2013 International Conference on Electronic Packaging Technology

(ICEPT 2013)

August 11~14, 2013, Dalian, China

The 14th International Conference on Electronic Packaging Technology (ICEPT 2013) will be held in Dalian, China, from August 11 to 14, 2013. The ICEPT 2013 is hosted by Chinese Institute of Electronics (CIE) and organized byElectronic Manufacturing and Packaging Technology Society (EMPT) of CIE and Dalian University of Technology. As one of the most famous international conferences on electronic packaging technology, the conference has received strong support from IEEE CPMT and active involvement from IMAPS, ASME and iNEMI, and was highly appreciated by Chinese Institute of Electronics and China Association for Science and Technology (CAST).

ICEPT 2013 is a four-day event, featuring technical sessions, invited talks, professional development courses/forums, exhibition, and social networking activities. It aims to cover the latest technological developments in electronic packaging, manufacturing and packaging equipment, and provide opportunities to explore the trends of research and development, as well as business in China.

We are looking forward to receiving your papers and meeting you at the conference.

CONFERENCE THEMES: Advanced Packaging & System Integration; Packaging Materials & Processes; Packaging Design and Modeling; High Density Substrate & SMT; Advanced Manufacturing Technologies and Packaging Equipment; Quality & Reliability; Solid State Lighting Packaging & Integration; Emerging Technologies etc.

Guided by

Department of Electronic Information, Ministry of Industry and Information Technology

Department of Higher Education, Ministry of Education

Department of High and New Technology Development and Industrialization, Ministry of Science and Technology

Hosted by

Chinese Institute of Electronics (CIE)

Organized By

Electronic Manufacturing and Packaging Technology Society (EMPT) of Chinese Institute of Electronics (CIE)

Dalian University of Technology (DUT), China

Technically Sponsored By

IEEE-CPMT

General Chair: Prof. Keyun BI

Technical Chair: Prof. Mingliang HUANG, Dr. Yifan GUO

Conference Website: http://www.icept.org

Conference Email: icept2013@vip.163.com

Hosted By CIE — CIE–Electronic Manufacturing and Packaging Technology Society

Technically Sponsored By IEEE — IEEE CPMT — IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Organized By 大连理工大学

Electronic Manufacturing and Packaging Technology Society of Chinese Institute of Electronics （CIE-EMPT）
Beijing Office: Room 411,27 Zhichun Road,Haidian Dist.,Beijing,China 100191
Tel:+86-10-82356605 Fax:+86-10-82356605 E-mail:empt-cie@sohu.com

EMPC 2013 (European Microelectronics Packaging Conference) is the premier international conference organized by IMAPS-Europe and IEEE-CPMT. The program will focus on industrial needs and trends and on academic longer term solutions; This event brings together researchers, innovators, technologists, business and marketing managers with an interest in semiconductor packaging

• Advanced packaging: 3D packaging, TSVs, interposers, wafer level packaging, fan-out WLP and embedded IC package, substrates (flexible, ceramic, laminates), PCB.

• CAD and tools for IO placement for advanced packaging, design for reliability, IC and package co-design, opto & RF package design, thermal & mechanical modeling & simulation.

• MEMS and smart system packaging,

• Innovative packaging for emerging and growing applications: photovoltaic, textile electronics medical, power, LEDs, photonics, optoelectronics...

• Materials, equipment and processes.

• Emerging technologies and novel approaches; microfluidics, carbon nano tubes, ...

• Assembly manufacturing and business aspects of the industry.

• Reliability, test & characterization, electromigration, thermal management.

• Advanced interconnections: flip-chip, interconnections for advanced CMOS process nodes, WLP metallurgies, bumping techniques, non-traditional interconnections, PCB solutions.

Organized by *Co-organizers* *Media sponsors*

November 11–13, 2013

Kyoto University Clock Tower Centennial Hall, KYOTO, JAPAN

http://www.vlsi-pkg-ws.org/

"Advanced Packaging for 100 G and Beyond"

"IEEE CPMT Symposium Japan" is recognized international symposium for leading-edge packaging technologies.

The symposium started as "The VLSI Packaging Workshop in Japan" in 1992 and held every two years. To cover the wide area of electronics packaging, the committee refurbished the workshop, and started the new symposium—IEEE CPMT Symposium Japan in 2010. Due to ever increasing recent electronics demands, we'll expand the symposium to an annual event this year. IEEE CPMT Symposium Japan will provide component, packaging, and manufacturing researchers who are extending their activities beyond borders with opportunities to exchange technical knowledge and perspective. Bring your latest research results and share with the participants who are experts from the industry and the academia, and discuss with them. Anybody contributing to the achievement of a sustainable society through electronics is very welcome at this symposium. The following areas of technology are primary interest to the participants:

Topics of Interest Include:

+ Optoelectronics Packaging & Subsystems
+ 3D Packaging & Chip on Chip
+ Packaging for Sensors, MEMS, and Bio Devices
+ Board-Level Integration
+ Integrated Substrate
+ Laminated Materials & Processing
+ Electrical Performance & Thermal Management
+ Materials for Packaging, Wafer Process &High-Speed Application
+ Packaging for High-Speed Interconnection
+ Packaging for Automobile
+ Advanced Fine Pitch Packaging
+ Assembly & Packaging Challenges for Cu/Low-k Chips
+ Micro Bumping Technology, Wafer Level CSP
+ Nanotechnology, Emerging Technologies
+ RF Components & Modules / RF Tags

General Chair: Shigenori Aoki (Fujitsu Laboratories, Ltd.)

Vice Chairs: Shigeru Nakagawa (IBM Research - Tokyo) and S.W. Ricky Lee (Hong Kong University of Science and Technology)

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Publication Chairs: Nobuhiro Imaizumi (Fujitsu Laboratories, Ltd.) and Shinya Takyu (Toshiba Corporation) and Atsushi Nakamura (Renesas Electronics Corporation)

Arrangement Chairs: Tadaaki Mimura (Panasonic Corporation) and Katsumi Terada (Toray Engineering Co.,Ltd.)

EDAPS 2013

2013 IEEE Electrical Design of Advanced Packaging & Systems Symposium

December 12-14 & 15, 2013. Nara, Japan

Scope of Symposium

The IEEE Electrical Design of Advanced Packaging & Systems (EDAPS) symposium has been one of the most important events in Asia Pacific region for the researchers and developers related to the electrical design issues on chip, package and system levels. The EDAPS symposium consists of paper presentations, industry exhibitions, workshops and tutorials. The 2013 EDAPS will be held in Nara of Japan from December 12 to 14, 2013. Additionally, a special joint workshop with EMC Compo2013 will be embedded on Dec. 15th. The technical program of the symposium not only addresses the current technical issues but also brings out the challenges facing IC design, SiP/SoP packaging, EMI/EMC, and EDA tools and most importantly the challenge issues in advanced 3-D IC and packaging design. The symposium provides a major platform for researchers, designers and developers from diverse fields to exchange knowledge and build up network and community.

Paper Topics of Interest

- Signal Integrity
- Substrate Technology for Package and PCB
- Power Integrity / Ground Noise
- Time/Frequency Domain Measurement Techniques
- 3DIC / 3D-Stacked IC
- SiP/SoP
- Embedded Passives
- Electromagnetic Compatibility (EMC)
- Design and Modeling for High-speed Channels and Interconnects
- Package Reliability
- RF/Microwave Package
- Advanced Simulation Tools and CAD
- Testing on 3DIC and SiP
- Others

EDAPS 2013 in Nara will be organized in conjunction with EMC Compo 2013, which will be held on Dec. 15-18, 2013 at the same venue. A special joint workshop will be planned on Dec. 15th. Details of EMP Compo are available at http://www.emccompo2013.org/

www.edaps2013.org

64th ECTC Call for Papers

First Call For Papers

64th Electronic Components and Technology Conference

www.ectc.net

To be held May 27 - May 30, 2014

at the Walt Disney World Swan and Dolphin Resort, Lake Buena Vista, Florida, USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:
3D integration, embedded, and wafer level packaging, flip chip, advanced substrates, novel assembly technologies, interposers, TSVs, MEMS & sensors, electronic (digital, analog, & RF),and optoelectronic & photovoltaic device packaging.

Applied Reliability:
3D package reliability, characterization and test methods, interconnection reliability; solder and material characterization, and next generation/novel packaging reliability.

Assembly and Manufacturing Technology:
Assembly challenges and solutions, manufacturing aspects of 3D/TSV, manufacturing challenges of wafer thinning and flip chip processing.

Electronic Components & RF:
Components (including embedded components) and modules for RF/THz systems and bio applications, metamaterials, wireless sensors, RFID, RF MEMS, flexible & printed electronics, "green" RF electronics, wireless power transmission, power scavenging components, nano-based RF structures, and low-power RF designs.

Emerging Technologies:
Emerging packaging concepts and technologies, emerging 3D packaging concepts, novel approaches to packaging, organic IC & TFT, microfluidics and MEMs, anti-counterfeiting packaging, and packaging for biosensing.

Interconnections:
First- and second-level interconnections: designs, structures, processes, performance, reliability, test including TSV, Si interposer, and interconnections for 3D integration, flip chip, solder bumping and Cu-pillar, wafer-level packaging, advanced wirebonds, non-traditional interconnections (e.g. ECA, CNT, graphene, optical, etc), electromigration for 2.5D and 3D, substrates and PCB solutions for the next generation systems, system packaging and heterogeneous integration.

Materials & Processing:
Adhesives and adhesion, lead free solder, novel materials and processing; underfills, mold compounds, and dielectrics, emerging materials and processing for 3D.

Modeling & Simulation:
Thermal, mechanical, electrical modeling and related measurements, 3D/TSV design and modeling, signal and power integrity, fracture and warpage in packages, material and fabrication modeling, first-level and second-level interconnects, high-speed interconnects.

Optoelectronics:
Fiber optical interconnects, active optical cables, parallel optical transceivers, silicon and III-V photonics devices, optical chip-scale and heterogeneous integration, micro-optical system integration and photonic system-in-package, optoelectronic assembly and reliability, materials and manufacturing technology, high-efficiency LEDs and high power lasers, and integrated optical sensors.

Interactive Presentations:
Papers may be submitted on any of the listed major topics; presentation of papers in an interactive format is highly encouraged at ECTC. Interactive presentations allow significant interaction between the presenter and attendees, and are especially suited for material that benefits from more explanation than is practical for oral presentations. Highly rated abstracts not fitting the theme of an oral session or submitted specifically for interactive presentation, and abstracts that are selected at the discretion of the program chair are included in the Interactive Presentation sessions.

You are invited to submit a <750-word abstract that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net. If you have any questions, contact:

Alan Huffman, 64th ECTC Program Chair
RTI International
3040 Cornwallis Rd.
Research Triangle Park, NC 27709
Phone: +1-919-248-9216
Email: huffman@rti.org

Abstracts must be received by October 14, 2013. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/ Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 14, 2013. If you have any questions, contact:

Kitty Pearsall, 64th ECTC Professional Development Courses Chair
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Austin, TX 78758
Phone: +1-512-286-7957
Email: kittyp@us.ibm.com

Upcoming CPMT Sponsored and Cosponsored Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the CPMT Society sponsors and supports a number of global and regional conferences, workshops and other techical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through IEEE Xplore.

For details go to: www.cpmt.ieee.org

Name: 2013 14th International Conference on Electronic Packaging Technology (ICEPT)
Location: Dalian, China
Dates: August 11–14, 2013

Name: 2013 35th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)
Location: Las Vegas, NV USA
Dates: September 8–13, 2013

Name: 2013 European Microelectronics Packaging Conference (EMPC)
Location: Grenoble, France
Dates: September 9–12, 2013

Name: 2013 IEEE 59th Holm Conference on Electrical Contacts (Holm 2013)
Location: Newport, RI USA
Dates: September 22–25, 2013

Name: 2013 19th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)
Location: Berlin, Germany
Dates: September 25–27, 2013

Name: 2013 IEEE International 3D Systems Integration Conference (3DIC)
Location: San Francisco, CA USA
Dates: October 2–4, 2013

Name: 2013 Workshop on Accelerated Stress Testing & Reliability (ASTR)
Location: San Diego, CA USA
Dates: October 9–11, 2013

Name: 2013 8th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)
Location: Taipei, Taiwan
Dates: October 22–25, 2013

Name: 2013 IEEE 22nd Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
Location: San Jose, CA USA
Dates: October 27–30, 2013

Name: 2013 IEEE CPMT Symposium Japan (Formerly VLSI Packaging Workshop of Japan)
Location: Kyoto, Japan
Dates: November 11–13, 2013

Name: 2013 IEEE 15th Electronics Packaging Technology Conference (EPTC 2013)
Location: Singapore, Singapore
Dates: December 11–13, 2013

Name: 2013 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)
Location: Nara, Japan
Dates: December 12–15, 2013

IEEE Components, Packaging and Manufacturing Technology Society
Marsha Tickman, Executive Director
445 Hoes Lane
Piscataway, NJ 08854 USA

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3. Select the "Classics" tab from the top of the page. Under this tab you will find a listing of all the Free titles.

Here are a few examples of available books in pdf format: (more added every year)

1. *Lead-Free Electronics: iNEMI Projects Lead to Successful Manufacturing* by E. Bradley, C. Handwerker, J. Bath, R. Parker and R. Gedney; Publication Date: 2007
2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

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