Components, Packaging, and Manufacturing Technology Society Newsletter

THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

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President's Column....

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2014–2015 CPMT President
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Dear CPMT members,

As the holiday season is approaching, it whisks us into a new year before we know it. And as 2015 draws to a close, so does my presidency. This is my last president's message to you, and we have a lot to celebrate together!

Since my last message in June, I attended **ICEPT 2015 in August in Changsha, China**. CPMT has been the technical sponsor of this largest packaging conference in China for many years. I am very encouraged to see the growing number of attendees, high technical quality of papers, and overall impact on R&D in China. During the conference, Professor Chris Bailey, CPMT VP, Conferences and I gave an opening day talk on "3D Printing: Hype, Hope, or Happening." And the CPMT/EDS Shanghai Joint Chapter hosted an information booth to outreach to packaging professionals in China.

I am also very pleased with the **formation of two new Chapters in Beijing and Korea** which have been fully approved by IEEE MGA. As Asia is playing a more and more important role in the Semiconductor segment, the establishment of these two Chapters strategically positions CPMT to extend our influence and provide services to our members in the region. I look forward to the continued growth of the CPMT membership and Chapters in Asia.

There are two additional important conferences in 2015:

- **December 2–4 in Singapore: IEEE 17th Electronics Packaging and Technology Conference (EPTC).** CPMT-sponsored flagship conference in Singapore.
- **December 15–17 in Seoul, Korea: IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)**. Annual conference sponsored by the CPMT Technical Committee on Electrical Design, Modeling & Simulation. I will be attending the conference to give an opening day keynote and meet the leadership of the new CPMT Korea chapter.

As my presidency nears the end of the term, I am very excited to inform you that **Jean Trewhella** from Global Foundries will be the new president of CPMT for 2016–2017. At the CPMT Board of Governors (BoG) meeting in Dallas in November, a new leadership team of CPMT officers was also approved. I want to congratulate Jean and the new CPMT leadership team. I will be working closely with them to ensure a smooth transition.

Looking back on the past two years, it was my honor to serve as CPMT president and had many opportunities to travel globally and meet many CPMT members/volunteers. I am beyond impressed by the diverse talent in our Society and inspired by the energy and passion of our volunteers. At the beginning of my presidency, I laid out and communicated two priorities:

1) **Influence emerging and disruptive technologies** through
   a) long-term strategic planning within our society, defining CPMT positions on 3D printing, Si Photonics, Power electronics, and other hot topics,

(continued on page 3)

NEWSLETTER SUBMISSION DEADLINES:

1 January 2016 for Winter issue 2016
1 March 2016 for Spring issue 2016
30 June 2016 for Summer issue 2016
30 September 2016 for Fall issue 2016

Submit all material to nsltr-input@cpmt.org

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2015 term-end: Regions 1–6,7,9—Phil Garrou, Patrick Thompson; Region 8—Karlheinz Bock; Region 10—Kuo-Ning Chiang, Charles W. Lee, Daniel Lu

2016 term-end: Regions 1–6,7,9—Li Li, Ning-Cheng Lee, James E. Morris, Jeffrey C. Suhling; Region 8—Toni Mattila, Gilles Poupon

2017 term-end: Regions 1–6,7,9—Avram Bar-Cohen, Darvin Edwards, Beth Keser, CP Wong; Region 8—Mervi Paulasto-Kröckel; Region 10—Masahiro Aoyagi

CPMT Society Newsletter

Editor-in-Chief: Kitty Pearsall kitty.pearsall@gmail.com

CPMT Archival Publications

Transactions on Components, Packaging and Manufacturing Technology

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3D/TSV:
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Program Director: Jean Trewhella, Jean.Trewhella@globalfoundries.com

Lecturers: Muhannad Bakir, Ph.D., Avram Bar-Cohen, Ph.D., Moises Cases, Rajen Chanchani, Ph.D., William T. Chen, Ph.D., Badih El-Kareh, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., George G. Harman, Ph.D., R. Wayne Johnson, Ph.D., Beth Keser, Ph.D., John H. Lau, Ph.D., Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., Michael Pecht, Ph.D., Eric D. Perfecto, Karl J. Puttlitz, Ph.D., Dongkai Shangguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Yutaka Tsukada, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Ralph W. Wyndrum Jr., Ph.D., Jie Xue, Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branch Chapters

Refer to cpmt.ieee.org for CPMT Society Chapters and Student Branch Chapters list

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SFI Logo

b) and strategic collaborations with other IEEE societies such as EDS, PELS, MTT, and non-IEEE organizations such as Semi, IMAPS and ITRS

2) **Increase membership value and expand global membership** through webinars, joint Chapter events, new Chapters, and career development and mentoring opportunities

Now looking back, I am very pleased with the accomplishment and progress we have made together. I am confident about direction of the CPMT society as well as the increased global reach and cross-society collaborations. Special thanks to CPMT officers: **Steve Bezuk, Chris Bailey, Wayne Johnson, Tom Reynolds, Rolf Ashenbrenner, Ricky Lee, Eric Perfecto, Kitty Pearsall, Pat Thompson, Kwang-Lung Lin, Bill Chen, Toni Mattila, Hirofumi Nakajima**, and CPMT Society Executive Director **Marsha Tickman**. Finally, sincere thanks to all the CPMT volunteers and members!

Wishing you and your family health and happiness this holiday season!

CPMT Society News....

Newly-Elected Members of the CPMT Society Board of Governors

In late 2015, CPMT Society members elected six Members- at-Large to the CPMT Board of Governors for the three-year term of 1 January 2016 through 31 December 2018.

Members-at-Large are elected to achieve totals proportionate to the geographic distribution of CPMT members. Any IEEE Region/grouping of Regions determined to have at least 10% of total CPMT members has the proportional number of Member-at-Large positions designated to it for representation on the BoG. The slate of candidates for each year's election is constructed to ensure that the resulting total of newly elected Members-at-Large plus continuing Members-at-Large has the proper proportion of representatives from each Region/grouping of Regions.

Each Region/grouping of Regions has a separate slate of candidates from that Region. CPMT voting members (all CPMT members above the grade of Student) elect Members-at-Large from within their Region only (that is, members in Region 8 vote only for Members-at-Large from Region 8, members in Region 10 vote only for Members-at-Large from Region 10; etc.)

The six newly-elected Members-at-Large will join continuing Members-at-Large (shown below) on the Board of Governors:

From Regions 1–6, 7 and 9: Avram Bar-Cohen, Darvin R. Edwards, Beth Keser, Li Li, Ning-Cheng Lee, James E. Morris, Jeffrey C. Suhling, CP Wong

From Region 8: Toni Mattila, Mervi Paulasto-Kröckel, Gilles Poupon

From Region 10: Masahiro Aoyagi

REGIONS 1-6, 7 AND 9

PHILIP GARROU (M'88, SM'92, F'00) has a PhD in Chemistry. He worked for Dow Chemical from 1975 to 2004. During the 1990s he developed and then ran the Thin Film DIelecrics Business (BCB). He retired from Dow as Global Director of Technology & New Business Development for their Advanced Electronic Materials business unit.

Since 2004 he has kept busy operating his consulting firm Microelectronic Consultants of NC while also serving as contributing editor and blogger ("Insights from the Leading Edge" IFTLE) for Solid State Technology, and as a part time Sr analyst for Yole Development.

Phil has served as Technical VP and President of both IEEE CPMT and IMAPS and is a Fellow of both organizations. He has edited several microelectronic texts including McGraw Hill's "Multichip Module Handbook" in 1998 and Wiley's "Handbook of 3D Integration" Vol 1 & 2 in 2008 and Vol 3 in 2014.

He has won the Milton Kiver Award for Excellence in Electronic Packaging (1994); the IMAPS Ashman Award (2000) for "…the development of wafer level packaging"; the Fraunhoffer International Adv. Packaging Award (2002) for "…his introduction of new thin film polymer packaging materials"; the IEEE CPMT Sustained Technical Achievement Award (2007) for "…25 years of contributions to applications including multichip modules, wafer level packaging, integrated passives and 3DIC integration" and the Feldman Outstanding Contribution Award (2012) for "a quarter century of leadership in the CPMT Society and many key CPMT conferences".

In 2009 he initiated and served as General Chair of the IEEE 3D System Integration Conference which is rotated annually through the US, Europe and Asia.

ERIC PERFECTO (M'95, SM'01) has 33 years of experience working at IBM in the development of advanced packages for high-end systems. He last served as C4 Development Chief Technologist responsible for UBM and Pb-free solder definition for u-Pillar interconnect, and yield improvements in C4 and 3D wafer finishing. As part of the IBM Microelectronics Division divestiture, Eric is now with GLOBALFOUNDRIES. His technical interests include 3D interconnects, chip-package interaction, electromigration, multi-level Cu-Polyimide wiring structures, and design for manufacturing. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College.

An author of more than 60 technical papers and two book chapters, Eric received two Best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CPMT Trans. on Adv. Packaging. He holds over 35 US patents and has been honored with two IBM Outstanding Technical Achievement Awards: one for the development and implementation of Cu-Polyimide structures, and the other for the development and implementation of 150 um pitch Pb-Free C4 technology. He is an active member of SRC.

Eric served as the 57th ECTC General Chair, the 55th ECTC Program Chair, the ECTC Materials and Processes Subcommittee Chair ('02–'03), and is currently a member of the Advanced Packaging subcommittee. He is the current ECTC Publicity chair. For the last 6 years, Eric's popular Flip Chip Fabrication and Interconnection course has been given at ECTC to great reviews. He has achieved senior member status from IEEE, IMAPS and Society of Plastic Engineers.

From 2006 to 2013, Eric was an elected CPMT BoG member. For 3 years he served as the CPMT Strategic Director of Global Chapters and Membership where he focused on enhancing the CPMT membership value. Through his efforts, the CPMT Transactions are now part of the CPMT membership. He also highlighted the importance of technical content in the CPMT members-only page, where now webinars and presentations can be found. He is an Associate Editor for the CPMT Transactions, a CPMT Distinguish Lecturer in the area of Flip Chip, and member of the CPMT Technical Committee on Materials and Processes. For the last 2 years, Eric has chaired the CPMT Awards Committee, which is responsible for the CPMT Mayor Awards, the Regional Awards and the ECTC Student Travel Awards. At a local level, Eric is the membership Chair of the Mid-Hudson IEEE Section.

REGION 8

KARLHEINZ BOCK (M'96) since 2014 he serves as Professor and chair of electronics packaging and director of the institute of electronics packaging (IAVT) at the TU Dresden.

Since 2008 he has served as a Professor of Polytronic Microsystems at the faculty of Communication and Electronics Engineering at the University of Berlin. He earned his Diploma on electrical and communication engineering from the University of Saarbrücken, Germany in 1986 and his Dr.-Ing. (Ph.D.) for RF microelectronics from the University of Darmstadt, Darmstadt, Germany in 1994. From 1996 to 1999 he worked in the materials packaging and reliability department of IMEC vzw. in Leuven Belgium. He received the "Japan Society for Promotion of Science (JSPS) Award" in 1994 for his PhD thesis and worked as post-doc from 1994 to 1995 at the Tohoku University in Sendai, Japan. In 2012 he received the Doctor honoris causa of the Polytechnical University of Bukarest in Romania for his work on Heterosystem Integration.

He served in the Fraunhofer Gesellschaft, from 2001 until 2014 where he has been employed as head of the Polytronic and Multifunctional Systems department at the Fraunhofer Institute for Reliability and Microintegration (IZM, Munich branch, from 2010 named EMFT) and as deputy director from 2006 until 2010 of IZM and from 2010 until 2012 as acting director of EMFT. Fokus of his work is on polytronics and 3D heterointegration of systems inparticular on thin silicon; thinning, dicing and handling; reliability, characterization and condition monitoring; self-assembly of Si dies; flexible and organic electronics; MEMS; condition monitoring; medical electronics; implantable devices; biosensors.

Karlheinz Bock has contributed 250 publications and 20 patents. He co-authored 14 best paper awards. (see Google Scholar and Research Gate) He is engaged in developing the technological community of 3D systems, heterosystem integration and packaging and organic and flexible electronics. He serves on the emerging technology TPC of IEEE ECTC since 2008, as sub-committee member and vice chair 2011 and chair 2012; as member of IEEE IEDM since 2008 on TPC for display sensors MEMS (DSM) and as chair of DSM TPC in 2010; as the European arrangements co-chair 2011, chair 2012 of IEEE IEDM executive committee; on the ESTC TPC since 2012; since 2010 on the TPC of Plastic Electronics and since 2012 of FlexTech; since 2013 as session organizer for additive manufacturing and 3D printing at LOPE-C; on Board of Editors of the Micro-and Nanotechnology Journal of Bentham Science Publishers. Since 2014 he serves on the board of governors BoG of IEEE CPMT and since 2015 as the vice chair of the TC of emerging technologies of the IEEE CPMT.

REGION 10

C. ROBERT KAO (SM'11) received his Ph.D. in Materials Science from University of Wisconsin-Madison in 1994. He joined National Central University (Taiwan) in 1995 as an assistant professor. In 2005, he became the first director for the newly established Graduate Institute of Materials Science & Engineering at National Central University. In 2006 he relocated to National Taiwan University, became a University Distinguished Professor in 2008, and served as the Department Head of Materials Science and Engineering from 2010 to 2013. He currently also serves as the program manager of Materials Engineering in Ministry of Science and Technology of Taiwan. His main research interests include electronic, optical, and MEMS packaging with a main thrust on the thermodynamics and kinetics of materials interactions within packages. He helped organizing 16 international symposia on solders and soldering technology for TMS and ASM. He has served as guest editors for *Journal of Electronic Materials* and *Microelectronic Reliability,* and currently is a Principal Editor for *Journal of Materials Research* and Associate Editor for *Journal of Materials Science – Materials in Electronics.* Kao is a committee member for CPMT Materials and Processing Technical Committee, and also served as session chair for ECTC meeting.

Kao is a Fellow of the ASM and MRS-Taiwan. In 2014, he received the Brimacombe Medalist Award from TMS. He is a High Impact Research Icon of University of Malaya, Kuala Lumpur.

He has authored over 130 referred journal papers, five of which reached the status of Highly Cited Papers according to Web of Science Essential Science Indicators. He has an h-index of 33. He holds 10 US and Taiwan patents. Kao is considered the leading experts on the metallurgical reactions for electronic packaging applications, and has given more than 30 invited or keynote lectures in international conferences. He presented an invited talk at the Gordon Research Conference (Plymouth State College, July 23–28, 2000), and served as a discussion leader for the same conference in 2006. In addition to his teaching and research activities, Professor Kao was an independent board member of LOTES (2006–2010), and served as consultants for many industry leading corporations, including ASUS and VIA Technologies.

DANIEL LU (S'98, M'00, SM'04) Dr. Daniel Lu is the Vice President of Technology of Henkel Corporation (China). Prior to joining Henkel, he worked for the R&D department of Intel Corp, as a Sr. Scientist for 7 years. He also had worked for Lucent Technologies, Amoco's Electronics Materials Division, and the Electronics Materials Group of National Starch and Chemical Company before. He has extensive experience in development of electronic packaging materials such as underfills, adhesives, molding compounds, conductive adhesives, etc. His current research interests cover advanced materials for interconnects, packaging, and structural bonding for electronics, optoelectronics, and display applications, with emphasis on both high performance and low cost.

He received his MS and PhD degrees on Polymer Science and Engineering from Georgia Institute of Technology in 1996 and 2000, respectively. He received a BS in Chemistry from East China Normal University in Shanghai, China in 1990.

Dr. Lu received many awards including Henkel Lion awards in 2009 and 2014, the IEEE CPMT Outstanding Young Engineer Award in 2004, the IEEE ECTC best poster paper in 2007, Intel's most patent filing in 2003–2007, Intel Divisional Recognition Awards in 2002, 2003, and 2007, Intel most patent granting of the year for 2006 and 2007. Dr. Lu has published more than 60 technical papers, wrote chapters for five books, and holds 80 US and international patents. He is the editor of the book "Materials for Advanced Packaging (2008)" and the co-author of the book "Electronically Conductive Adhesives with Nanotechnologies (2009)". He has been serving key roles in organizing international electronic packaging conferences and teaching professional development short courses in these conferences. Dr. Lu is a Senior Member of IEEE, and an associate editor of IEEE Transactions on Components, Packaging and Manufacturing Technology and Journal of Nanomaterials, and an editorial board member of Nanoscience & Nanotechnology-Asia. Dr. Lu is a CPMT Board of Governors Member-at-Large. Dr. Lu led to establish the IEEE EDS/CPMT Shanghai Chapter where he is serving as the co-chair.

ANDREW TAY (M'91) Dr. Andrew Tay is currently a Senior Research Fellow at the Singapore University of Technology and Design. Prior to this he was a Professor in the Department of Mechanical Engineering, National University of Singapore (NUS). He obtained his B.E. (Hons I and University Medal) and PhD in Mechanical Engineering from the University of New South Wales, Australia. His research interests include thermo-mechanical failures, thermal management of electronics and EV battery systems, reliability of solar photovoltaic modules and fracture mechanics. To date he has published more than 250 technical papers, 4 book chapters, 7 keynote presentations, 11 invited presentations, 3 panel discussions, and co-edited 4 conference proceedings and two special issues of technical journals.

Dr Tay was the inaugural General Chair of the 1st and 2nd Electronics Packaging Technology Conference (EPTC) in 1997 and 1998. Since then, he has been in the organising committee of EPTC. In 2006 he was appointed the inaugural Chairman of the EPTC Board, charged with steering the development of EPTC, and is currently again serving as its Chairman. He has been in the Executive Committee of the Singapore Joint Reliability/CPMT/ED Chapter since 2000 and was its Chairman from 2010–2011. He has been involved in the international advisory boards and program committees of more than 108 electronics packaging conferences worldwide including DTIP, ECTC, EMAP, EPTC, EuroSimE, HDP, ICEPT, IEMT, IMPACT, InterPack, ITHERM and THERMINIC.

Dr Tay was an Associate Editor of the ASME Journal of Electronics Packaging, an editorial board member of several journals including *Microelectronics Journal* and *Finite Elements in Analysis and Design*, and a guest editor of a special issue on *Microelectronics Reliability*.

He has contributed significantly as a member of the IEEE CPMT Education Committee from 1998 to 2007 where he helped to evaluate projects on web-based educational modules.

From 1998 to 2005, he coordinated the implementation of the Specialized Manpower Program in Electronics Packaging and Wafer Fabrication which was funded by the Singapore Economic Development Board. He has taught many professional short courses at packaging conferences. He has been awarded competitive research grants exceeding S$14 Million for electronics packaging projects.

He has received the following major awards: 2012 IEEE CPMT Exceptional Technical Achievement Award, 2012 IEEE CPMT Regional Contributions Award, 2004 ASME Electronics & Photonics Packaging Division Engineering Mechanics Award, 2000 IEEE Third Millennium Medal, 2000 Special Presidential Recognition Award

He has been an IEEE member since 1990, an ASME member since 1993, an ASME Fellow since 2004 and a Fellow of the Institution of Engineers (Singapore) since 2004.

2017 IEEE CPMT Technical Field Award

Nomination Deadline: 31 January 2016

This, the highest IEEE CPMT Award, was established in 2002. Recipient selection is administered through the Technical Field Awards Council of the IEEE Awards Board.

Presented to: An individual or a team of not more than three

Scope: For meritorious contributions to the advancement of components, electronic packaging, or manufacturing technologies

Prize: The award consists of a bronze medal, certificate, and honorarium.

Basis for judging: In the evaluation process, the following criteria are considered: enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless, and micro-electro-mechanical systems (MEMS).

Nomination deadline: 31 January

Notification: Recipients are typically approved during the June IEEE Board of Directors meeting, usually held towards the end of the month. Recipients and their nominators will be notified following the meeting. Subsequently, the nominators of unsuccessful candidates will be notified of the status of their nomination.

Presentation: IEEE policy requires that its awards be presented at major IEEE events that are in keeping with the nature of the award and the cited achievement.

Sponsor: IEEE Components, Packaging, and Manufacturing Technology Society

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IEEE Xplore® Table of Contents Alert

Any technologist – **member or non-member** – is welcome to receive alerts when upcoming issues of our CPMT *Transactions* are posted to the IEEE's Xplore database and all the papers are available for downloading. This is a handy way to scan the issue's Table of Contents and quickly learn about novel approaches to packaging, modeling, reliability, materials, assembly and other topics.

The website link is:ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

If you already have an IEEE web account, you may sign in and select those journals you wish to track. If you don't have an account, all it takes is your name and email address! Then simply click the Alert Status box next to the journals you wish to monitor. You will receive an email each quarter when that journal is posted to Xplore.

Similarly, if you prefer to receive information by RSS feed, you may add our journals' feeds to your Reader. You'll get a listing of the papers in that issue, along with full abstracts and a link for downloading the paper. The RSS links are shown on this same web page.

Here are the journals we suggest you select for monitoring:

Transactions on Components, Packaging and Manufacturing Technology
Transactions on Semiconductor Manufacturing

Call for Nominations: 2016 CPMT Society Awards

Deadline: 9 February 2016

Do you know someone who has exceptional technical achievements? Given outstanding service to the profession? Made significant contributions to the CPMT Society?

If so, consider nominating them for a CPMT Society Award.

For additional information and to submit a nomination, go to: http://cpmt.ieee.org/awards.html

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.

Prize: $3,000 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years (2013-2015), and renewed for 2016.

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.

Prize: $3,000 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. Work in the management of CPMT Conferences or its BoG may be contributory but it is not a requirement for the award.

Eligibility: No need to be a member of IEEE and CPMT Society.

David Feldman Outstanding Contribution Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.

Prize: $2,500 and Certificate

Basis for Judging: Contributions to the organizations or enterprises connected with the field; contributions to CPMT Chapter or Board of Governors activities; contributions to the fields encompassed by the CPMT Society.

Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years (2011–2015), and renewed for 2016.

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.

Prize: $2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years (2013–2015), and renewed for 2016. There are no requirements for service to the IEEE or CPMT Society.

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.

Prize: $1,500 and Certificate

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years (2013–2015), and renewed for 2016, and must be 35 years of age, or younger, on December 31, 2015.

Congratulations to IEEE CPMT Senior Members

The members listed below were elevated to the grade of Senior Member between July and November 2015.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

- **Michael Aldrich,** Boston Section
- **Arun Chandrasekhar,** Bangalore Section
- **Tracy Hudson,** Huntsville Section
- **Natarajan Krishnaswamy,** Bangalore Section
- **ChiChuen Lo,** Hong Kong Section
- **Suresh Ramalingam,** Santa Clara Valley Section
- **Shiguo Rao,** Buenaventura Section
- **Eak Hwan Song,** Seoul Section
- **Lawrence Williams,** Orange County Section

Publication News....

Have You Read Them? The Most Downloaded CPMT Transactions Papers

What might you be missing in the CPMT literature? Following is a list of most downloaded papers in the first three quarters of 2015. CPMT members and subscribers can access these and other papers in IEEE Xplore.

"Signal-Integrity Optimization for Complicated Multiple-Input Multiple-Output Networks Based on Data Mining of S-Parameters," Mu-Shui Zhang; Hong-Zhou Tan; Jun-Fa Mao, *Components, Packaging and Manufacturing Technology, IEEE Transactions on* (Volume: 4, Issue: 7), July 2014, Page(s): 1184–1192

In this paper, an efficient signal-integrity analysis and optimization method for complicated multiple-input multiple-output (MIMO) networks is proposed, in which data mining is applied to discover the concealed information in black-box S-parameter models. Instead of performing a number of circuit simulations, data mining employs mathematical search algorithm directly into the model, which can save significant analyzed time and improve the efficiency. An optimized mining flow is presented for large scale data set, where the data processing and data mining are performed simultaneously, and thus it is unnecessary to save large extracted data. The proposed data mining method consider both the interconnect structure and the stimulated pattern of a MIMO system, which can perform thoughtful analysis and optimization with high efficiency. Two examples, signal-integrity analysis of two coupled microstrip lines and noise coupling among multiple signal vias through a power-ground plane pair, are presented to demonstrate the efficiency of the proposed data mining method in signal-integrity optimization design.

"Thermally Conductive MgO-Filled Epoxy Molding Compounds," Wereszczak, A.A.; Morrissey, T.G.; Volante, C.N.; Farris, P.J.; Groele, R.J.; Wiles, R.H.; Hsin Wang, *Components, Packaging and Manufacturing Technology, IEEE Transactions on* (Volume: 3, Issue: 12), December 2013, Page(s): 1994–2005

The use of magnesium oxide (MgO) as a filler in an epoxy molding compound (EMC) was considered to identify the maximum thermal conductivity that could be achieved without compromising rheological or processing control and processing flexibility. MgO is an attractive candidate filler for EMCs used in automotive and other applications because MgO is inexpensive, electrically insulative, has relatively high thermal conductivity, is nontoxic, and is a relatively soft filler material meaning it will be less abrasive to surfaces it contacts during its processing and shape molding. A maximum bulk thermal conductivity of 3 W/mK was achieved with a 56% volume fraction of MgO filler. This 56 vol% MgO-filled EMC has a thermal conductivity approximately twice that of traditional silica-filled EMCs with the same volume fraction of filler and has equivalent electrical insulative, thermal expansion, and water absorption characteristics. It is concluded that if a thermal conductivity greater than 3 W/mK is needed in an EMC, then a much more expensive filler material than MgO must be used.

"U-Shape Slots Structure on Substrate Integrated Waveguide for 40-GHz Bandpass Filter Using LTCC Technology," Sai-Wai Wong; Rui Sen Chen; Kai Wang; Zhi-Ning Chen; Qing-Xin Chu, *Components, Packaging and Manufacturing Technology, IEEE Transactions on* (Volume: 5, Issue: 1), January 2015, Page(s): 128–134

Millimeter-wave (mmW) bandpass filter using substrate integrated waveguide (SIW) is proposed in this paper. The propagation

constants of three different types of electromagnetic bandgap (EBG) units are discussed and compared with their passbands and stopbands performance. The slotted-SIW unit shows a very good lower stopband and upper stopband performance. The mmW bandpass filter with three cascaded uniform slotted-SIW-based EBG units is constructed and designed at 40 GHz. The extracted coupling coefficient (K) and quality factor (Q) are used to determine the filter circuit dimensions. To prove the validity, the previous proposed structure is fabricated in a single circuit layer using low-temperature co-fired ceramic technology and measured at 40 GHz, respectively. The measured results are in good agreement with simulated results in such frequency and the measured insertion losses at 40 GHz is 1.42 dB, respectively.

"High-Efficiency PCB- and Package-Level Wireless Power Transfer Interconnection Scheme Using Magnetic Field Resonance Coupling," Sukjin Kim; Jung, D.H.; Kim, J.J.; Bumhee Bae; Sunkyu Kong; Seungyoung Ahn; Jonghoon Kim; Joungho Kim, *Components, Packaging and Manufacturing Technology, IEEE Transactions on* (Volume: 5, Issue: 7), Page(s): 863–878, July 2015

As technology develops, the number of chips increases while the thickness of mobile products continuously decreases, which leads to the need for high-density packaging techniques with high numbers of power and signal lines. By applying wireless power transfer technology at the printed circuit board (PCB) and package levels, the number of power pins can be greatly reduced to produce more space for signal pins and other components in the system. For the first time, in this paper, we propose and demonstrate a high-efficiency PCB- and package-level wireless power transfer interconnection scheme. We enhance the efficiency by applying magnetic field resonance coupling using a matching capacitor. The proposed scheme can replace a high number of power interconnections with rectangular spiral coils to wirelessly transfer power from the source to the receiver at the PCB and package levels. The equivalent circuit model is suggested with analytic equations, which is then analyzed to optimize the test vehicle design. For the experimental verification of the suggested model, the Z -parameter results obtained from the model-based equation and measurement of the designed and fabricated test vehicles are compared at up to 1 GHz. The power transfer efficiency from the source coil to the receiver coil in this scheme is able to reach 85.6%. Finally, we designed and fabricated a CMOS full-bridge rectifier and mounted it on the receiver board to convert the transferred voltage from ac voltage to dc voltage. A measured dc voltage of 2.0 V is sufficient to operate the circuit, which generally consists of 1.5 V devices.

IEEE Transactions on Components, Packaging and Manufacturing Technology

Special Issue on Nanopackaging

Publication Date: Summer of 2016

The Nanopackaging technical committees of IEEE CPMT and the IEEE Nanotechnology Council are launching a special section in "IEEE Transactions on CPMT", with a comprehensive collection of the latest scientific and technical advances in the areas of nanopackaging:

- *Modeling and design with nanomaterials*
- *Materials and structures at the nanoscale*: e.g. nanoparticles, nanocomposites, nanolaminates, CNTs, nanowires, graphene and others
- *Applications*: Interconnections, thermal interfaces and heat-spreaders; underfills, encapsulants; Functional components for power, RF, energy storage:
- *Processes*: chemical, electrochemical, and physical processes with vapors, solutions and suspensions, and pastes (e.g. Printing)
- *Devices and Systems*: electronic, optoelectronic and bioelectronic

Papers focusing on technology readiness or technical challenges for commercialization are highly encouraged.

Papers are invited from

Scientists, engineers and technical leaders from, universities and industry (semiconductors, electronic systems, energy, defense and aerospace).

Instructions to Authors:

Manuscripts should be on new and significant (unpublished) advances by the authors, but can also include a comprehensive review the state-of-the-art. State-of-the-art review papers with no new research results will only be considered in special cases, (and authors should contact the editors beforehand.)

All papers for the Transactions on CPMT must be submitted for peer-review through the on-line SCHOLARONE manuscript review site at:
https://mc.manuscriptcentral.com/ieee-tcpmt

When submitting papers, authors must:
•Select "Special Section" under Manuscript Topics.
•Enter "This paper is submitted for the Special Section on Nanopackaging" in the Author's Cover Letter window.

Information and resources for authors are found at:
http://cpmt.ieee.org/transactions-on cpmt/information-and-resources-for-authors.html

The IEEE peer review standards of excellence will be applied consistently to all submissions. All accepted articles will be included in the print issue mailed to subscribers.

Topics of Interest

Nanocomposites for packaging applications (ex. Dielectrics and Substrates)
- Modeling
- Synthesis
- Characterization

Interconnections:
- Nanostructured
- Nanopaste
- Nanowire interconnections:
- CNT, graphene

Nanomaterials for Reliability
- Encapsulants; Underfills; stress-buffers

Nanostructured passive & storage components:
- Capacitors and supercapacitors:
- Nanostructured inductors
- Nanobatteries
- RF components with nanomaterials

Nanoscale materials for TIM and heat-spreaders
- CNTs, graphene
- Nanofluids

EMI shielding and filters

Manuscript Submission Deadline: 1/15/2016
Revisions and Editorial Decision: 3/15/2016
Anticipated Publication Date: Summer of 2016

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Conference News....

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Important Dates

January 31, 2016
Paper submission (2-4 pp.)

February 28, 2016
Notification of acceptance

Conference Program

May 8, 2016 (afternoon)
Tutorials & welcome reception

May 9 - May 11, 2016
Technical sessions, exhibition
Social event & gala dinner

May 11, 2016 (afternoon)
European IBIS summit

+ Info and instructions @
www.spi2016.org

Information for Authors

Over the past nineteen years, the IEEE Workshop on Signal and Power Integrity has evolved into a forum of exchange on the latest research and developments on design, characterization, modeling, simulation and testing for Signal and Power Integrity at chip, package, board and system level. The workshop brings together developers and researchers from industry and academia in order to encourage cooperation. In view of last year's success, the Committee is looking forward to the 20th Edition which will convene in Turin, Italy.

The SPI2016 technical program will include both oral and poster sessions. The conference proceedings will be published on **IEEE Xplore**. Student authors will be eligible for the **Best Student Paper Award**. Authors of best-ranked papers (based on peer review and presentation at the workshop) will be invited to submit an extended manuscript for a **special section of the IEEE Transactions on Components, Packaging and Manufacturing Technology** (subject to regular review process). A number of prominent experts will be giving keynotes, tutorials, and short courses on areas of emerging interest. An **Industry Forum** will additionally host both invited and contributed talks from the industry, with the aim of fostering the discussion and cooperation with academia and tool vendors on challenging problems that have no satisfactory solution yet. Details on submission of contributions (both as regular papers and for the Industry Forum) are available on the SPI web site. The **19th European IBIS Summit** will also be hosted at the conference venue.

As a consolidated tradition, the technical program will be complemented by **fascinating social events**, allowing the attendees to enjoy the architectural and cultural heritage as well as the vibrant atmosphere of the former capital of Italy.

Topics of Interest

- Modeling and simulation for SI/PI
- Coupled Signal and Power Integrity analysis
- Noise reduction and equalization techniques
- High-speed link design and modeling
- Power distribution networks
- RF/microwave/mixed signal packages
- 3D IC and packages (TSV/SiP/SoC)
- Nano-interconnects and nano-structures
- Electromagnetic theory and modeling
- Transmission line theory and modeling
- Macromodeling, reduced order models
- Electromagnetic compatibility
- Design methodology/flow
- Measurements
- Jitter and noise modeling
- Stochastic/sensitivity analysis
- Electro-thermal integrity
- Chip-package co-design
- Novel CAD concepts
- Optical interconnects

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GRENOBLE 2016 **6TH ELECTRONICS SYSTEM-INTEGRATION TECHNOLOGY CONFERENCE**

http://www.estc2016.eu/

September 13–15, 2016

CALL FOR PAPERS

SEMICONDUCTOR PACKAGING CONFERENCE IN EUROPE

The 6th ESTC Conference will be held September 13-15, 2016, at the World Trade Center in Grenoble, France. As the premier European event in the field of microelectronics packaging and integration, ETSC brings together both academics as well as the industry leaders to discuss and debate state-of-the-art and future trends in packaging and integration technologies. Mark your calendar today!

CALL FOR PAPERS

ESTC 2016 seeks original papers describing research and innovations in all areas of electronic packaging and system integration. You are invited to submit abstracts that provide non-commercial information of new developments and knowledge in the areas including, but not limited to the following technical tracks*: Advanced Packaging, Assembly and Manufacturing Technologies, Emerging Technologies, Flexible, Printed and Hybrid Circuits, IC and Package Design, Interconnections, Innovative Packaging and Systems, MEMS and Sensors, Materials and Processing, Optoelectronics and LEDs, Power Electronics Systems Packaging, and Reliability Test and Characterization.*

ABSTRACT SUBMISSION

Abstracts should contain 300-500 words and describe the scope, content and key points of the proposed paper. The official language of all presentations is English. Please consult the website www.estc2016.eu for more information and to upload your abstract. Abstracts are due by January 29, 2016. All abstracts must be submitted electronically at the conference web site. All submitted abstracts will be reviewed by the committee to ensure high quality. Authors will be notified of paper acceptance by March 15, 2016 and provided with instructions for paper publication. For further information, please contact: Karlheinz Bock, Program Chair by e-mail karlheinz.bock@tu-dresden.de.

IMPORTANT DATES: Abstract submission deadline: 29 January 2016. Author notification: 15 March 2016.

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The 37th International Electronics Manufacturing Technology & 18th Electronics Materials and Packaging Conference

G Hotel, Georgetown, Penang. 20th-22nd Sep, 2016

1st Call for Papers

The IEMT-EMAP 2016 will be held at Georgetown, Penang, Malaysia. It is an international event organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from CPMT society of IEEE, Santa Clara Valley Chapter. IEMT-EMAP 2016 will feature short courses, 4 parallel technical sessions, and table top exhibition. It aims to provide good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation. It is a major forum, providing opportunities to network and meet leading experts, in addition to exchange of up-to-date knowledge in the field. Since 1990's, IEMT has gained a reputation as a premier electronic materials and manufacturing technology conference and well attended by experts all over the world.

SCOPE OF PAPERS SOLICITED

Extended abstracts are being sought from, but not limited to, the following areas:

- Advanced Packaging
  - 2.5D/ 3D
  - Wafer level packaging
- Assembly & Manufacturing Technology
- Thermal/Mechanical/Electrical Design, Simulation & Characterization
- Materials & Processing
- LED, MEMS & Sensor Packaging
- Emerging Packaging & Interconnection Technologies
  - Optoelectronics packaging
  - Medical electronics packaging
  - Nano technology, materials and packaging
  - Wearable electronics
- Advanced Semiconductor Fabrication Technologies
  - Thin film materials and processing
  - Frontend process characterization
  - Yield enhancement
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- Surface Mount Technology
- Quality, Reliability & Failure Analysis

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The conference will present the "Best Paper Award" to papers in various categories:-

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Become an IEMT-EMAP 2016 Sponsor: Don't miss this great opportunity!

Important Date:

Abstract Submission:
31st March 2016
Abstract Acceptance Notification:
30th Apr, 2016
Full Paper Submission:
30th Jun, 2016

Abstract Submission

https://easychair.org/conferences/?conf=iemtemap2016

Location

G Hotel Penang

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Conference Web

IEMT-CPMT 2016
http://ewh.ieee.org/r10/malaysia/cpmt/Home/iemt/2016/iemt2016.html

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Upcoming CPMT Sponsored and Cosponsored Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the CPMT Society sponsors and supports a number of global and regional conferences, workshops and other technical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through IEEE Xplore.

For details go to: www.cpmt.ieee.org

Name: 2016 Pan Pacific Microelectronics Symposium (Pan Pacific)
Location: Kamuela, HI USA
Dates: January 25–28, 2016

Name: 2016 China Semiconductor Technology International Conference (CSTIC)
Location: Shanhai, China
Dates: March 13–14, 2016

Name: 2016 32nd Thermal Measurement, Modeling & Management Symposium (SEMI-THERM)
Location: San Jose, CA USA
Dates: March 14–17, 2016

Name: 2016 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)
Location: Montpellier, France
Dates: April 17–20, 2016

Name: 2016 IEEE 20th Workshop on Signal and Power Integrity (SPI)
Location: Turin, Italy
Dates: May 8–11, 2016
Abstract Submission Date: January 31, 2016

Name: 2016 27th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)
Location: Saratoga Springs, NY USA
Dates: May 16–19, 2016

Name: 2016 15th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)
Location: Las Vegas, NV USA
Dates: May 31–June 3, 2016

Name: 2016 IEEE 66th Electronic Components and Technology Conference (ECTC)
Location: Las Vegas, NV USA
Dates: May 31–June 3, 2016

Name: 2016 6th Electronic System-Integration Technology Conference (ESTC)
Location: Grenoble, France
Dates: September 13–16, 2016
Abstract Submission Date: January 29, 2016

Name: 2016 IEEE 37th International Electronics Manufacturing Technology (IEMT) & 18th Electronics Materials and Packaging (EMAP) Conference
Location: Georgetown, Penang, Malaysia
Dates: September 20–22, 2016
Abstract Submission Date: March 31, 2016

Name: 2016 IEEE 62nd IEEE Holm Conference on Electrical Contacts (Holm)
Location: Tampa, FL USA
Dates: October 9–12, 2016
Abstract Submission Date: February 3, 2016

Name: 2016 IEEE 25th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
Location: TBD, CA USA
Dates: October 23–26, 2016
Abstract Submission Date: July 1, 2016

Name: 2016 IEEE International 3D Systems Integration Conference (3DIC)
Location: San Francisco, CA USA
Dates: November 8–11, 2016

Name: 2016 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)
Location: HI, USA
Dates: December 14–16, 2016

The IEEE Virtual Career And Talent Expo

The IEEE Virtual Career and Talent Expo, hosted by Region 6, takes place January 20, 2016 from 10:00 AM to 2:00 PM PDT. Register today at www.IEEEexpo.org for instant access to jobs and career resources.

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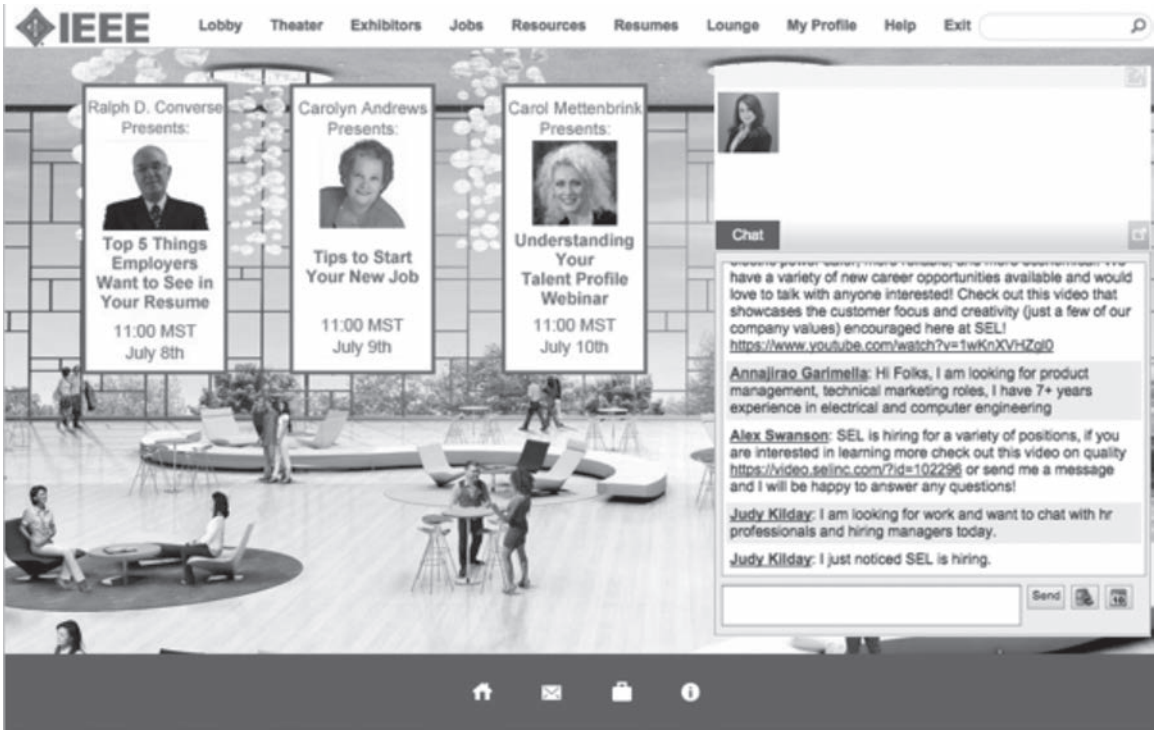

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