



Components, Packaging, and Manufacturing Technology Society Newsletter



THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

VOL. 39 NO. 1, SUMMER 2016, ISSN 1077-2999

cpmt.ieee.org

President's Column....



Jean Trehwella
GLOBALFOUNDRIES
Malta, NY, USA

jean.trehwella@GLOBALFOUNDRIES.com

It's been just over 6 months since I took this role and I'm having a blast! I've made a few changes to our CPMT officers, set my top priorities, welcomed attendees to ECTC and ICEP, participated in two IEEE Technical Activities Board (TAB) meetings, and helped Bill Chen launch the Heterogeneous Integration Roadmap Activity (see article in this Newsletter)! What is exciting is that this is just beginning. I welcome all of you to join me participating in new and different ways!

Our new officer positions are Beth Keser as VP, Education and she is taking over the Webinar series responsibilities in addition to the Distinguished Lecturers program. We have already exceeded the number of DL trips we are supporting this year and I look forward to your using this excellent resource for your chapter, student and workshop events! Pat Thompson is our new VP, Technology and he is meeting with the Technical Committee chairs to set objectives and goals including more engagement between our TCs and our conference committees. Jeff Suhling is our new Director of Membership and he is looking at growing our membership diversity in age, gender and region so that we can match our leadership in diversity of disciplines. Yasumitsu Orii who has been active in Region 10 events for many years has agreed to serve as our new Region 10 Director. Please welcome our new and returning officers by asking how you can get involved in programs of special interest to you.

My top two priorities build on the strategic groundwork Jie Xue has laid over the past 2 years.

My first is to drive a compelling vision of our Society, as the **center for discussion of all packaging topics**. Packaging is becoming a larger and larger part of the solution to technology

advancement and as such we need to serve as a bridge between all the different societies that are now embracing packaging and looking for how to take advantage of the value our expertise can drive. Collaboration with other Societies inside IEEE and technical communities outside will be key to realizing this vision. We have already started down this journey with prime examples being the Heterogeneous Integration Roadmap activity and our technical sponsorship of a Packaging Track at Semicon West. The more we collaborate with others the better understanding we will have of how packaging innovation can influence the world. Then we will use our conferences, workshops and journals to bring together that vast variety of packaging content for cross fertilization of ideas.

My next priority is to ensure we are maximizing the value we bring to our membership, to the industry and to humanity. Over the past few years we have worked to increase our value through our webinars, new chapters and chapter events, as well as career development and diversity events at our conferences. Now I will be shifting the focus onto increasing engagement. Part of this is increasing visibility of the diverse of activities we sponsor. Did

(continued on page 3)

NEWSLETTER SUBMISSION DEADLINES:

30 August 2016 for Fall issue 2016

1 November 2016 for Winter issue 2017

1 March 2017 for Spring issue 2017

1 July 2017 for Summer issue 2017

Submit all material to nsltr-input@cpmt.org

CPMT Officers

| | | |
|----------------------------|------------------------|------------------------------------|
| President: | Jean Trehwella | Jean.Trehwella@globalfoundries.com |
| VP (Technology): | Patrick Thompson | patrick.thompson@ti.com |
| VP (Conferences): | Chris Bailey | C.Bailey@gre.ac.uk |
| VP (Publications): | R. Wayne Johnson | wjohnson@tntech.edu |
| VP (Education): | Beth Keser | bkeser@qti.qualcomm.com |
| VP (Finance): | Thomas G. Reynolds III | t.reynolds@ieee.org |
| Sr. Past Pres.: | S.W. Ricky Lee | rickylee@ieee.org |
| Jr. Past Pres.: | Jie Xue | jixue@cisco.com |
| Executive Director: | Marsha Tickman | m.tickman@ieee.org |

RF & Thz Technologies:

Manos Tentzeris

Green Electronics:

Nils F. Nissen

Photonics:

Gnyaneshwar Ramakrishna

3D/TSV:

Paul Franzon

Program Directors

Membership Programs: Jeffrey Suhling, jsuhling@auburn.edu

Chapter Programs: Kitty Pearsall, kitty.pearsall@gmail.com

Awards Programs: Eric Perfecto, eric.perfecto@globalfoundries.com

Student Programs: Kwang-Lung Lin, matkllin@MAIL.NCKU.EDU.TW

Industry Programs: William T. Chen, William.Chen@ASEUS.COM

Region 8 Programs: Toni Mattila, toni.mattila@investinfinland.fi

Region 10 Programs: Yasumitsu Orii, ORII@jp.ibm.com

Elected Board Members

| | |
|-----------------------|---|
| 2016 term-end: | Regions 1–6,7,9—Li Li, Ning-Cheng Lee, James E. Morris, Jeffrey C. Suhling; Region 8—Toni Mattila, Gilles Poupon |
| 2017 term-end: | Regions 1–6,7,9—Avram Bar-Cohen, Darvin R. Edwards, Alan Huffman, CP Wong; Region 8—Mervi Paulasto-Kröckel; Region 10—Masahiro Aoyagi |
| 2018 term-end: | Regions 1–6,7,9—Philip Garrou, Eric Perfecto; Region 8—Karlheinz Bock; Region 10—C. Robert Kao, Andrew Tay; Sursesh Subramanyam |

CPMT Society Newsletter

Editor-in-Chief: Kitty Pearsall kitty.pearsall@gmail.com

CPMT Archival Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:

R. Wayne Johnson,

Co-Editor, Special Topics:

Ravi Mahajan

Co-Editor, Electrical Performance:

José E. Schutt-Ainé

Co-Editor, Components:

Characterization and Modeling:

Koneru Ramakrishna

Co-Editor, Advanced Packaging Technologies:

Kuo-Ning Chiang

Co-Editor, Electronics Manufacturing:

R. Wayne Johnson

Technical Committee Chairs

Materials & Processes:

Myung Jin Yim

High Density Substrates & Boards:

Venky Sundaram

Electrical Design, Modeling & Simulation:

Dale Becker

Thermal & Mechanical:

Dereje Agonafer

Emerging Technology:

Chris Bower

Nanotechnology:

Raj M. Pulugurtha

Energy Electronics:

Patrick McCluskey

Standing Committee Chairs

Fellows Evaluation: CP Wong, cp.wong@ieee.org

Long Range / Strategic Planning: S.W. Ricky Lee, rickylee@ieee.org

Nominations: Jie Xue, jixue@cisco.com

Distinguished Lecturers

Program Director: Beth Keser, bkeser@qti.qualcomm.com

Lecturers: Muhannad Bakir, Ph.D., Karlheinz Bock, Ph.D., Avram Bar-Cohen, Ph.D., Moises Cases, William T. Chen, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., R. Wayne Johnson, Ph.D., Beth Keser, Ph.D., John H. Lau, Ph.D., Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., Ravi Mahajan, Ph.D., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Michael Pecht, Ph.D., Eric D. Perfecto, Karl J. Puttlitz, Ph.D., Dongkai Shanguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branch Chapters

Refer to cpmt.ieee.org for CPMT Society Chapters and Student Branch Chapters list

IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US \$1.00 per member per year is included in Society fee for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved, copyright (c) 2005 by the CPMT Society of IEEE. Authors and Artists given full permission for further use of their contributions. For circulation information call IEEE Customer Service 800-701-4333, or FAX 908-981-9667.

**Circulate your printed or PDF copy of this
NEWSLETTER to co-workers.**

*IEEE prohibits discrimination, harassment, and bullying.
For more information, visit <http://www.ieee.org/web/aboutus/whatis/policies/p9-26.html>.*

you know we have a conference or workshop every month? Did you know we are involved in outreach activities like the ECTC polo shirt donations? (see photo in this Newsletter)

Thanks to your dedication and hard work we have many upcoming events including upcoming webinars on Sintered Nanoparticle-Based Interconnection, Interconnect Materials in Electronic Pack-

aging, and Understanding Voids in Flip Chip Interconnects; and conferences, including ICEPT in China (Aug 16–19), ESTC in Grenoble (Sept 13–16), IEMT in Malaysia (Sep 20–22), ICSJ in Japan (Nov 7–9) and EPTC in Singapore (Nov 30–Dec 3). I look forward to see you there and sharing in the exchange of ideas that are changing the world.

CPMT Society News....

Charting a New Course: Heterogeneous Integration Roadmap

***Submitted by the International Roadmap Committee:
Bill Chen, Chair (IEEE CPMT Society); Bill Bottoms
(IEEE CPMT Society); Tom Salmon (SEMI) and
Subramanian Iyer (IEEE EDS)***

In Fall 2015, SIA announced that it would bring the ITRS activities to a close in the Spring of 2016. The 2015 edition of ITRS 2.0, published July 8th by the SIA will be its final edition. This announcement portends a fundamental shift in our industry's approach to pursuing the spirit of Moore's law. We recognize that classical device scaling is saturating. Classical Von Neumann computing architectures, while improving, are ill-equipped to address the power performance challenges of more diverse and heterogeneous applications, such as cognitive computing and the new applications the IoT era makes possible. While no specific device or technology is expected to dominate, highly heterogeneous and diverse systems with intimate high bandwidth, low latency and low power interconnects are areas that our new roadmap must address, And this must be done in the context of a very diverse and expanding application space along with the development of design and test tools for this space. In fact, SIA, in its prescient wisdom, did mandate the heterogeneous

integration focus for ITRS 2.0, the final edition of the International Roadmap for Semiconductors.

The IEEE Components, Packaging and Manufacturing Technology Society (CPMT) has a long association with the ITRS Assembly & Packaging Technical Working Group and Heterogeneous Integration Focus team. It recognized that is crucially important to continue this Heterogeneous Integration Roadmap function for the profession, industry and the entire technical community. In this era of IoT becoming IoE, migration to the cloud, smart things everywhere and autonomous automotive, there is immense need for a pre-competitive technology roadmap providing a long term vision to the future. This Roadmap activity, identifying roadblocks, difficult challenges and potential solutions, will enable pre-competitive collaboration thereby reducing time and cost for identifying and verifying solutions to these technical challenges. As we move towards a predominance of multi-die devices from integrated circuits to integrated subsystems and system in package (SiP), it is critical that we have a roadmap that recognizes the end market inflexion points and their system level implications, and identifies the technologies at the semiconductor and system integration level to address those needs.

Bringing this mission under the auspices of CPMT and other IEEE technical societies and organizations with the same vision will fill this important gap with the deep knowledge base from the global



Heterogeneous Integration Roadmap Workshop July 11, 2016 Palo Alto, Ca.

membership and worldwide network of these organizations. It will provide a service to technical professionals and the technical community globally, consistent with the IEEE mission of service to humanity.

Taking the guarding principles from IEEE and ITRS, CPMT has developed a set of basic documents for this Roadmap incorporating purpose, mission and governance, fully consistent with transparency, quality control, volunteer action, and open access to the profession, academia and industry. (<http://cpmt.ieee.org/technology/heterogeneous-integration-roadmap.html>)

SEMI has had long association with the CPMT Society collaborating in technical seminars and workshops in advanced packaging technologies, SiP and heterogeneous integration. With its global corporate stakeholders in the electronics design and manufacturing industry and its focus at the intersection of technology and business, SEMI brings additional resources and a broader perspective to the Roadmap. When the CPMT Society formally launched the roadmap initiative in March 2016, SEMI readily joined in collaboration with CPMT.

The IEEE Electron Devices (EDS) and CPMT societies have long collaborated in exploring the synergy at the interface between device and packaging technologies. It was a natural extension for EDS to formally join in this Heterogeneous Integration Roadmap collaboration with CPMT and SEMI.

With the joint sponsorship of IEEE CPMT, SEMI and IEEE EDS, the first HIR face-to-face workshop was held at the ECTC Conference in Las Vegas on May 31st.

At this workshop presentations were made on the purpose, governance and organization of the HI Roadmap. The proposed list of technical working groups (TWGs) was reviewed and members of the TWGs were identified from the participants.

The next meeting was an all-day workshop on July 10th followed by a half-day meeting at Semicon West on July 11th. Going forward we have scheduled a series of workshops in Asia, Europe and America towards completing the 2016 HI Roadmap in the spring of 2017.

Going forward we are actively in dialogue with other IEEE societies and organizations outside IEEE with the same vision, for collaboration in bringing this roadmap of broader and diverse technologies, markets and businesses.

For additional Information:

- Heterogeneous Integration Roadmap website: <http://cpmt.ieee.org/technology/heterogeneous-integration-roadmap.html>
- “How to build System in Package” *SEMICONDUCTOR ENGINEERING* June 15th, 2016: <http://semiengineering.com/how-to-build-systems-in-package/>

Congratulations to 2016 CPMT Award Recipients

The CPMT Society annually recognizes individuals for contributions to the profession through technical achievements, service to the industry and to the Society. The following individuals received their awards at the 66th Electronic Components and Technology Conference (ECTC), June 2016.

The **Electronics Manufacturing Technology Award** is given to recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society. The 2016 recipient:



Yifan Guo, ASE, Shanghai, China

For pioneering work in development and mass production of new packaging technologies and processes, including the first BGA interconnection, as well as characterization methodologies for reliability evaluation/prediction and thermal solutions in semiconductor packaging.

The **Outstanding Sustained Technical Contribution Award** is given to recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society. The 2016 recipient:



Minhua Lu, IBM T. J. Watson Research Center, USA

For outstanding contributions to the fundamental understanding, optimization, and manufacturing implementation of Pb-free solders and contact metal layers for high performance chip interconnects.

The **Exceptional Technical Achievement Award** is given to recognize an individual, or group of individuals for exceptional technical achievement in the fields encompassed by the CPMT Society. The 2016 recipient:



Xiaobing Luo, Huazhong University of Science and Technology, China

For exceptional contribution in modeling and experimental characterization of IC/LED packaging, focusing primarily on thermal packaging and innovations in packaging processes.

The **David Feldman Outstanding Contribution Award** is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions. The 2016 recipient:



Jie Xue, Cisco Systems, Inc., USA

For outstanding leadership of the CPMT Society as Vice President and President, with key impact on globalization, industry connections, technical committee revitalization, as well as initiating transformation to prepare the Society for rapid, disruptive changes in the semiconductor and electronics industries.

The **Regional Contribution Awards** are given to recognize significant and outstanding leadership and contributions to the growth and impact of CPMT programs and activities at the Region level. One award may be given annually for each Region/Groups of Regions: Regions 1–7 & 9; Region 8; and Region 10. The 2016 recipients:



REGION 8 (Europe, Africa, Middle East):
Zsolt Illyefalvi-Vitéz, Budapest University of Technology and Economics, Hungary

For outstanding contributions in promoting electronic packaging and IEEE CPMT networking activities in East Europe and Region 8, including founding the ISSE - International Spring Seminar on Electronics Technology and establishing and developing the IEEE CPMT Hungary-Romania Joint Chapter.



REGION 10 (Asia & Pacific):
Yasuhiro Ando, FUJIKURA Ltd., Japan

For contributions to the reconstruction and activation of the CPMT Japan Chapter as Vice Chair and Chair, and leadership in electronics and photonics packaging technologies development in Japan.

Congratulations to IEEE Fellows Class of 2016

Listed below are new IEEE Fellows who are members of the CPMT Society. See a list of all CPMT members who are IEEE Fellows at: <http://cpmt.ieee.org/ieee-fellows-program.html>.

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Henning Braunisch

Intel Corporation, USA

For contributions to high-bandwidth microprocessor packaging.

Patrick Fay

University of Notre Dame, USA

For contributions to compound semiconductor tunneling and high-speed device technologies.

Tzyy-Sheng Horng

Nat'l Sun Yat-Sen University, Taiwan

For contributions to system-in-package modeling and design.

Qing-An Huang

Southeast University, China

For contributions to modeling and packaging of microsensors and microactuators.

Dan Jiao

Purdue University, USA

For contributions to computational electromagnetics.

Joungho Kim

KAIST- Korea Advanced Inst. of Science & Technology, Korea

For contributions to modeling signal and power integrity in 3D integrated circuits.

Congratulations to IEEE CPMT Senior Members

The members listed below were elevated to the grade of Senior Member between February and June 2016.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

Seungyoung Ahn,
Daejeon Section

Adrijan Baric,
Croatia Section

Kuan Yew Cheong,
Malaysia Section

Eunyong Chung,
Seoul Section

Ki Jin Han,
Changwon Section

Azmat Malik,
Santa Clara Valley Section

Min Miao,
Beijing Section

Yasumitsu Orii
Tokyo Section

Sung Joo Park,
Atlanta Section

Kishio Yokouchi,
Tokyo Section

Chansei Yoo,
Seoul Section

Brian Zahnstecher,
Santa Clara Valley Section

E-Mail Alias and IEEE Web Account Needed 2016 CPMT Society Board of Governors Election On-Line

In order to vote in this year's CPMT Board of Governors election, members will need to have a valid e-mail alias on record with IEEE and also have an IEEE Web Account.

Eligible voting members will receive notification by e-mail soon with instructions for voting on-line. You will need an IEEE Web Account to access the ballot and cast your vote. This Web Account is the same one you may use for IEEE services such as renewing membership and accessing IEEE Xplore.

If you do not recall your Web Account username and password, or aren't sure whether you have established an account, please go

to <http://www.ieee.org/web/accounts> to recover your password or establish a new account.

Please be sure to update your IEEE membership record with your current e-mail alias. If you DO NOT HAVE AN E-MAIL address or would prefer to receive a paper ballot by mail, please send your name, mailing address and IEEE Member Number by 1 October to:

Marsha Tickman
IEEE CPMT Executive Office
445 Hoes Lane
Piscataway, NJ 08854 USA
m.tickman@ieee.org



CPMT Chapter News....

CPMT Malaysia Chapter Report: 2015 Activity Highlights *University Final Year Project Initiative and Engagement by CPMT Malaysia*

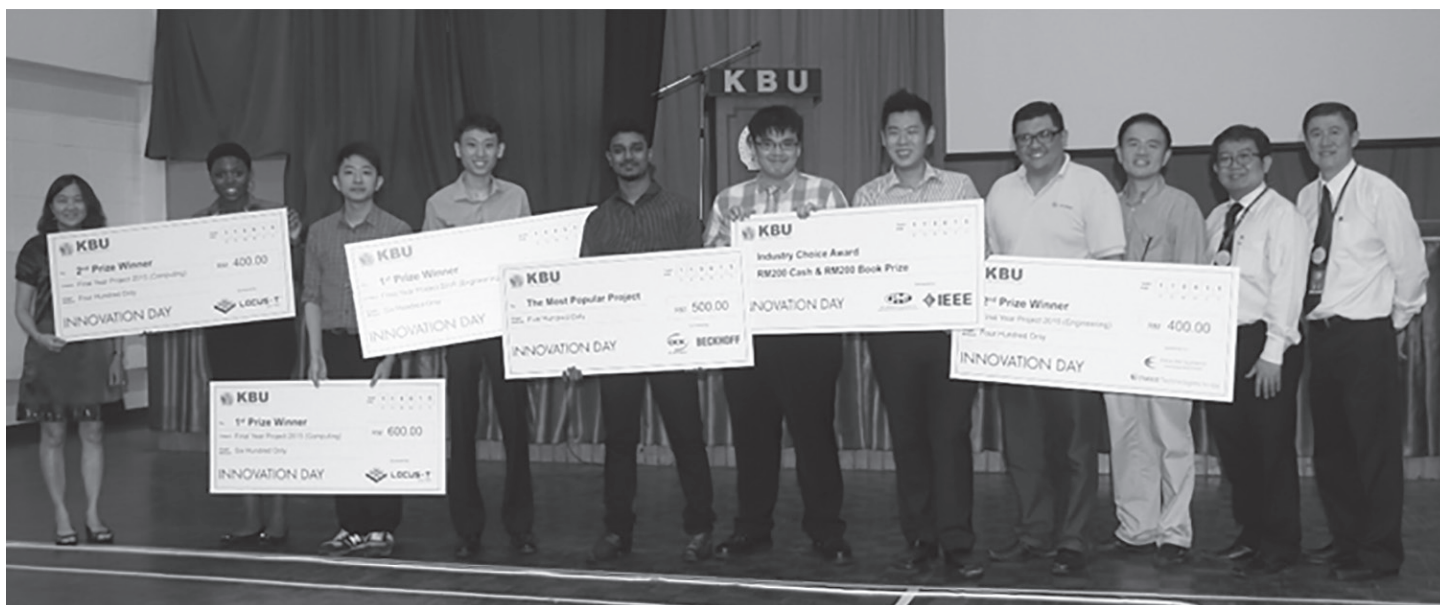
CPMT Malaysia Chapter delivered best Industry Choice Award at KBU International College 2015 Innovation Day

It is evident that KBU has done a great job in educating innovative leaders of tomorrow together with the partnership by IEEE/CPMT Malaysia chapter. The School also encouraged students by presenting RM3500 worth of cash and book prizes for students who excelled under the categories of the best Industry Choice Award sponsored by the Institute of Electrical & Electronics Engineers (IEEE) Component, Packaging & Manufacturing Technology

Society (CPMT) and the best Engineering & Computing final-year projects sponsored by the College. The projects were chosen based on 60 percent of professional assessment and 40 percent of voting process. The first award was given out by Mr Lim Wee Teck, IEEE CPMT representative and the latter two awards were given out by Dr. Chee Choong Kooi, the Principal of KBU. Prof Rao Tummala of Georgia Tech also sponsored a book entitled "Fundamentals of Microsystems Packaging" for the first award winner to be donated to KBU Library in her name.

Ping Ting wins the Inaugural IEEE Final Year Project (Curtin University Sarawak)

IEEE CPMT Malaysia organized the inaugural IEEE Final Year Project for Malaysian Universities. Competition was open to



Student Desmond Siah Zhao Qiang (centre) posing with his IEEE CPMT M'sia award, flanked by (from right) Mr. Lye, Dr. Chee and Mr. Lim (CPMT representative).



Organizing committee and speakers, along with participants at the event in Penang on Sept 7.



Organizing committee and speakers, along with participants at the event in Putrajaya on Sept 8.

full time and part-time student studying in areas broadly related to electrical/electronics, physics (incl. materials science), info-communication and related areas (hardware and software). Curtin University Sarawak was the first university to partici-

pate in this program. Their inaugural winner was Chong Ping Ting, an electronic and communication engineering graduate of Curtin University, Sarawak Malaysia (Curtin Sarawak). Chong's project entitled 'Low Power Reversible Logic Circuit

Design for IEEE 802.11 application' involved designing a reversible logic circuit for real world application. Reversible logic circuits have advantages in information-lossless and thus dissipate little heat compared to conventional logic circuits. Her down-to-earth application-oriented research earned the IEEE CPMT judges' nod to be the 2015 winner for Curtin Sarawak. This event was featured in our national newspaper i.e. the Star Online, the Borneo Post Online and Utusan Malaysia Online. Similar to the KBU event, Prof Rao Tummala of Georgia Tech also sponsored the same book edited by himself i.e. "Fundamentals of Microsystems Packaging" for Ms Chong to be donated to Curtin Sarawak Library in her name. Further information is available here: http://www.curtin.edu.my/campusnews/mediarelease/2015/PR_15-100.htm

Workshop on Semiconductor Advanced Packaging: September 7–8, 2015

The IEEE-CPMT Malaysian chapter organized a 1 day workshop on Semiconductor Advanced Packaging on the 7th and 8th of September at G Hotel, Penang and Shangri-La, Putrajaya, respectively. The event managed to gather close to 200 industry experts, peers and academicians from across Malaysia. The main speakers were Ms. E. Jan Vardman, President of TechSearch International, Inc based in Austin, Texas, USA and Mr Hamid Syed, the Director of Supply Chain for Cisco in Hong Kong. Ms Jan Vardman's presentation was titled "Latest trends in Advanced Packaging: Driving package volumes with mobile and wearable products", whilst Mr Hamid spoke on "Internet of everything—Latest trend, challenges, applications and case studies".

Inauguration of CPMT Beijing Chapter

A workshop held at Unisplendour International Center nearby Tsinghua University on Dec 12, 2015, with 90+ registered attendees, signified the inauguration of IEEE Components, Packaging and Manufacturing Technology (CPMT) Society, Beijing Chapter. The workshop was hosted and chaired by Prof. Jian Cai.

The workshop began with an invited lecture by Prof. Ricky LEE, Hong Kong University of Science & Technology, also an IEEE CPMT Distinguished Lecturer and the Junior Past-President of IEEE CPMT, titled "eSilk Roads: Conventional Evolution and Contemporary Migration of Electronic Packaging Technologies between the East and the West". This talk reviewed the conventional evolution and contemporary migration of electronic packaging technologies between the East and the West, and several unique observations in the past and perspectives for future development

is offered by the presenter, along with keen insights into current situations.

Next, a short inaugural ceremony was held. Prof. Ricky LEE spoke on behalf of IEEE CPMT, give an introduction of the society. Prof. Keyun Bi, the President of Electronic Manufacturing and Packaging Society, Chinese Institute of Electronics, gave a speech on the brief history of Chinese electronic packaging industry and expressed his congratulation. Prof. Jinjun Feng, the President of IEEE, Beijing Section, spoke on behalf of the local section.

Then three talks were given by professionals from renowned universities and leading companies in China, listed as follows: 1) "Technical Challenges in Via Last 3D WLCSP", by Dr. Daquan YU, from Tianshui Huatian Technology Co., LTD; 2) "Novel Low-temperature Nano-scale Interconnects", by Dr. Qian WANG, from Tsinghua University; 3) "Interfacial Sliding in TSV and its Influences on the Stress of TSV Structure", by Dr. Fei SU, from Beihang University.



Publication News....

2015 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 200 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

The awards were presented at the 66th Electronic Components and Technology Conference (ECTC), June 2016.

Subscribers to this publication can access the papers on-line in IEEE Xplore at:

URL: <http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870>

Advanced Packaging Technologies Category

Integrating and Interfacing Flexible Electronics in Hybrid Large-Area Systems

Warren S. A. Rieutort-Louis, Student Member, IEEE, Josue Sanz-Robinson, Tiffany Moy, Student Member, IEEE, Liechao Huang, Student Member, IEEE, Yingzhe Hu, Student Member, IEEE, Yasmin Afsar, James C. Sturm, Fellow, IEEE, Naveen Verma, Member, IEEE, and Sigurd Wagner, Fellow, IEEE, Vol. 5, No. 9, September 2015

Abstract: An approach to creating large-area systems is described that combines flexible thin-film electronic sensor surfaces with complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs). Complete systems are built by lamination of multiple layers, consisting of thin-film subsystems and CMOS ICs on a passive flexible substrate. A flexible passive backplane provides in-plane interconnections. Via-type interconnections between stacked layers are made by inductive or capacitive coupling. Steps and testing techniques, from devices and circuits to fully integrated hybrid systems, are illustrated.

URL: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7163342&filter%3DAND%28p_IS_Number%3A7272756%29

and

Thermal Remote Phosphor Coating for Phosphor-Converted White-Light-Emitting Diodes

Xingjian Yu, Bin Xie, Qi Chen, Yupu Ma, Ruikang Wu, and Xiaobing Luo, Vol. 5, No. 9, September 2015

Abstract: We demonstrated a thermal remote phosphor coating method for realizing high angular color uniformity (ACU) and high efficiency of phosphor-converted white-light-emitting diodes based on thermal control. The proposed phosphor-coating method can fabricate remote phosphor layer geometries through a simple package process. Experimental results show that compared with those samples packaged by conventional dispensing coating, this method can efficiently improve the ACU. Angular color-correlated temperature (CCT) deviation of the test samples by the present method can reduce from 1100 to 90 K for an average CCT of 4300 K from -90° to $+90^\circ$ view angles, and the CCT distributions are 150 and 250 K for average CCTs of 5300 and 6300 K, respectively. In addition,

this method can improve the lumen efficiency by 4.45% for an average CCT of about 4300 K, and increased by 4.96% and 5.45% for average CCTs of 5300 and 6300 K, respectively.

URL: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7174531&filter%3DAND%28p_IS_Number%3A7272756%29

Components: Characterization and Modeling Category

Cox-Proportional Hazards Modeling in Reliability Analysis—A Study of Electromagnetic Relays Data

Lingling Li, Dongjuan Ma, and Zhigang Li, Vol. 5, No. 11, November 2015

Abstract: Ambient temperature is an important factor influencing the reliability of electromagnetic relays. The effect of different environmental temperatures on relay lifetime can be examined through the Cox-proportional hazards model (PHM). In this paper, relay life tests were carried out at -20°C , 20°C , and 55°C . Relay lifetime data were collected at various temperature conditions and were integrated to establish a Weibull PHM of electromagnetic relays. A comparative analysis of the experimental data indicates that an ambient temperature has a significant influence on contact resistance. The characteristic life, the mean life, and the probability density function of failure under temperature conditions not tested in the conducted experiment were estimated through the implementation of Cox PHM. Both the characteristic life and mean life decrease significantly with increasing ambient temperature. The perspectives and the methodology of the implementation of the Weibull PHM presented in this paper are generic and could be adopted for other systems/products directly.

URL: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7298432&filter%3DAND%28p_IS_Number%3A7327287%29

and

Evolution of Voltage Transients During the Switching of a MEMS Relay With Au/MWCNT Contacts

Adam P. Lewis, John W. McBride, and Liudi Jiang, Vol. 5, No. 12, December 2015

Abstract: Gold is commonly used for microelectromechanical electrical contacts due to its desirable electrical and mechanical properties; however, the lifetime of gold contacts is limited, particularly in the case of hot switching. To improve the lifetime of electrical contacts, we have developed a gold-coated multiwalled carbon nanotube bilayer composite. Experiments with these composites have shown that the switching dynamics vary over the lifetime of the switch. The change in potential across the switch contacts during the contact-break process, referred to as the transient opening voltage, has been monitored at a number of intervals throughout the switch life. The transient opening voltage shows behavior indicative of the molten metal bridge (MMB) phenomenon. While stable for most of the contact lifetime, the duration of this behavior increases sharply as the contacts approach failure. Throughout the switch lifetime, the contacts are required to survive a large number of opening and closing cycles

and, therefore, it is important to understand the switching dynamics. A contact pair was investigated to failure where the experimental conditions were: load current and voltage of 50 mA and 4 V, respectively. Failure occurred after 28 million hot-switched cycles. The average energy of the MMB process was evaluated as 1.54 μJ per opening event during the stable region, this rose to 13.2 μJ shortly before failure. An experiment run under similar conditions but with a lower load current of 10 mA, which was switched for over 500 million cycles, showed a stable contact resistance and an average MMB energy of 5 Ω and 57 nJ, respectively.

URL: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7310863&filter%3DAND%28p_IS_Number%3A7348621%29

Electrical Performance of Integrated Systems Category

Modeling of Through-Silicon Via (TSV) Interposer Considering Depletion Capacitance and Substrate Layer Thickness Effects

Ki Jin Han, Member, IEEE, Madhavan Swaminathan, Fellow, IEEE, and Jongwoo Jeong, Vol. 5, No. 1, January 2015

Abstract: To support the recent progress in 3-D integration based on through-silicon via (TSV) technology, an improved electromagnetic modeling method for TSVs is presented. In the framework of the mixed-potential integral equations combined with cylindrical modal basis functions, the proposed method can extract the effects of depletion capacitances and a finite substrate. To include the effects of depletion region generated by an external dc bias voltage, an additional capacitive cell is employed around a TSV. The proposed method also considers the effect from the finite silicon substrate accurately by employing the multilayered Green's functions. To reduce the computational cost for calculations involving Green's functions, a method to approximate Green's functions over localized intervals when computing partial potential coefficients is presented. The proposed method is validated for simple TSV examples and shows an improved accuracy with the acceptable usage of memory and simulation time. In addition, a 10×10 TSV array is modeled using different design parameters, showing the capability for dealing with larger size problems using this method.

URL: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=6975150&filter%3DAND%28p_IS_Number%3A7008581%29

Electronics Manufacturing Category

Model for Inverse Determination of Process and Material Parameters for Control of Package-on-Package Warpage

Pradeep Lall, Fellow, IEEE, Kewal Patel, and Vikalp Narayan, Vol. 5, No. 9, September 2015

Abstract: Package-on-package (PoP) assemblies may experience warpage during package fabrication and later during surface mount assembly. Excessive warpage may result in loss of coplanarity, open connections, misshaped joints, and reduction in package board-level reliability under environmental stresses of thermal cycling, shock, and vibration. Previous researchers have shown that warpage may be influenced by a number of design and process factors including underfill properties, mold properties, package geometry, package architecture, board configuration, underfill and mold dispense and cure parameters, and package location in the molding panel. A comprehensive inverse model incorporating a full set of design and process parameters and their effect on PoP and PoP assembly warpage is presently beyond the state of the art. In this paper, data have been gathered on multiple PoP assemblies under a variety of assembly parameters. The packages have been speckle coated. The warpage of the PoP assemblies have been measured using a glass-top reflow oven using multiple cameras. Warpage measurements have been taken at various temperatures of the reflow profile between room temperature and the peak reflow temperature. Finite-element models have been created, and the PoP warpage predictions have been correlated with the experimental data. The experimental data set has been augmented with the simulation data to evaluate configurations and parameter variations, which were not available in the experimental data set. Statistical models have been developed to capture the effect of single and multiple parameter variations using principal component regression and ridge regression. The best subset variables obtained from stepwise methods have been used for model development. The developed models have been validated with the experimental data using a single factor design of the experimental study and are found to accurately capture material and geometry effects on part warpage. The results show that the proposed approach has the potential of predicting both single and coupled factor effects on warpage.

URL: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7194791&filter%3DAND%28p_IS_Number%3A7272756%29

Conference News....

Over 1,400 in Attendance at the 66th ECTC in Las Vegas

Submitted by Chris Bower, Assistant Program Chair, IEEE ECTC 2017

This year's IEEE Electronic Components and Technology Conference (ECTC) was held at the Cosmopolitan of Las Vegas from May 31 to June 3, 2016. Even in the midst of industry consolidation and corporate travel restrictions, the conference exceeded 1,400 attendees for only the second time in its 66 year history, with a total of 1,436 industry professionals in

attendance. The conference included a record number of 392 technical contributions, which were organized into 36 oral sessions and 5 interactive presentation (IP) sessions. For the third straight year the conference had over 100 exhibitors at the Technology Corner Exhibit, a tribute to the quality of the conference and its attendees. The 66th ECTC benefited from a record number of sponsors and sponsorship, further testament to the value delivered by this flagship conference. This year, ECTC was co-located at the Cosmopolitan with the biannually-held iTherm conference, and many attendees took advantage of this opportunity to attend both of these IEEE CPMT events.



The attendance at the 66th ECTC exceeded 1,400 for the second time.



Luu Nguyen instructing PDC attendees interested in wafer-level packaging.

Preparations for the 66th ECTC started last October, when the professional volunteers serving in the technical committees reviewed a record number of 649 submitted abstracts. Ultimately, 60% of the submissions were accepted, leading to 392 presentations at the conference. This year, 46% of the submitted abstracts were from corporations, 41% were from academia, and 13% were from research institutions. In a testimony to the diversity of the industry and the conference, abstracts were received from 26 different countries.

The conference program, consisting of 36 oral sessions and 5 interactive presentation sessions, came together at the Technical Program Committee's annual planning meeting near Dallas, Texas, on November 5 and 6, 2015. This year the 3D/TSV work group, under the leadership of Karlheinz Bock of TU Dresden, Germany, identified and helped to coordinate 9 oral sessions. The subcommittee chairs and session chairs did a great job developing interesting sessions and communicating with their session authors, which enabled all the manuscripts to be publication-ready well before the start of the conference. Also, this was the first year that ECTC utilized the IEEE Computer Society's Conference Publishing Services (CPS) to receive and process manuscripts. As in previous years, we used the IEEE CrossCheck system to ensure that all of the ECTC manuscripts maintain a high level of original content.

As usual, the first day of the conference, the Tuesday following Memorial Day, included professional development courses (PDCs), special sessions, and workshops. This year, the conference had eight morning PDCs, running from 8am to noon, and another eight afternoon PDCs, running from 1:30pm to 5:30pm. The total number of PDC attendees was 386, which was the second highest ever. The courses continue to serve a convenient way for students and engineers to quickly get "up to speed" on many important subjects, such as wafer-level and fan-out packaging, 3D integration, and various aspects of reliability.

Once again this year, there were three special sessions on Tuesday. At 10am, Nanju Na from Xilinx, chaired a panel session titled "Memory Technology Advances and Prospects for Packaging". During this panel, the numerous attendees were treated to candid and insightful thoughts from experts in the field, which included Bryan Black from AMD, Sandeep Bharathi from Xilinx, Nick Kim from SK Hynix, Craig Hampel from Rambus, and Ravi Mahajan from Intel. At 2pm, Kannan Raj from Oracle and Fuad Doany from IBM chaired a special panel session developed by the Optoelectronics technical subcommittee titled "Emerging Optical Interconnect Packaging for the Cloud". The distinguished panelists included Frank Flens from Finisar, Peter De Dobbeleare from Luxtera, Wilfried Haensch from

IBM, Ashok Krishnamoorthy from Oracle, and Erin Byrne from TE Connectivity. On Tuesday evening at 7:30pm, Yoshikazu Takahashi from Fuji Electric and Patrick McCluskey from the University of Maryland chaired a panel on "Power Module Integration". This evening panel included contributions from technology leaders from around the globe, including: Klaus-Dieter Lang from Fraunhofer, Bernd Roemer from Infineon, Hiroshi Hozoji from Hitachi, Yoshiyuki Nagatomo from Mitsubishi, Jared Hornberger from Wolfspeed, and Avi Bar-Cohen from the University of Maryland.

Tuesday at ECTC was also the occasion of the first IEEE CPMT Heterogeneous Integration Technology Roadmap Workshop. This day-long workshop was chaired by William Chen and W. R. Bottoms. This activity is organized under the auspices of the IEEE CPMT Society, and follows the purpose, process, and format of the ITRS Heterogeneous Integration Roadmap which ended in the spring of 2016. This important workshop, which will be held annually at future ECTC conferences, will be critical to developing a 15-year roadmap for navigating technology challenges, such as the slowing of Moore's law, and market challenges, like the emergence of the Cloud and the Internet of Things (IoT).

The ECTC Student Reception was held on Tuesday evening and sponsored by Texas Instruments. A steady stream of student attendees took advantage of the opportunity to mingle and network with professionals in the field. Right after this, a General Chair's Reception was given for Speakers and Session Chairs, at the Cosmopolitan's 4th floor pool, which provided great food, drink, weather, and views of the Las Vegas Strip. These receptions provided a great start to the conference and helped prepare everyone for the following three days filled with technical presentations and networking opportunities.

Each day at ECTC begins with the Speakers Breakfast in which the presenters and session chairs meet and take care of the preparatory work for their respective sessions. The PDC Chair, Kitty Pearsall, provided instructions to the PDC instructors and proctors on Tuesday morning, and Sam Karikalan, the 66th ECTC Program Chair, hosted these breakfast meetings for the benefit of the session chairs and speakers on the other three days of the conference.

Wednesday marks the start of the technical sessions with six sessions running in parallel, both in the morning and in the afternoon each day. Wednesday morning started with large crowds in numerous sessions, the "Advances in Fan-Out Packaging" session in the Nolita 1 ballroom was standing room only. Other notable morning session topics included "Thermal Compression Bonding Processes", "Next Generation Substrates" and two 3D/TSV sessions. High session attendance was noted throughout the day, with



Panelists discuss recent advances in memory technology and the impact for the packaging industry.



66th ECTC Program Chair, Sam Karikalan (in the background), delivering instructions at the daily Speakers Breakfast.



The Tuesday afternoon panel on optical packaging for the Cloud draws a crowd.



The General Chair's Speakers Reception was poolside with views of Las Vegas in the background.

afternoon topics covering “3D Process & Integration Technologies”, “Innovations in TSV”, and “Optical Interconnects”.

The keynote speech at the ECTC luncheon on Wednesday was given by Jordan P. Evans, Manager of the Mechanical Systems Division at the Jet Propulsion Laboratory (JPL). In his inspirational presentation, titled “Dare Mighty Things: Landing a Car on Mars”, Mr. Evans provided his first hand perspective of how the team at JPL was able to pursue “crazy” ideas without fear of failure, and how this culture allowed them to successfully land the “Curiosity” rover on the surface of Mars. The lunch ballroom was packed during this presentation and the general feedback was that this keynote left many people feeling inspired and motivated to generate a similarly innovative culture within their respective groups.

Awards for best and outstanding papers from the 65th ECTC 2015, both in oral presentation sessions and interactive sessions, were presented by the 66th ECTC Vice General Chair, Henning Braunisch, at this luncheon. Also presented was the Intel Best Student Paper Award for ECTC 2015. A list of the award recipients can be found on the ECTC webpage (www.ectc.net).

In addition, David McCann, the ECTC Sponsorship Chair, was honored for his tremendous support of the conference. David has provided service to the conference for many years, and has served as the Sponsorship Chair since 2011. The sponsorship of the conference has increased in each year under his leadership. At this conference, Wolfgang Sauter, was announced as the new ECTC Sponsorship Chair.

The Technology Corner Exhibit area saw a steady stream of attendees, with very busy bursts of activity during the breaks from the technical sessions. The exhibitors hosted a reception on Wednesday evening that provided more opportunities for technical and business exchanges with perspective customers and collaborators. The interactive presentation (IP) sessions were conveniently located just outside the Technology Corner and had a high number of patrons studying the presented results.

For the second year in a row, Beth Keser from Qualcomm, chaired the CPMT Women's Panel, with this year's session titled “Maximize Your Career Potential”. Attendees heard career perspectives from distinguished entrepreneurs and business leaders including: Marayam Rofougaran, Jan Vardaman from TechSearch, and Rebecca Jimenez from Amkor. The panelists participated in a Q&A session with the audience, and then the panelists and audience participated in an in-room reception where the questions and networking continued.

The Wednesday evening Plenary Session titled “Life after Moore's Law” was chaired by Rozalia Beica from Dow Electronic Materials and included presentations from leading technology institutes. The speakers included: Luc Van den hove from IMEC, Marie-Noelle Semeria from CEA-LETI, Dim Lee Kwong from IME-Singapore, Subramanian Iyer from UCLA, and C. P. Wong presenting on behalf of NCAP China. The panelists shared many insights with the over 225 attendees present, with some panelists stressing the importance of investment in ever smaller nodes to make sure Moore's law continues and others suggesting



66th ECTC General Chair, Alan Huffman, presenting an award to the keynote speaker, Jordan P. Evans.



ECTC thanks Dave McCann for his tremendous leadership and support.



The 66th ECTC had 104 exhibitor booths at the Technology Corner.



Over 225 attended the Wednesday evening Plenary Session "Life after Moore's Law".

it is time to invest in entirely new strategies for increasing device functionality.

The Thursday morning sessions were well attended and covered topics ranging from "Advanced Assembly" to "Wirebond Process & Reliability" to "Advanced Flip Chip Packaging". Thursday afternoon included sessions on "MEMS and Sensors", "High-Speed Systems", and "Interconnect Reliability".

The IEEE CPMT Society President, Jean Trehwella, presided over the luncheon on Thursday and presented the CPMT Society Awards. The 2016 IEEE CPMT Field Award, the highest award recognizing technical achievement in the field of device packaging, was presented to Michael Pecht of the University of Maryland. Prof. Pecht leads the Center for Advanced Life Cycle Engineering and was recognized for his technical leadership in the fields of physics of failure and electronic reliability.

The ECTC 2016 Technical Program Committee meeting was held on Thursday evening. Mark Poliks, who will serve as the Program Chair for ECTC 2017, chaired this meeting and presented the statistics of the 66th ECTC and also the timeline for the run up to the 67th ECTC that will be held in Orlando, Florida, next year. The CPMT Representative on the ECTC Executive Committee, C. P. Wong, introduced Chris Bower of X-Celeprint as the Assistant Program Chair of the 67th ECTC. This meeting also enabled

the ECTC technical program subcommittees to get in touch with potential new members of their committees.

The Gala Reception on Thursday evening was the highlight of the week for the conference attendees, exhibitors, sponsors, and their guests. It was a time to celebrate the success of the 66th ECTC by socializing and enjoying the excellent food and beverages that were supported by the Gala Reception Gold and Silver sponsors.

Following the Gala Reception, the 2016 CPMT Seminar on "Systems, Devices, and Packaging Technologies for the IoT and Hyper-Connected Society" was chaired by Venkatesh Sundaram of Georgia Tech and Yasumitsu Orii of IBM. At this seminar, Mudasar Ahmad of Cisco Systems, Kohji Hosokawa of IBM, Christian Hoffmann of TDK-Epcos, and Eita Horike of Sekisui each presented their vision of the importance of packaging technology and how packaging technology is being applied to the unique challenges associated with IoT and hyper-connectivity.

For those interested in the latest advances in the packaging field, Friday was not to be missed. The morning sessions ranged from "Wafer-Level CSP & Heterogeneous Integration" to "Innovative Interconnects" to "RF, Microwave & Millimeter Wave". The afternoon included sessions on "3D Application", "Novel Fan-Out Interconnects", and "Wearable Electronics". At lunch on Friday, everyone had the usual fun at the famous ECTC raffle, where Tom



Prof. Michael Pecht receives the 2016 IEEE CPMT Field Award.



The Gala Reception was the time for socializing after a day full of technical meetings and brainstorming.



The 66th ECTC Executive Committee Leadership Team: Sam Karikalan, Program Chair; Henning Braunisch, Vice General Chair; Alan Huffman, General Chair; and Mark Poliks, Assistant Program Chair.

Reynolds, the ECTC Treasurer, kept everyone laughing and longing to hear the numbers on their ticket called.

Overall, the 66th ECTC was a great success in terms of its near record attendance, strong exhibitor presence, record sponsorship and a record number of technical presentations and submitted abstracts. The ECTC Executive Committee sincerely thanks all the attendees, exhibitors, and conference sponsors for their support. The 67th ECTC will be

held at The Walt Disney World Swan & Dolphin Resort, Lake Buena Vista, Florida, USA, May 31–June 3, 2017. Henning Braunisch from Intel will be the General Chair of this conference. The Call for Papers and PDC Proposals will be available at www.ectc.net and the abstract submission will close on October 10, 2016. So, get those abstracts ready and submit them as soon as abstract submission opens online.

See you all in Florida in 2017!

ECTC Donates to a Worthy Cause



Dr. Tom Brian, Director of Send Hope (<http://www.send-hope.org/>), models one of the ECTC polo shirts donated for the people of the Mosquito Coast in Honduras.

IEEE Electrical Design of Advanced Packaging & Systems (EDAPS) Symposium

Hawaii - 14-16 December 2016



Call for Papers



The IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium is the premier international conference in Asia-Pacific region to share the recent progress of design, modeling, simulation and measurement related to the electrical issues arising at the chip, package and system levels. Covering the paper presentations, industry exhibitions, workshops and tutorials, the EDAPS 2016 will be held at the **Sheraton, Waikiki, in Honolulu, Hawaii, USA from December 14 to 16, 2016**. The technical program of the symposium not only addresses the current technical issues but also brings out the topics on IC design, SiP/SoP packaging, EMI/EMC, EDA tools and most importantly the challenge issues in advanced 3D-IC and TSV design. For further information, please send your inquiry to admin@edaps2016.org

IMPORTANT DATES

Conference Dates: **December 14-16, 2016**

Paper Submission Deadline: **August 15, 2016**

Acceptance Notification: **September 1, 2016**

Location: Sheraton Waikiki,

2255 Kalakaua Avenue,
Honolulu Hawaii 96815

Conference Co-chairs:

José Schutt-Ainé, University of Illinois

Madhavan Swaminathan, Georgia Tech

Conference web site: www.edaps2016.org

For more information/contact: admin@edaps2016.org

TOPICS

- 3D-Ics / TSVs / Interposers
- Testing on 3D-IC and SiP
- Signal and Thermal Integrity
- Power Integrity / Power Distribution Networks (PDNs) / Ground Noise
- Multi-physics Simulation Techniques for SI / PI / TI Analysis
- Design and Modeling for High-speed Channels and Interconnects
- Electronic Packages, SiP / SoP
- IC and Package Level EMC
- RF/mm-wave Packages
- Embedded Passives
- Power Electronic Packages
- Time / Frequency Domain Measurement Techniques
- Advanced Simulation Tools and CAD
- Substrate Technology for Packages and PCBs
- Package Reliability
- Others

PAPER SUBMISSION

All papers should be submitted electronically in two-column and three-page PDF file format. All submissions must be made through the EDAPS website (www.edaps2016.org). A Microsoft Word template is available on the symposium website. Hardcopy submissions will NOT be accepted. Submitted manuscripts should be camera ready and compliant with the general standards of the IEEE, including appropriate referencing. Non-compliant manuscripts will not be considered for review. An IEEE copyright transfer form completed with paper title, author(s) name(s) and authors' signatures should be submitted at the time of the paper submission. Files with scanned signatures are considered valid documents.

First Call for Papers

IEEE 67th Electronic Components and Technology Conference www.ectc.net

To be held May 30th - June 2nd, 2017

at the Walt Disney World Swan and Dolphin Resort, Lake Buena Vista, Florida USA

The Electronic Components and Technology Conference (ECTC) is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. ECTC is sponsored by the Components, Packaging and Manufacturing Technology (CPMT) Society of the IEEE. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the areas including, but not limited to as given below under each technical program subcommittee name. Authors are encouraged to review the sessions of the previous ECTC programs to determine the committee selection for their abstracts.

Advanced Packaging:

2.5 & 3D TSV Technologies, Embedded Technologies, Flip Chip, Fan-Out, Wafer Level Packaging, Panel Level Packaging, Advanced Substrates, Interposers, MEMS and Sensors, System-in-Package, System Integration, Heterogeneous Integration, EMI Shielding, RF/Microwave/Millimeter Wave Packaging, Power Management, Power Packaging, Novel Assembly Technologies, Internet-of-Things, Wearables, Bio-Compatible and Medical Packaging, Security, Automotive, Infotainment.

Applied Reliability:

TSV/2.5D/3D Packaging Reliability, WCSP/Fan-out/Embedded Package Reliability, Challenges in SiP reliability, Flip-Chip/Wire bond Interconnect Reliability, LED/RFID/High Voltage Packaging and IoT Reliability, System Level Reliability Testing/Modeling, Reliability Test Methods and Life Models, Physics of Failure, Failure Analysis Techniques and Materials Characterization, Drop and Dynamic Mechanical Reliability, Probabilistic Design for Reliability (PDR), Automotive Reliability Requirements.

Assembly and Manufacturing Technology:

Advanced Assembly Technology Solutions, Thermal Compression Bonding, Warpage Control Solutions, 2.5D/3D Package Assembly Technology, Packaging and Assembly Methods for Emerging Applications, Manufacturing Automation and Assembly Process Improvement, Trends in Predictive Assembly Modeling: Approach & Validation.

Emerging Technologies:

Hetero-Integration Concepts, Photovoltaic Packaging, Components for Wireless Packaging, Large Area Packaging and Manufacturing Processes, Quantum Computing Device Packaging, 3D Printing, New Additive Packaging Process Technologies and Materials, Novel Substrates, Novel Materials and Approaches to Packaging; Components for Internet-of-things, Wearable and Medical Electronics, Flexible, Bendable, Stretchable, Disposable, or Dissolvable Packaging Concepts, Compact & Autonomous Sensor Packaging, Interconnects for Nano-Devices and Sensors, New Materials for Nano-Interconnects, Bio-Sensor Packaging, Implantable Device Packaging, New Materials for Bio, Microfluidics and MEMS packaging, Small Form Factor/High Power Packaging, Novel High Performance Thermal Interface Materials, Packaging for Advanced Cooling, Energy Reuse and Harvesting, Packaging Processes for Security, Redundancy, Repair, Self-Alignment and Assembly, Organic IC & TFT, Anti-Counterfeiting Packaging, Nano-Battery Integration and Materials.

High-Speed, Wireless & Components:

Electrical Modeling & Design, Advanced Materials Integration, Passive and Active Components, Integrated Modules and Sub-Systems, Power and Signal integrity, High-Speed Data Transfer/Communications, Power and RF Modules, mm wave, THz, Radars, Imagers, Wearable and Sensor Technologies for Internet of Things (IoT), Flexible Electronics, 3D Printed RF Components and Modules, Biomedical Implants, Automotive Sensors, RF-MEMS, RF-Opto, RFID and Tagging, M2M Platforms, Ambient Intelligence, Wireless Power, Wireless Sensor/Computing Nodes.

Interconnections:

Interconnection Designs, Structures, Processes, Performance, Yield, Thermal/Mechanical/Electrical Tests & Reliability, Embedded Heterogeneous System Integration; Fan-Out and Fan-In Die-, Wafer- and Panel-level interconnects, 2.5D/3D stacking, TSV, Silicon/Glass/Organic Interposers, SiP, PoP, WLCSP, Flip Chip Interconnects, Solder Bumping and Cu Pillar, Thermal-Compression Bonding, TLPS IMC Interconnect, Wirebonds, Cu & Ag wire, RDL, Electrically Conductive Adhesives, Carbon Nanotubes, Graphene, Optical Interconnects, Flexible Substrates & Interconnection Solutions; Application Driven SiP Integration for Trillion Sensors, MEMS, Power Modules, Mobility, Wearables, Interconnects for Bio-Medical, Automotive, Datacenters, Cloud, Network and Harsh environments.

Materials & Processing:

Conductive and Non-Conductive Adhesives, 3D Materials and Thin Wafer Processing, Solder Alloys, Dielectrics, Underfills, Molding Compounds, Thermal Interface Materials, Novel Materials and Processing, Emerging Materials.

Thermal/Mechanical Simulation & Characterization:

Thermal, Mechanical and Multiphysics Modeling & Simulation, Component/Board/System Level Modeling including 3D Interconnects, 2.5D Packaging on Silicon/Glass/Flexible Interposers, Wafer-Level-Package, Ball-Grid-Array, Embedded Packages with Active and Passive Components, System-in-Package (SiP), Power Electronic Modules, LED Packaging, and MEMS; Reliability Modeling Related Fracture Mechanics, Fatigue, Electromigration, Warpage, Delamination/Moisture, Drop Test, Material Constitutive Relations and Characterization, Novel Modeling including Multi-Scale and Multi-Physics Techniques and Solutions; Measurement Methodologies, Characterization and Correlations.

Optoelectronics:

Silicon Photonics Integration, Optical Interconnects, Parallel Optical Transceivers, Silicon and III-V Photonics Packaging, Single Mode or Multicore Connectors, Optical Waveguide Coupling, Optical Chip-Scale and Heterogeneous Integration, Micro-Optical System Integration and Photonic System-in-Package, 3D Photonics Integration, Optoelectronic Integration for Internet of Things, Optoelectronic Assembly and Reliability, Materials and Manufacturing Technology, High-Efficiency LEDs and High Power Lasers, Integrated Optical Sensors.

Interactive Presentations:

Abstracts may be submitted related to any of the nine major program committee topics listed above. Interactive presentations of technical papers are highly encouraged at ECTC as it allows significant interaction between the presenter and attendees. It is especially suited for material that benefits from more explanation than is practical in oral presentations. Interactive presentation session papers are published and archived in equal merit with the other ECTC conference papers.

You are invited to submit an abstract of no more than 750 words that describes the scope, content, and key points of your proposed paper via the website at www.ectc.net.

If you have any questions, contact:

Mark Poliks, 67th ECTC Program Chair

Binghamton University, Watson School of Engineering & Applied Science,
PO Box 6000, Binghamton, NY 13902-6000, USA

Phone: +1-607-777-5361

E-mail: mpoliks@binghamton.edu

Abstracts must be received by October 10, 2016. All abstracts must be submitted electronically at www.ectc.net. You must include the mailing address, business telephone number, and email address of presenting author(s) and affiliations of all authors with your submission.

Professional Development Courses

In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses (4 hours) on topics described in the Call for Papers. Using the format "Course Objectives/Course Outline/Who Should Attend," 200-word proposals must be submitted via the website at www.ectc.net by October 10, 2016.

If you have any questions, contact:

Kitty Pearsall

67th ECTC Professional Development Courses Chair

Boss Precision, Inc.

1806 W. Howard Lane, Austin, TX 78728, USA

Phone: +1-512-845-3287

E-mail: kitty.pearsall@gmail.com

Call for Abstracts
(Due August 25, 2016)

ITherm 2017

ITherm 2017: Sixteenth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems May 30 – June 2, 2017 Walt Disney World Swan & Dolphin Hotel Lake Buena Vista (Orlando), FL USA

ITherm 2017 is the leading international conference for scientific and engineering exploration of thermal, thermo-mechanical and emerging technology issues associated with electronic devices, packages, and systems. ITherm 2017 will be held along with the 67th Electronic Components and Technology Conference (ECTC 2017, www.ectc.net), a premier electronic packaging conference, at the Disney World Resort. Joint registrations are available at a discounted rate. All papers will be peer reviewed by two or more reviewers, and will be published in the ITherm proceedings. Selected papers will be published in a special issue of Journal of Electronics Packaging. All papers will be presented in oral sessions. Students have the opportunity to apply for ITherm travel grants and make an oral presentation and also participate in poster presentation of their paper and compete for poster awards. In addition to paper presentations and vendor exhibits, ITherm 2017 will have panel discussions, keynote lectures by prominent speakers, and professional short courses. Original papers are solicited in the following general areas of interest (but not limited to):

Thermal-1 Component Level -- Track I

- Single/Multi-Chip Module, System in Package
- 3D Packaging, Embedded Cooling
- Heat Pipes, Vapor Chambers, Thermosyphons
- Heat Spreaders
- Hot Spot Cooling
- Thermoelectric
- Single & Two-Phase Cold Plates
- Pumps, Fans
- Heat Exchangers, Air Cooling

Thermal-2 System Level -- Track II

- Data Center, Energy Efficiency
- Thermal Storage
- Immersion Cooling, Refrigeration
- Mobile, Internet of Things, MEMS
- Telecommunication Systems
- Automotive
- Space and Aerospace
- Power Electronics
- LEDs
- Photovoltaics
- RF Electronics
- Battery

Mechanics & Reliability -- Track III

- Thermo-mechanical Modeling and Simulation of Devices, Components, Boards, and Systems
- Mechanics and Reliability of Solder Joints & Interconnects
- Materials Characterization, Processing, Constitutive Models
- Failure Mechanics, Fatigue, Damage Modeling
- Experimental Techniques for Packaging Deformations, Strains, and Stresses
- Shock, Drop, and Vibrational Analysis of Packages, Sub-Systems, and Systems
- TSV / 3D Reliability and Packaging Challenges
- Mechanics issues in Assembly and Manufacturing

Emerging Technologies & Fundamentals -- Track IV

- Numerical Methods from Nano-to-Macro Scale
- Experimental Methods from Nano-to-Macro Scale
- Nanotechnology incl. 1&2-Dimensional Materials
- Thermal Interface Materials, Phase Change Materials
- Embedded Cooling
- Transistor Technology
- Novel Materials and Manufacturing Techniques
- Measurement and Instrumentation Techniques
- Prognostic Health Management and Reliability Analysis

Some important dates:

Deadline for Abstracts: August 25, 2016
Notification of Acceptance: Sept. 30, 2016
Draft Paper Submission: Dec. 1, 2016
Reviews Returned: Feb. 1, 2017
Final Paper Submission: Mar. 1, 2017

Direct general inquiries to:

Professor Michael Ohadi
General Chair, Email: ohadi@umd.edu
Program inquiries to Dr. Thomas
Brunschwiler, Program Chair, Email:
TBR@zurich.ibm.com

Visit us: www.ieee-ITherm.org

Call for Papers

Abstract Deadline

August 30, 2016

Sheraton Kauai Resort
Kauai, Hawaii
February 6-9, 2017



Microelectronic Symposium "Best of Today, Preview of Tomorrow"

The Pan Pacific Microelectronics Symposium promotes international technical exchange and provides a premier forum for extensive networking among professionals and business leaders throughout the Pacific Basin. All papers published in conference proceedings, SMTA Knowledge Base and submitted to IEEE Xplore Digital Library.



IEEE COMPONENTS, PACKAGING AND
MANUFACTURING TECHNOLOGY SOCIETY



IEEE

3D/Heterogeneous Integration Build

Blind & Buried Via PWBs
Cu Pillars & Posts MCM/SiP Advances
Module Stacking Origami Flex Packages
Package on Package (PoP) Shaped Circuits
Through Si Vias (TSV)

Photonics

Fabrication
Integration Techniques

Emerging Technologies

Advanced Interconnect
Embedded Assembly (Passive & Active)
Interposer Technologies (Si, Glass, etc.)
Thermal Management
Structural Electronics

Reliability, Quality

Failure Analysis
Quality Assessment
Reliability Physics
Test & Measurement
Yield Projection

High Performance Low I/O

Chip on Glass (CoG)
Compact Florescent Systems
Optoelectronics
Developments MEMS/MOEMS
Display Drivers
Flat Panel Processes
LED Packaging & Assembly
Lighting & Displays OLED
Optoelectronics

Material Advances

Connections (Adhesives, Solders, etc.)
Integrated Passive Devices Interconnect
Taxonomy
Interface Metallurgy (FC, WB, TAB, Pb
Free Soldering, etc.)
Interface Materials (TIMs) Thin & Thick
Phosphors & Light Absorption
Thermal Film Systems

IoT

Edge Devices
Flexible Electronics
Medical and Healthcare devices
Printed Electronics
Sensor Technology
Wearable Electronics

Green Electronics

Environmental Impact Analysis
Green Manufacturing (Pb/Halogen free,
etc.) Large Area/Module Assembly
Photovoltaics
Power Control/Conversion/Distribution
Power Packaging
Solar Thermal Conversion

Nanotechnology

Applications in Electronics
Materials
Processes & Handling
Smart Devices

Strategic Direction/ Industry Roadmaps

Economics & Cost Analysis
Health & Prognostics
Manufacturing Management & Control
Penetration Strategies
Supply Chain & Operations Management
Technology Drives

2017 Steering Committee

Charles E. Bauer, Ph.D., TechLead Corp.
Ross Berntson, Indium Corp.
Dock Brown, DfR Solutions
Phil Isaacs, IBM Corp.

Soeren Noerlyng, MICRONSULT
Yasumitsu Orie, Ph.D., IBM Corp.
David Raby, STI Electronics
Jing Zhang, IBM Corporation

**NOW
ACCEPTING
ABSTRACTS**

www.smta.org/panpac

Upcoming CPMT Sponsored and Cosponsored Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the CPMT Society sponsors and supports a number of global and regional conferences, workshops and other technical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through IEEE Xplore.

For details go to: www.cpmnt.ieee.org

Name: 2016 17th International Conference on Electronic Packaging Technology (ICEPT)
Location: Wuhan, China
Dates: Aug 16, 2016–Aug 19, 2016

Name: 2016 Electronics Goes Green 2016+ (EGG)
Location: Berlin, Germany
Dates: Sep 7, 2016–Sep 9, 2016

Name: 2016 38th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)
Location: Garden Grove, CA USA
Dates: Sep 11, 2016–Sep 16, 2016

Name: 2016 6th Electronic System-Integration Technology Conference (ESTC)
Location: Grenoble, France
Dates: Sep 13, 2016–Sep 16, 2016

Name: 2016 IEEE 37th International Electronics Manufacturing Technology (IEMT) & 18th Electronics Materials and Packaging (EMAP) Conference
Location: Georgetown, Penang, Malaysia
Dates: Sep 20, 2016–Sep 22, 2016

Name: 2016 IEEE 62nd IEEE Holm Conference on Electrical Contacts (Holm)
Location: Tampa, FL USA
Dates: Oct 9, 2016–Oct 12, 2016

Name: 2016 IEEE 25th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
Location: TBD, CA USA
Dates: Oct 23, 2016–Oct 26, 2016

Name: 2016 11th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)
Location: Taipei, Taiwan
Dates: Oct 26, 2016–Oct 28, 2016

Name: 2016 IEEE CPMT Symposium Japan (ICSJ)
Location: Kyoto, Japan
Dates: Nov 7, 2016–Nov 9, 2016

Name: 2016 IEEE International 3D Systems Integration Conference (3DIC)
Location: San Francisco, CA USA
Dates: Nov 8, 2016–Nov 11, 2016

Name: 2016 IEEE 18th Electronics Packaging Technology Conference (EPTC)
Location: Singapore, Singapore
Dates: Nov 30, 2016–Dec 3, 2016

Name: 2016 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)
Location: HI, USA
Dates: Dec 14, 2016–Dec 16, 2016

Name: 2017 Pan Pacific Microelectronics Symposium (Pan Pacific)
Location: Kauai, HI USA
Dates: Feb 6, 2017–Feb 9, 2017
Abstract Submission Date: Aug 30, 2016

Name: 2017 IEEE International Workshop On Integrated Power Packaging (IWIPP)
Location: Delft, Netherlands
Dates: Apr 5, 2017–Apr 7, 2017
Abstract Submission Date: Nov 18, 2016

Name: 2017 IEEE 67th Electronic Components and Technology Conference (ECTC)
Location: Orlando, FL USA
Dates: May 26, 2017–Jun 3, 2017
Abstract Submission Date: Oct 14, 2016

Getting the Most out of IEEE and CPMT Membership: eBooks

Did you know that IEEE members now have access to more than 220 eBooks from the IEEE Press collection through IEEE Xplore, including: handbooks; introductory and advanced texts; reference works; professional books.

Follow 3 simple steps:

1. Log in to IEEE Xplore <http://www.ieeexplore.ieee.org/Xplore/guesthome.jsp> using your IEEE Member Web account.
2. Under the “Browse” heading in the left-hand navigation, click on “Books”.
3. Select the “Classics” tab from the top of the page. Under this tab you will find a listing of all the Free titles.

Here are a few examples of available books in pdf format: (more added every year)

1. *Lead-Free Electronics: iNEMI Projects Lead to Successful Manufacturing* by E. Bradley, C. Handwerker, J. Bath, R. Parker and R. Gedney; Publication Date: 2007
2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. *Silicon Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Hareme; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

For more information visit: http://www.ieee.org/membership_services/membership/products/ebookclassics.html