Components, Packaging, and Manufacturing Technology Society Newsletter

THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

VOL. 40 NO. 1, SUMMER 2017, ISSN 1077-2999 cpmt.ieee.org

President's Column....

Jean Trewhella
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Dear Society members,

I am just back from ECTC, our flagship US conference where we had record breaking participation again! It was a great demonstration of our Society's fundamental belief in collaboration through the sharing of high-quality technical content, the discussion of thought provoking questions, and close interaction with our colleagues from around the world. We do this not just through our conferences but also through our workshops, webinars, publications, and most recently through our major initiative the **Heterogeneous Integration Roadmap (HIR)**. We see a change in the industry where packaging is growing its impact in all areas of electronics and driving substantial new product value.

With this change it is even more critical to leverage our combined strengths and collaborate across all areas of our Field Of Interest. In this vain I am happy to announce that the CPMT Society name change to **Electronics Packaging Society** has been approved by the IEEE Board of Directors! We are now asking for your help and your support to realize the intended benefits of this change:

Improved Society Branding

- Shorter, simpler name
- Growing Industry recognition that packaging is strategic in all areas of electronics

More inclusive and better representation of the broad FoI of our society

- Simple name helps to not exclude topics: Eg. "Manufacturing" in our name could imply exclusion of "Research" focus which is also part of our FoI.
- Makes it clear that our focus is every niche and aspect of packaging and interconnection of ICs

Improved clarity will result in increased collaboration with other IEEE societies

- Packaging topics showing up more in other societies conferences and workshops
- Our society wants to be a source of expertise to work with other societies to make this successful

We will be rolling this out quickly so watch for updates, additional information, and ways for you to engage on the Society webpage! Our first ask is to **cast your vote to select our new LOGO.**

Jean Trewhella
IEEE EPS President

NEWSLETTER SUBMISSION DEADLINES:

30 August 2017 for Fall issue 2017
1 November 2017 for Winter issue 2018
1 March 2018 for Spring issue 2018
1 July 2018 for Summer issue 2018

Submit all material to nsltr-input@cpmt.org

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2019 term end: Regions 1–6,7,9—Li Li, David McCann, Kitty Pearsall, Subramanian S. Iyer; Region 8—Thomas Brunschwiler, Gilles Poupon

Publications

Transactions on Components, Packaging and Manufacturing Technology

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Lecturers: Mudasir Ahmad, Muhannad Bakir, Ph.D., Avram Bar-Cohen, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., Moises Cases, William T. Chen, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., R. Wayne Johnson, Ph.D., Beth Keser, Ph.D., John H. Lau, Ph.D., Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., Ravi Mahajan, PhD., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Michael Pecht, Ph.D., Eric D. Perfecto, Karl J. Puttlitz, Ph.D., Dongkai Shangguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branch Chapters

Refer to cpmt.ieee.org for EP Society Chapters and Student Branch Chapters list

IEEE Electronics Packaging Society (formerly CPMT) Newsletter is published quarterly by the IEEE Electronics Packaging Society (formerly CPMT) of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US $1.00 per member per year is included in Society fee for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE EPS Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. For circulation information call IEEE Customer Service 800-701-4333, or FAX 908-981-9667.

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Heterogeneous Integration Roadmap

A. Introduction

We are in the Digital Economy. Industrial, academic, and governmental organizations in every part of the world are responding rapidly to the commercialization of data generation and data access, drawing on the wealth of data for adding knowledge and gaining insight into their operations. Image intensive applications from entertainment to health and medicine are growing creating exponential escalation of big data and data analytics.

New applications in data analytics, such as artificial intelligence and augmented reality, are being adopted by every profession, every industry and every aspects of daily living. The progress towards self driven vehicles is real, and it is almost here leading to disruptive change in the automotive industry and transportation systems worldwide. New data center architectures and new network systems are springing up in response to the flood of data and demand for bandwidth with lower latency.

The electronic industry is at the forefront, providing hardware platforms and software solutions to address emerging requirements of this new digital landscape. The pace of technology innovation across the broad ecosystem continues to expand to meet the challenges of this new digital era. Four major driving forces are:

- The Internet of Thing and Wearables
- Smart and Smarter Mobile Devices
- Migration to the Cloud – Data Centers and the Global network
- Autonomous Transportation

The crucial question is: What are the critical paths going forward?

Our Society initiated the Heterogeneous Integration Roadmap early in 2016 to meet the need for a technology roadmap providing a long term vision to the future where innovation in packaging and heterogeneous integration will be a key enabling elements. (Please see CPMT Newsletter Summer 2016) Our goal for this roadmap is to be open and transparent. Collaborating with other organizations worldwide to generate the Roadmap and sharing it with everyone to stimulate pre-competitive collaboration across industry, academia and government to accelerate the pace of progress.

IEEE EPS provides institutional sponsorship to ensure sustainability and quality. We have established a Heterogeneous Integration Roadmap web page link in the EPS (CPMT) Web site, which also includes a list of upcoming HIR workshops. **http://cpmt.ieee.org/technology/heterogeneous-integration-roadmap.html**

B. Roadmap Collaboration

Today the Heterogeneous Integration Roadmap activities are sponsored by IEEE Electronic Packaging Society (EPS), SEMI, IEEE Electron Devices Society (EDS), IEEE Photonics Society and the ASME EPPD Division. We welcome collaboration with other IEEE Technical Societies and Councils that share interest in the Heterogeneous Technology Roadmap as well as organizations outside IEEE that share this common vision. We believe that our Societies are rich in creativity, innovation and knowledge across science, technology and arts associated with electronics. We have the deep knowledge base from the Societies' global membership and worldwide network for the roadmap mission, HIR is working in collaboration with other roadmaps and their sponsor organizations. The science and technologies for the electronic industry are multilayered and multifaceted. Different roadmaps view the future from different vantage points of their technology space. Working together and collaboration across the industry will indeed greatly enrich our vision to the future.

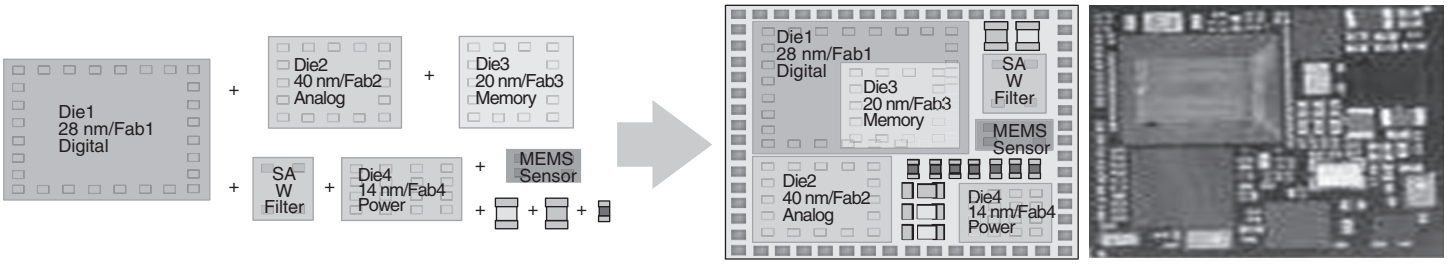
In addition to Heterogeneous Integration Roadmap sponsored by three IEEE Societies and two other organization, there are two other roadmaps under development in IEEE: International Technology Roadmap for Devices and Systems (IRDS) sponsored by the IEEE Standards Association and associated with the Rebooting Computing Initiative, and the International Technology Roadmap for Wide Band-Gap Semiconductors (ITRW) sponsored by the IEEE Power Electronics Society. We have had several meetings under IEEE auspices with the goal or collaboration and cooperation within IEEE to provide a common voice to the technical community worldwide.

C. Heterogeneous Integration Definition

How is Heterogeneous Integration defined? Heterogeneous Integration refers to the integration of separately manufactured components into a higher level assembly such as System-in-Package (SiP), that, in the aggregate, provides enhanced functionality and improved operating characteristics.

In this definition components should be taken to mean any unit whether individual die, MEMS or Sensor device, passive component and assembled package or sub-system that are integrated into a single package. The operating characteristics should also be taken in its broadest meaning including characteristics such as system level performance and cost.

In this sense the roadmap is a system hardware integration roadmap with strong application focus. In this digital age, hardware is



Heterogeneous Integration Illustration; Source ASE Group.

HIR Breakout session after the HIR Plenary presentation at ICEP Conference in Japan April 2017.

a platform for market applications whether they are in mobile, IoT, big data, health, or automotive when integrated into systems.

In view of the fast pace change in industry and technology, we have established a Global Advisory Council to provide high level guidance and counsel to the Roadmap Committee.

D. Roadmap Chapters and Technical Working Groups

The work of the Roadmap involves a specific set of technical working groups each addressing a specific topic in Heterogeneous Integration. They are divided in 6 specific categories as shown below.

a) Heterogeneous Integration of Components
- Single Chip and Multi Chip Packaging (including Substrates)
- Integrated Photonics
- Integrated Power Devices
- MEMS and Sensors
- RF and Analog Mixed Signal

b) Cross Cutting topics
- Materials and Emerging Research Materials
- Emerging Research Devices
- Interconnect
- Test
- Supply Chain

c) Integration Processes
- System in Package (SiP)
- 3D +2.5D
- Wafer Level Packaging including fan in and fan out (including panel processing)

d) Heterogeneous Integration for Specialized Applications
- Smart Mobile Devices – Smart Phone
- High Performance Computing
- IoT and Wearable
- Medical and Health
- Automotive
- Aerospace and Defense

e) Design methodology and tools
- Co-Design and Modeling and Simulation

Our industry is a global industry. Our professionals, whether in companies, academia, research institutes or government, are around the globe. The work for the Roadmap must involve the global technical professional and our global society membership. We have scheduled talks and workshops around the world mainly at EPS and partner technical conferences and workshops reaching out to the technologists at these events. Good examples are the ICEP in Japan in April, ECTC in Orlando in May and NorPACK in June.

The next major Roadmap workshop will be at Semicon West on July 9th and 10th. A full list of 2017 events may be found in the roadmap web link. We would like to invite everyone who are interested to visit the web page and we welcome your participation and contribution.

Our goal is to have the white paper and chapter outline done for the Technical Working Groups at the Semicon West workshop. This will give us the next five months to complete the chapters by year end, and publication in January 2018.

E. Concluding Remarks

The Heterogeneous Integration Roadmap is a technology roadmap with a broad coverage of our society's field of interest. It is our technology roadmap for our profession whether we work in industry, academia, research institutions and government.

William (Bill) Chen
WR (Bill) Bottoms

2017 IEEE EPS Society Award Recipients

An IEEE Fellow, Ho is director of the Laboratory for Interconnect and Packaging at the University of Texas at Austin, Austin, TX, USA. Tu is the TSMC Chair Professor at National Chiao Tung University, Hsinchu, Taiwan.


Paul S Ho and King-Ning Tu

2017 IEEE Components, Packaging and Manufacturing Technology Award

For contributions to the materials science of packaging and its impact on reliability, specifically in the science of electromigration

Daoqiang (Daniel) Lu, Henckel Corporation Shanghai, China

2017 IEEE CPMT Electronics Manufacturing Technology Award

For significant contributions to improve the manufacturing process of mobile devices with innovative materials and processing solutions.

Xuejun Fan, Department of Mechanical Engineering, Lamar University, USA

2017 IEEE CPMT Outstanding Sustained Technical Contribution Award

For sustained and outstanding contributions to the modeling and characterization of IC packaging, LED packaging and system reliability, and new interconnect material development in wafer level packaging, 3D integration and power electronics packaging.

Ephraim Suhir, ERS Co., USA

2017 IEEE CPMT Exceptional Technical Achievement Award

For the development of numerous probabilistic design concepts that enable effective and rapid assessment of the probability or failure of electronic products.

Patrick Thompson, Texas Instruments, Inc., USA

2017 IEEE CPMT David Feldman Outstanding Contribution Award

For outstanding, sustained contributions to CPMT at the Chapter, Society and conference levels for more than 30 years. He has held a large range of leadership positions and has implemented multiple improvements and advancements, added value and provided an innovative mindset.

Yan Liu, Medtronic, Inc. USA

2017 Outstanding Young Engineer Award

For outstanding contributions to the field of electronic packaging materials and nanotechnology through work in the superhydrophobic surface for energy and electronic applications, novel polymeric materials for advanced coating and electronic packaging.

Shen-Li Fu, I-Shou University, Taiwan

2017 IEEE CPMT Regional Contributions Award - Region 10 (Asia and Pacific)

For contributions to the development of the IEEE CPMT Taipei Chapter and the successful establishment of a professional interactive platform among the chapters in Region 10, through international conferences.

Congratulations to IEEE Fellows Class of 2017

Listed below are new IEEE Fellows who are members of the EP Society. See a list of all EPS members who are IEEE Fellows at: http://cpmt.ieee.org/awards/ieee-fellows-program.html

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11)

Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Eric Perfecto
Global Foundries, USA
For the development of Pb-free, flip chip solder interconnect and advancements to multi-level Cu-polyimide packages.

Ning-Cheng Lee
Indium Corporation, USA
For leadership in Surface Mount Technology and interconnect materials.

Congratulations to IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between February and June 2017.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at https://www.ieee.org/membership_services/membership/senior/application/index.html

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Michael Cracraft,
Mid-Hudson Section
Roy Davis,
Southeastern Michigan Section
Mysore Divakar,
Santa Clara Valley Section
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Denver Section
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FranceSection
Eiji Higurashi,
Tokyo Section
Francesca Iacopi,
New South Wales Section
Hideyuki Nasu,
Tokyo Section
Jeffrey Suhling,
Montgomery Subsection
Yutaka Uematsu,
Tokyo Section

The Society collaborates and cooperates with other IEEE Societies as well as with other professional associations through initiatives, publications, conferences and councils. Following are some of the areas and activities that EPS jointly sponsors or supports:

Activities/Initiatives
Heterogeneous Integration Road Map
Women in Engineering
IoT
Rebooting Computing
5G

Councils
Sensors Council
Council on RFID
Nanotechnology Council
Superconductivity Council

Publications
IEEE Transactions on Semiconductor Manufacturing
IEEE Transactions on Nanotechnology
IEEE Nanotechnology Magazine
IEEE Internet of Things Journal

IEEE Sensors Journal
IEEE RFID Virtual Journal
IEEE Transactions on Applied Superconductivity
IEEE Journal on Exploratory Solid-State Computational Devices and Circuits
IEEE Journal on Photovoltaics
IEEE Transactions on NanoBioscience
IEEE Transactions on Big Data
IEEE Transactions on Multi-Scale Computing Systems
IEEE Transactions on Molecular, Biological, and Multi-Scale Communications
IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology

Conferences
ASMC, DTIP, EOS/ESD, EMPC, EuroSIME, ICEPT, ISSE, THERMINIC, EDAPS, EPEPS, EPTC, ESTC, IEMT-EMAP, IWASI, IWIPP, SPI

Upcoming Webinar

Microassembly Using Elastomer Stamps, August, 9, 2017.
More details to come.

EPS Chapter News....

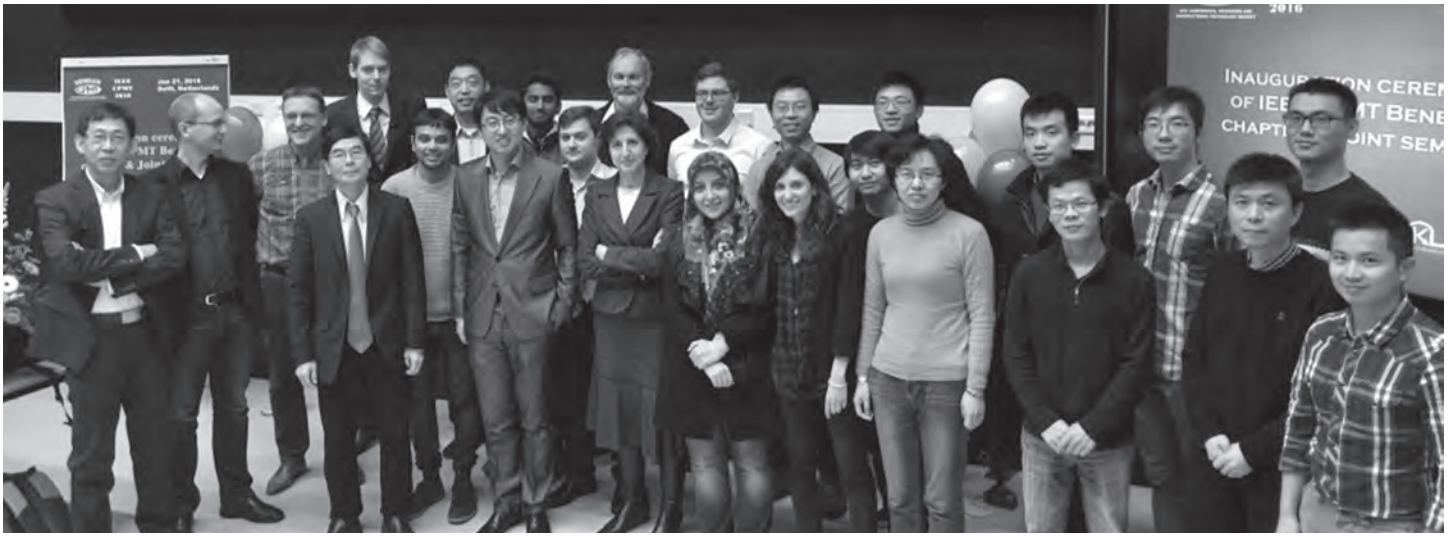
Electronics Packaging Society Benelux Chapter Establishment and Joint Seminar

Benelux has been a very active region in electronics and microelectronics packaging related research and development for decades. Thus, IEEE Electronics Packaging Society has over 35 members in Benelux, which is the 3rd largest in Europe. However, no technical chapter is available to serve as an efficient platform for members to communicate. Under the circumstances, the former regional director Dr. Toni Mattila approached Prof. G.Q. Zhang, who is one of the two IEEE fellows in Benelux, to discuss the possibility to initiate a chapter. Prof. Zhang felt very positive towards the proposal, and he introduced his postdoc Dr. Jing Zhang to Dr. Mattila for arrangement of the petition.

With the help of Dr. Mattila, Dr. Zhang contacted the members and received replies with great enthusiasm. More than 45% members signed up for the petition even in the summer holiday period. Therefore, after a successful petition presentation in IEEE Benelux EXCOM, the petition was submitted to the committee, and finally got approved in December 2015.


Prof. Lina Sarro welcomed attendants and guests.

This chapter is meant to represent the interests of EPS members in the **Bel**gium, **Ne**therlands, and **Lux**embourg area and inspire cooperation, further the career opportunities of its members, host



regular talks and seminars, and form a bridge between academia and industry.

In order to further broadcast this great news, an inauguration ceremony of the newly formed chapter together with a joint seminar took place on the 21st of January 2016 in Delft (Netherlands) at TU Delft. All the attendants and guests were firstly welcomed by Prof. Lina Sarro on behalf of Dr. Rob Fastenau, who is the dean of Electrical engineering faculty.

She expressed sincere wishes in the future of the new chapter, and hope attendants enjoy the following seminar.

For the inauguration, Prof. C.P. Wong officially announced the opening of Benelux chapter representing the EPS society.

Publication News....

2016 EPS Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 200 published papers and represent the best, based on criteria including originality, significance, completeness and organization. The awards were presented at the 67th Electronic Components and Technology Conference (ECTC), June 2017.

Subscribers to this publication can access the papers on-line in IEEE Xplore at:

URL: http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870

Advanced Packaging Technologies Category

Finite Element Analysis and Experimental Test for a Capped-Die Flip Chip Package Design
Yuci Shen, Leilei Zhang, Weihang Zhu, Jiang Zhou, Xuejun Fan, Vol. 6, No. 9, September 2016

Abstract: In flip-chip packages, the coefficient of thermal expansion (CTE) mismatch between the chip and the substrate is the root cause for reliability issues such as excessive warpage, low-k dielectric layer cracking, solder mask cracking, and bump cracking. The first and foremost thing in designing a flip-chip package is to meet the warpage specification. This paper proposes a capped-die flip-chip package to control the warpage as well as to reduce the stress in solder bumps. In the capped-die flip-chip package, a metal cap tightly covers and bonds with the die through an adhesive material, leading to a capped die with a higher effective CTE. By adjusting the thickness of the metal cap, the effective CTE of the capped die may match with that of the substrate, theoretically achieving zero warpage or warpage free. Guided by finite-element analysis, a 45×45-mm^2 size of capped-die flip-chip package was manufactured, and a copper die cap with 0.4 mm thickness is selected to verify this concept. Shadow Moireé test data showed that in the temperature range from 25 °C to 260 °C, the warpage curve of the capped-die package is almost flat and close to zero, confirming the cappeddie concept. Furthermore, finite-element modeling was used to investigate the stress in bump, as well as the thermal performance of the capped-die flip-chip packages. It is found that thermal performance of the capped-die package can be good enough for high-power applications. The bump stress of the capped-die package is about 50% lower compared to the lidded package. The applications of the capped-die package design in coreless substrate packages are also discussed in this paper.

URL: http://ieeexplore.ieee.org/document/7553583/

Components: Characterization and Modeling Category

Chip To Chiller Experimental Cooling Failure Analysis Of Data Centers: The Interaction Between It And Facility
Husam Alissa, Kourosh Nemati, Bahgat G. Sammakia, Mark J. Seymour, Russell Tipton, David Mendo, Dustin W. Demetriou, Ken Schneebeli, Vol. 6, No. 9, September 2016

Abstract: Cooling failure in data centers (DCs) is a complex phenomenon due to the many interactions between the cooling infrastructure and the information technology equipment (IT). To fully understand it, a system integration philosophy is vital to the testing and design of experiment. In this paper, a facility-level DC cooling failure experiment is run and analyzed. An airside cooling failure is introduced to the facility during two different cooling set points as well as in open and contained environments. Quantitative instrumentation includes pressure differentials, tile airflow, external contour and discrete air inlet temperature, intelligent platform management interface (IPMI), and cooling system data during failure recovery. Qualitative measurements include infrared imaging and airflow visualization via smoke trace. To our knowledge of current literature, this is the first experimental study in which an actual multi-aisle facility cooling failure is run with real IT (compute, network, and storage) load in the white space. This will establish a link between variations from the facility to the central processing unit (CPU). The results show that using the external IT inlet temperature sensors, the containment configuration shows a longer available uptime (AU) during failure. However, the IPMI data show the opposite. In fact, the available uptime is reduced significantly when the external sensors are compared to internal IT analytics. The response of the IT power, CPU temperature, and fan speed shows higher values during the containment failure. This occurs because of the instantaneous formation of external impedances in the containment during failure, which renders the contained aisle to be less resilient than the open aisle. The tradeoffs between PUE, OPEX, and AU are also explained.

URL: http://ieeexplore.ieee.org/document/7557014/

Electrical Performance of Integrated Systems Category

Efficient Total Crosstalk Analysis of Large Via Arrays in Silicon Interposers

David Dahl, Torsten Reuschel, Jan Birger Preibisch, Xiaomin Duan, Ivan Ndip, Klaus-Dieter Lang, Christian Schuster, Vol. 6, No. 12, December 2016

Abstract: In this paper, we present for the first time a rigorous crosstalk analysis of through silicon via (TSV) arrays consisting of several hundreds of TSVs in interposers with metallized surfaces, using the physics-based via (PBV) modeling approach for applications up to 500 GHz. The PBV modeling approach is valid for complete and almost complete metallizations of the substrate where radial wave propagation in the parallel-plate structure dominates the electromagnetic properties and is utilized with models of good accuracy for localized and propagating fields in the inhomogeneous dielectrics. The approach shows very good to good agreement of crosstalk results for frequencies up to 500 GHz in comparison to full-wave simulations and attains a speedup of at least two orders of magnitude in comparison to general-purpose simulators. The definition of a weighted power sum for total uncorrelated crosstalk is applied for all channels in the TSV array. These power sum results give more meaningful insights into the global effects of the parameter variations than single crosstalk contributions. Based on variations of several technology and design parameters of TSVs, we derive quantitative estimations of the impact of these parameters on the total crosstalk.

URL: http://ieeexplore.ieee.org/document/7742348/

Electronics Manufacturing Category

Materials Characteristics of Ag-Alloy Wires and Their Applications in Advanced Packages

Chih-Hsin Tsai, Chien-Hsun Chuang, Hsing-Hua Tsai, Jun-Der Lee, Dennis Chang, Hsin-Jung Lin, Tung-Han Chuang, Vol. 6, No. 2, February 2016

Abstract: The materials characteristics of annealing-twinned Ag-alloy wires with various Au and Pd contents were evaluated in this paper. The results indicated that both Ag-8Au-3Pd and Ag-15Au-3Pd have higher strength and corrosion resistance than do pure Ag and binary Ag-Pd wires. On the other hand, the pure Ag, Ag-0.5Pd, Ag-3Pd, and Ag-4Pd wires possess the merits of lower material cost, higher electrical conductivity, and higher electromigration durability than do the ternary Ag-Au-Pd wires. However, the breaking load and elongation of pure Ag wire are inferior to those of Ag-0.5Pd, Ag-3Pd, and Ag-4Pd wires. In addition, the corrosion resistances of pure Ag and Ag-0.5Pd wires are far inferior to those of Ag-3Pd and Ag-4Pd wires. Based on these performances, the ternary Ag-8Au-3Pd wire is an ideal substitute for the traditional Au wire due to its high strength, corrosion resistance, and reliability, while the Ag-3Pd and Ag-4Pd are cost-friendly bonding wires for high-frequency integrated circuit devices.

URL: http://ieeexplore.ieee.org/document/7384455/

Conference News....

Over 1,400 in Attendance at the 67th ECTC in Orlando

Submitted by Nancy Stoffel, Assistant Program Chair, IEEE ECTC 2018

This year's IEEE Electronic Components and Technology Conference (ECTC) was held at the Walt Disney World Swan and Dolphin Resort, Lake Buena Vista, Florida from May 30 to June 2, 2017. Even in the midst of industry consolidation and corporate travel restrictions, the conference exceeded 1,400 attendees for the third time in its 67 year history, with a total of 1,439 industry professionals in attendance.

This was a record for attendance in Orlando, 23% more than in Orlando in 2014, and 68% more than in 2011. The conference included 335 technical contributions, which were organized into 36 oral sessions and 5 interactive presentation (IP) sessions. For the fourth straight year the conference had over 100 exhibitors at the Technology Corner Exhibit, a tribute to the quality of the conference and its attendees. The 67th ECTC benefited from a record number of sponsors and sponsorship, further testament to the value delivered by this flagship conference.

Preparations for the 67th ECTC started last October, when the professional volunteers serving in the technical committees

The attendance at the 67th ECTC exceeded 1,400 for the third time.

reviewed a record number of 576 submitted abstracts. Ultimately, 60% of the submissions were accepted, leading to 337presentations at the conference. This year, 45% of the submitted abstracts were from corporations, and 55% were from academia and from research institutions. In a testimony to the diversity of the industry and the conference, abstracts were received from 26 countries.

The conference program, consisting of 36 oral sessions and 5 interactive presentation sessions, came together at the Technical

Rao Tummala instructing PDC attendees on "Future of Device and Systems Packaging: Strategic Technologies, Manufacturing Infrastructure, and Applications."

Bill Bottoms (standing), along with Bill Chen/ASE led a full day workshop on Heterogeneous Integration Technology Roadmap. For more information visit: http://cpmt.ieee.org/technology/heterogeneous-integration-roadmap.html

Jean Trewhella/GLOBALFOUNDRIES (standing), EPS President co-chairs with Young Gon Kim/Integrated Device Technology the Panel Fan-Out Manufacturing panel session on Tuesday night. The panelists seated are (from left to right) Douglas Yu/TSMC, Steffen Kroehnert/NANIUM, Steve Bezuk/Qualcomm Technologies Inc., Rolf Aschenbrenner/IZM Fraunhofer, and Tim Olson/DECA.

Students enjoy yo-yos provided by Texas Instruments, sponsor of the 2017 ECTC Student Reception.

Program Committee's annual planning meeting near Dallas, Texas, on November 3 and 4th, 2016. The subcommittee chairs and session chairs did a great job developing interesting sessions and communicating with their session authors, which enabled all the manuscripts to be publication ready well before the start of the conference. ECTC again utilized the IEEE Computer Society Conference Publishing Services (CPS) to receive and process manuscripts. As in previous years, the IEEE CrossCheck system was used to ensure that all of the ECTC manuscripts maintain a high level of original content.

As usual, the first day of the conference, the Tuesday following Memorial Day, included professional development courses (PDCs), special sessions and workshops. This year, the conference had nine morning PDCs, running from 8 a.m. to noon, and another nine afternoon PDCs, running from 1:30 p.m. to 5:30 p.m. The total number of PDC attendees was 473 which was the highest attendance ever. The courses continue to serve a convenient way for students and engineers to quickly get "up to speed" on many important subjects, such as wafer-level and fan-out packaging, 3D integration, and various aspects of reliability. There were two new courses this year, as well as two contributed by instructors from the concurrently held ITherm conference.

This year, there were three special sessions on Tuesday. At 10 a.m., Vikas Gupta from Texas Instruments, Inc. and Pradeep Lall from Auburn University jointly chaired a panel session titled "Material and Package Reliability Needs/Challenges for Harsh Environments". During this panel, the attendees were treated to candid and insightful thoughts from experts in the field, which included: Robert Smith from Boeing Research & Technology, Przemyslaw Jakub Gromala from Bosch, Steve Dunford from Schlumberger, Anton Z. Miric of Heraeus Deutschland GmbH & Co. KG, and Nancy Stoffel from GE Global Research. At 2 p.m., Bing Dang from IBM chaired a special panel session entitled "Flexible Hybrid Electronics-Electronics Outside the Box". The distinguished panelists included: Benjamin Leever from the Air Force Research Lab, James L. Zunnin from the US Army RDECOM ARDEC, Robert Smith from Boeing Research & Technology, Girish Wable from Jabil, and John Knickerbocker from IBM Corporation.

On Tuesday evening at 7:30 p.m., Jean Trewhella, EPS President, from GLOBALFOUNDRIES, and Young Gon Kim from Integrated Device Technology, chaired a panel on "Panel Fan-Out Manufacturing: Why, When, and How?". This evening panel included contributions from technology leaders from around the globe, including: Douglas Yu from TSMC, Tim Olson from DECA, Steffen Kroehnert from NANIUM, Rolf Aschenbrenner from IZM Fraunhofer, and Steve Bezuk from Qualcomm Technologies, Inc.

1) Best Session Paper
"High-Frequency Analysis of Embedded Microfluidic Cooling Within 3-D ICs Using a TSV Testbed"
Authors: Hanju Oh, Xucheng Zhang, Gary S. May, and Muhannad S. Bakir – Georgia Institute of Technology

2) Best Interactive Presentation Paper
"Constitutive Relations for Finite Element Modeling of SnAgCu in Thermal Cycling – How Wrong We Were!" - Peter Borgesen, Thaer Alghoul, Farhan Batieha, Nardeeka Adams, Saif Khasawneh, Dustin Watson, and Chris Greene – Binghamton University

3) Outstanding Session Paper
"Eternal Packages: Liquid Metal Flip Chip Devices" - Authors: Assane Ndieguene, Pierre Albert, and Julien Sylvestre – Université de Sherbrooke; Clément Fortin and Valérie Oberson – IBM Corporation

4) Outstanding Interactive Presentation Paper
"20" x 20" Panel Size Glass IPD Interposer Manufacturing" - YuHu Chen, ChunHsien Chien, YuChung Hsieh, WeiTi Lin, Wen-Liang Yeh, ChienChou Chen, and TzyyJang Tseng – Unimicron Technology Corp.; Hobie Yune – Qualcomm Technologies, Inc.

5) Intel Best Student Paper
"Non-Linear Finite Element Analysis on Stacked Die Package Subjected to Integrated Vapor-Hygro-Thermal-Mechanical Stress" - J. Wang and S. Park - Binghamton University

6) Texas Instruments Outstanding Student Interactive Presentation Paper Award
"2D Grating Pitch Mapping of a Through Silicon Via (TSV) and Solder Ball Interconnect Region Using Laser Diffraction" T. Houghton, M. Saxon, Z. Song, H. Nguyen, H. Jiang, and H. Yu - Arizona State University

2016 ECTC Best Paper Awards.

Over 250 people attended this panel session, proving the point that Panel-Level Fan-Out packaging is still a very hot topic.

Tuesday at ECTC was also the occasion of the IEEE EPS Heterogeneous Integration Technology Roadmap Workshop. This day long workshop was chaired by William Chen and W. R. Bottoms. This activity is organized under the auspices of the IEEE EP Society, and follows the purpose, process, and format of the ITRS Heterogeneous Integration Roadmap which ended in the spring of 2016. This important workshop, which will be held annually at future ECTC conferences, will be critical to developing a 15 year roadmap for navigating technology challenges, for example the slowing of Moore's law, and market challenges, for example the emergence of the Cloud and the Internet of Things (IoT).

The ECTC Student Reception, sponsored by Texas Instruments, was held on Tuesday at 5 p.m. A steady stream of student attendees took advantage of the opportunity to mingle and network with professionals in the field. Right after this, a General Chair's Reception was given for Speakers and Session Chairs, at the Dolphin Northern Hemisphere room, moved inside due to inclement weather. These receptions provided a great start to the conference, and helped prepare everyone for the following three days filled with technical presentations and networking opportunities.

Tuesday night at 7:30PM the 2017 ECTC Panel session was focused on "Panel Fan-Out Manufacturing: Why, When and How?". The session was organized by Jean Trewhella EPS President/GLOBAL FOUNDRIES and by Young Gon Kim from Integrated Device Technology. Experts assembled to provide their insights included: Douglas Yu of TSMC, Tim Olson of DECA, Steffen Kroehnert, from Nanium Ralf Aschenbrenner from IZM Fraunhofer, and Steve Bezuk from Qualcomm Technologies, Inc. Each panelist gave their perspective on the direction that manufacturing would move for fan-out packages. The panelists all agreed that fan-out packaging would move to the panel level in the near future although there are remaining challenges. A large benefit of the transition from the wafer level to the panel level will be cost reduction. Issues that need to be addressed to accelerate the transition to PLFO include the adoption of standards, design constraints, metrology tools, and yield constraints. The panelists discussed the importance of embedded technologies such as WLFO and PLFO as an important part of heterogeneous integration solutions. Audience participation enhanced the discussion and topics expanded to include the impact of low and high density on the need, difficulty and likelihood of adoption of the larger format.

Each day at ECTC begins with the Speakers Breakfast in which the presenters and session chairs meet and take care of the preparatory work for their respective sessions. The PDC Chair, Kitty Pearsall, provided instructions to the PDC instructors and proctors on Tuesday morning, and Mark Poliks, the Program Chair, hosted these breakfast meetings.

Wednesday marks the start of the technical sessions with six sessions running in parallel, both in the morning and in the afternoon each day. Wednesday morning started with large crowds in numerous sessions including "Fan-Out Packaging Process and Integration", "TSV Process Characterization and Applications", "Emerging Sensors and Microsystems Packaging", and "Advanced Substrates and Integrated Devices". High session attendance was noted throughout the day, with afternoon topics covering "Singulation Process Developments", "Harsh Environment Interconnect Reliability", and Mechanical Modeling and Characterization of Interposers and Interconnections." As last year, all oral session paper ratings were done only through the ECTC mobile app.

The keynote speech at the ECTC luncheon on Wednesday was given by Babak Sabi, Corporate Vice President and Director of Assembly and Test Technology Development, Intel Corporation.

Babak Sabi (left), Intel Corporate VP and Director of Assembly and Test Technology Development receives a plaque as a keynote speaker from Henning Braunisch/Intel, 67th ECTC General Chair.

The Gala Reception was the time for socializing after a day full of technical meetings and brainstorming.

The 67th ECTC had 106 exhibitor booths at the Technology Corner. The YES team was the best dressed.

The 2017 ECTC Executive Committee members from left to right: Sam Karikalan/Broadcom Limited, Vice-General Chair, Christopher Bower/X-Celeprint Inc., Assistant Program Chair, Henning Braunisch/Intel Corporation, General Chair, and Mark Poliks/Binghamton University, Program Chair.

In his inspirational presentation, titled "Advanced Packaging in the New World of Data", Dr. Sabi provided his perspective on the need for heterogeneous on-package integration as the only viable solution for the exponentially increasing demand for system performance in this "Age of Data". He showed how the needs for high interconnect density and bandwidth are driving compact integration of multiple nodes, intellectual property blocks, and functions. His talk was also a call for the community to continue the focus on delivering increasing high density interconnect, power efficient signaling, efficient power delivery, and improved thermal performance, with an eye on implementation of high volume, high yield manufacturing. The audience welcomed the crisp summary of the challenges that lay before us. It is indeed a good time to be a packaging engineer.

Awards for best and outstanding papers from last year's 66th ECTC, both in oral presentation sessions and interactive sessions, were presented by the ECTC 2016 Program Chair, Sam Karikalan, at this luncheon. Also presented was the Intel Best Student Paper Award for ECTC 2016.

The Technology Corner exhibit area was a busy place this year with 106 exhibitors. The exhibits saw a steady stream of attendees, with very busy bursts of activity during the breaks from the technical sessions. The exhibitors hosted a reception on Wednesday evening that provided more opportunities for technical and business exchanges with prospective customers and collaborators. The Interactive Presentation sessions were conveniently located just outside the Technology Corner and had a high number of patrons studying the presented results.

Kitty Pearsall from Boss Precision, Inc., chaired the 3rd EPS/CPMT Women's Panel session titled "Emotional Intelligence (EI)—Link to Successful Leadership". This year, the attendees heard perspectives from distinguished women leaders including: Joanne Martin, JLM Consulting LLC, Rozalia Beica, Dow Corporation, and Tanja Braun from the Fraunhofer Institute for Reliability and Microintegration IZM. The panelists discussed their careers and the importance that emotional intelligence played in their professional lives. They then participated in a Q & A session with the audience, which was followed by an in-room reception where discussions and networking continued.

The Wednesday evening Plenary Session titled "Packaging for Autonomous Vehicle Electronics" was chaired by Luke England from GLOBALFOUNDRIES and included presentations from leading

technology institutes. The speakers included Venky Sundaram, Georgia Institute of Technology, Brent Richardson of Texas Instruments, Frank Bertini of Velodyne, Dongji Xie from Nvidia, and Raj Pendse from Qualcomm Technologies, Inc. The panelists shared many insights on this rapidly evolving business area with the attentive audience.

The Thursday morning sessions were well attended and covered topics ranging from "Warpage, Electro-migration and Mechanical Characterization" to "Flipchip and Embedding in Substrates" to "Materials and Processes for Flexible and Wearable Devices". Thursday afternoon included sessions on "MEMS and Sensor Technologies", "Recent Advances in FOWLP Technology", and "Novel Methods to Assess Reliability".

The IEEE EP Society President, Jean Trewhella/GLOBALFOUNDRIES, presided over the luncheon on Thursday and presented the EPS/CPMT Society Awards. The recipients were honored with a plaque and warm applause from the audience.

The ECTC 2016 Technical Program Committee meeting was held on Thursday at 5:30 p.m. Chris Bower, who will serve as the Program Chair for ECTC 2018, chaired this meeting and presented the statistics of the 67th ECTC and the timeline for the run up to the 68th ECTC that will be held in San Diego next year. The EPS Representative on the ECTC Executive Committee, C. P. Wong, introduced Nancy Stoffel of GE Global Research as the Assistant Program Chair of the 68th ECTC. This meeting also enabled the ECTC technical program subcommittees to get in touch with potential new members of their committees.

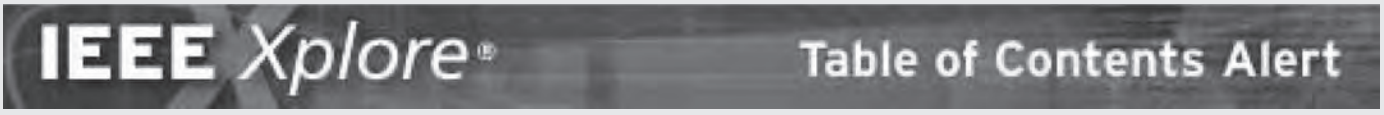
The Gala Reception on Thursday evening was the highlight of the week for the conference attendees, exhibitors, sponsors, and their guests. It was a time to celebrate the success of the ECTC by socializing and enjoying the excellent food and beverages that were supported by the Gala Reception Gold and Silver sponsors.

Following the Gala Reception, the 2017 EPS/CPMT Seminar on "3D Tools, Technologies and Applications" was chaired by Venkatesh Sundaram of the Georgia Institute of Technology and Yasumitsu Orii of Nagase, Japan. At this seminar, Manos Tentzeris of the Georgia Institute of Technology, Humair Mandavia of Zuken SOZO Center, Simon Fried of Nano Dimension, Ltd., and Takeshi Sato, Fuji Machine Mfg. Co., Ltd. each presented their vision of the rapidly evolving field of 3D printing, and its applicability for printed and embedded electronics. We were fortunate to get the perspective of a cutting-edge researcher using additive technologies, an EDA tool developer, as well as two companies developing newer and better tools to enable both prototyping and full high volume production.

For those interested in the latest advances in the packaging field, Friday was not to be missed. The morning sessions ranged from "Advanced Materials for Reliability Improvement" to "Warpage Control and Substrates" to "Characterization and Reliability of Fan-Out & WLP". The afternoon included sessions on "Auto Electronics Packaging and Power Modules", "Waveguide Devices and Chip-to-Fiber Packaging", and "Advanced Bonding and Soldering Technology". At lunch on Friday, everyone had the usual fun at the famous ECTC raffle, where Tom Reynolds, the ECTC Treasurer, kept everyone laughing and longing to hear the numbers on their ticket called.

Overall, the 67th ECTC was a great success in terms of its near record attendance, strong exhibitor presence, record sponsorship, and the large number of high quality technical presentations and submitted abstracts. The ECTC Executive Committee sincerely thanks all the attendees, exhibitors, and conference sponsors for their support. The 68th ECTC will be held at The Sheraton San Diego Hotel & Marina, San Diego, California, USA, May 29–June 1, 2018. Sam Karikalan from Broadcom Limited will be the General Chair of this conference. The Call for Papers and PDC Proposals will be available on www.ectc.net and the abstract submission will close on October 9, 2017. So, get those abstracts ready and submit them as soon as abstract submission opens online.

See you all in California in 2018!



Any technologist – **member or non-member** – is welcome to receive alerts when upcoming issues of our EPS *Transactions* are posted to the IEEE's Xplore database and all the papers are available for downloading. This is a handy way to scan the issue's Table of Contents and quickly learn about novel approaches to packaging, modeling, reliability, materials, assembly and other topics.

The website link is:ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

If you already have an IEEE web account, you may sign in and select those journals you wish to track. If you don't have an account, all it takes is your name and email address! Then simply click the Alert Status box next to the journals you wish to monitor. You will receive an email each quarter when that journal is posted to Xplore.

Similarly, if you prefer to receive information by RSS feed, you may add our journals' feeds to your Reader. You'll get a listing of the papers in that issue, along with full abstracts and a link for downloading the paper. The RSS links are shown on this same web page.

Here are the journals we suggest you select for monitoring:

Transactions on Components, Packaging and Manufacturing Technology
Transactions on Semiconductor Manufacturing

EPTC 2017

19th Electronics Packaging Technology Conference
6th-9th Dec 2017, Grand Copthorne Waterfront Hotel, Singapore

IEEE CPMT Society's Flagship Conference in Asia Pacific Region

CALL FOR PAPERS

ABOUT EPTC

The 19th Electronics Packaging Technology Conference (EPTC 2017) is an International event organized by the IEEE Reliability/EPS/ED Singapore Chapter and sponsored by IEEE EP Society.

EPTC 2017 will feature technical sessions, professional development courses, forums, an exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronics packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world. EPTC is the flagship conference of the IEEE EP Society in Region 10.

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new developments in the following categories:

- **Advanced Packaging:** advanced flip-chip, 2.5D & 3D, PoP, embedded passives & actives on substrates, System in Package, embedded chip packaging technologies, panel level packaging, RF, Microwave & Millimeter-wave, power and Rugged Electronics Packaging etc.
- **TSV/Wafer Level Packaging:** wafer level packaging (Fan In/Fan Out), embedded chip packaging, 2.5D/3D integration, TSV, silicon & glass interposers, RDL, bumping technologies, etc.
- **Interconnection Technologies:** Au/Ag/Cu/Al wire-bond / wedge bond technology, flip-chip & Cu pillar, solder alternatives (ICP, ACP, ACF, NCP, ICA), Cu to Cu, wafer level bonding & die attachment (Pb-free) etc.
- **Emerging Technologies:** packaging technologies for MEMS, biomedical, optoelectronics, internet of things, photovoltaic, printed electronics, wearable electronics, photonics, LED, etc.
- **Materials and Processing:** advanced materials, 3D materials, photoresists, polymer dielectrics, solder materials, die attach, underfill, substrates, leadframes, PCB etc for advanced packaging, and assembly processes using advanced materials, etc.
- **Equipment and Process Automation:** new processes development, equipment automation, equipment hardware development/improvements, data analytics, in-situ metrology, etc.
- **Electrical Simulations & Characterization:** Power plane modeling, signal integrity analysis of package. 2D/2.5D/3D package level high-speed signal design, characterization and test methodologies, etc.
- **Mechanical Modeling & Simulations:** thermo-mechanical, moisture, fracture, fatigue, vibration, shock and drop impact modeling, chip-package interaction, reliability, virtual prototyping, etc.
- **Thermal Characterization & Cooling Solutions:** thermal modeling and simulation, component, system and product level thermal management and characterization.
- **Quality, Reliability & Failure Analysis:** component, board, system and product level reliability assessment, interfacial adhesion, accelerated testing, failure characterization, etc.

Others are also welcomed, e.g. market trends, environmental issues, legislation, patents, education, cost analysis, etc.

IMPORTANT DATES

Online abstract submission start	31st Mar 2017
Closing of abstract submission	Extended 7th July 2017
Notification of acceptance	21st July 2017
Submission of manuscript	15th September 2017

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited which describe original and unpublished work. The abstract should be at least 500-750 words and must clearly state the purpose, methodology, results (including data, figures, graphs and photographs) and conclusions of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well. Authors can choose between oral or interactive presentation but the decision of the Organising Committee will be final. Only accepted papers which are presented (oral & interactive) in the conference will be published in the conference proceedings and in IEEE Xplore.

Authors must designate two appropriate categories (found under CONFERENCE TOPICS) for abstract review. All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by 7Th July 2017. Authors must include their affiliation, mailing address, telephone, and email address. Authors will be notified of paper acceptance and publication instructions by 21st July 2017. The final manuscript for publication in the conference proceedings and the presenter's registration are due on 15th September 2017.

OUTSTANDING TECHNICAL PAPERS

Author(s) of Best Technical Paper (oral/interactive), Outstanding Technical Paper (oral) and Best Student Paper will receive an award at the next conference. More details can be found at http://www.eptc-ieee.net.

CALL FOR PROFESSIONAL DEVELOPMENT COURSES

The conference program includes professional development courses (PDCs) which will be conducted by leading experts in the field. Details, when available, will be updated in the conference website. Proposals for PDCs can be submitted to pdc@eptc-ieee.net as soon as possible.

CALL FOR EXHIBITION/SPONSORSHIP PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment, software and service providers of microelectronics and electronic assembly industries, will be held during the conference. Potential exhibitors and sponsors may email exhibition@eptc-ieee.net and sponsorship@eptc-ieee.net for details.

EPTC 2017: website: **http://www.eptc-ieee.net** Email: secretariat@eptc-ieee.net

Join us on: **Linkedin [EPTC OC]** Follow us on: **Twitter [EPTC (@EPTCOC)]**

Organized by IEEE
IEEE Reliability/CPMT/ED Singapore Chapter

General Chair	Technical Chair	Program Chair
Zhang Xueren	Vempati Srinivasa Rao	Jung Boo Yang
Xilinx	IME	Globalfoundries
generalchair@eptc-ieee.net	techchair@eptc-ieee.net	program@eptc-ieee.net

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PROGRAM HIGHLIGHTS (SUBJECT TO CHANGE)

1. PROFESSIONAL DEVELOPMENT COURSES

- MEMS Fabrication and Packaging, Dr. Liu Aiqun, School of Electrical & Electronic Engineering College of Engineering Nanyang technological university, Singapore
- Electronic Packaging for 5G Microwave and Millimeter Wave Systems, Dr. Rick Sturdivant, Department of Engineering and Computer Science & Department of Engineering and Computer Science, Azusa Pacific University, USA
- Fan-Out Wafer-Level Packaging and 3D Packaging, Dr. John H Lau, ASM, Hong Kong
- small volume interconnect reliability and failure mechanisms for power/automotive package, Dr. Mervi Paulasto-Kröckel, Department of Electrical Engineering and Automation, Aalto University, Finland
- Advanced LED packaging technology and reliability, Dr. Shi-Wei Ricky Lee, LFASME, FIEEE, FInstP, LFIMAPS, Chair Professor of Mechanical & Aerospace Engineering, Hong Kong University of Science & Technology, Hong Kong

2. KEYNOTE SPEAKERS

- Dr. Wai Kooi Wong, Vice President, Quality And Reliability, Xilinx, Title TBC
- Dr. Rajendra Pendse, Vice President, R&D, Qualcomm, Title TBC

3. INVITED SPEAKERS

- Dr. Junsu Lee, Senior Packaging Scientist, Tyndall Research Institute, Title TBC
- Dr Napetschnig, Staff Engineer, Infineon, Title TBC

EPTC 2017: website: **http://www.eptc-ieee.net** Email: secretariat@eptc-ieee.net
Join us on: **Linkedin [EPTC OC]** Follow us on: **Twitter [EPTC (@EPTCOC)]**

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DRESDEN 2018

7th ELECTRONICS SYSTEM-INTEGRATION TECHNOLOGY CONFERENCE

September 18-20, 2018

CALL FOR PAPERS ANNOUNCEMENT

THE SINGLE LARGEST SEMICONDUCTOR PACKAGING CONFERENCE IN EUROPE

It is our pleasure to announce the 7th ESTC Conference, the premier European scientific conference event in the field of microelectronics packaging and system integration. The conference will be held from 18th to 20th of September, 2018, at the Westin Bellevue Hotel in Dresden, Germany. This international event brings together both academics as well as the industry leaders to present and discuss state-of-the-art and the future trends in packaging and integration technologies. ESTC provides a perfect opportunity to learn about the latest developments in those fields. Save the date right now! This major event only takes place once every 2 years. ESTC is supported by IEEE-EPS in association with IMAPS-Europe. The 2018 conference continues the line of prestigious events since the birth of ESTC 2006 in Dresden, followed by Greenwich, Berlin, Amsterdam, Helsinki and Grenoble every even year.

Read more about the whole history at www.estc-conference.net

CALL FOR PAPERS

ESTC 2018 seeks original papers describing research and innovations in all areas of electronic packaging and system integration. You are invited to submit abstracts that provide non-commercial information of new developments and knowledge in areas like:

- Advanced packaging, 3D integration, embedded structures, wafer level packaging, TSVs, TEVs…
- Materials for interconnects and packaging, piezoelectric, dielectric and memory materials, nanomaterials…
- Optoelectronic systems packaging, fiber optical interconnects, optical sensors, LEDs and other photonic devices…
- Assembly and manufacturing technologies, wafer level processing…
- MEMS/NEMS and sensors packaging, bonding technologies, wafer bonding, micro-bonding…
- Design tools and modeling, thermal, mechanical and electrical modeling, signal and power integrity
- Power electronic systems packaging, power embedding, wide bandgap power semiconductor devices…
- Advanced technologies for emerging systems, allotropes of carbon, nano packaging, bio-electronics…
- Reliability of electronic devices and systems, characterization and test, failure diagnostic …
- Flexible printed and hybrid electronics, printed/jetted conductors, paper electronics, energy storage…

ABSTRACT SUBMISSION

You are invited to submit a 300 - 500 word abstract that describes the scope, content and key points of your proposed paper. Abstracts must include results and graphics. The official language of all presentations is English. Please visit www.estc-conference.net to find more information and to upload your abstract. Submission of abstracts will be open from December 1st 2017 and abstracts are due **February 15th 2018**. All abstracts must be submitted electronically at the conference website. All submitted abstracts will be reviewed by the committee to ensure high-quality of the conference. Authors will be notified of paper acceptance with instructions for publication by March, 30th 2018. If you have any questions, please contact: Karlheinz Bock, the General Chair of the 7th ESTC, via email karlheinz.bock@tu-dresden.de.

PUBLICATION OF PAPERS

All oral and poster presentation papers will be included in the conference proceedings and made available at the IEEE Xplore Digital Library (ieeexplore.ieee.org). In order to be included in IEEE Xplore, the paper must be original and not previously published, and avoid inclusion of commercial content.

BEST PAPER AWARD

The ESTC Technical Committee will select the best paper presentation. The author(s) will receive a personalized ESTC award that comes with a 1.000 € prize money. The best poster paper will also be selected and the author(s) will receive a personalized ESTC award that comes with a 1.000 € prize money, too.

PROFESSIONAL DEVELOPMENT COURSES

In addition to abstracts for paper presentations, we call proposals from individuals interested in teaching Professional Development Courses (duration 4 hours) about the topics described in the Call for Papers. Up to four Professional Development Courses will be selected from the received proposals for Tuesday morning (September 18th, 2018) of the conference. Each selected course will be given an honorarium of 750 € if a minimum number of participants will sign in for the course. In addition, instructors of the selected courses will be offered the speaker discount rate for the conference. A 300 to 500 words proposal containing description of course objectives, course outline and who should attend, should be submitted to klaus-juergen.wolter@tu-dresden.de by February 15th, 2018.

IMPORTANT DATES

- **Website open for abstract submission: December 1st, 2017**
- **Abstract submission deadline: February 15th, 2018**
- **Notification of acceptance: March 30th, 2018**

General Chair:
Karlheinz Bock
Technische Universität Dresden, Germany

Executive Chair:
Thomas Zerna
Technische Universität Dresden, Germany

Technical Program Chair:
Steffen Kröhnert
Nanium S.A., Portugal

The 29th Annual Electronics Packaging Symposium (EPS) is the premier electronics manufacturing conference of the Northeast, bringing together the best and brightest in the international electronics packaging industry. The 2017 Symposium will be held at GE Global Research in Niskayuna, New York, September 19-20, 2017 and will feature over 40 technical presentations, EPS/IEEE workshop, student poster session and exhibits. Topics for symposium include:

Heterogeneous Integration
Electronic Materials
Thermal Challenges
2.5/3D Packaging
Power Electronics
Flexible & Additive Electronics
Sensors, Embedded Electronics & IoT
Automotive & Harsh Environments
Photonics & MEMS
Materials for Energy Storage

https://www.binghamton.edu/ieec/symposium/index.html

Summary of 37th IEMT & 18th EMAP 2016 Conference, Georgetown, Penang

(Compiled by Guat Li Chew, Dr. Tze Yang Hin, Ir. Dr. Wong Yew Hoong & Dr. Choong Kooi Chee)

Voted 2nd Top Tourist destination for 2017 by CNN, Penang was the Asian center of the packaging universe in the month of September 2016. Its multicultural and picturesque historical setting coupled with its reputation as having Asia's best street food proved to be an added bonus for conference participants and organizing committee alike. Amongst the clatter of Asam Laksa bowls, Nasi Kandar plates and abundant clinking of Teh Tarik glasses, rife conversations were on-going about the future of the globally connected world via numerous type devices in terms of security and possibilities. Packaging these devices at an affordable cost is a major challenge facing members of the Electronics Packaging (CPMT) society.

Since 2006, the IEEE EPS Malaysia chapter was the main advocate of International Electronics Manufacturing Technology (IEMT) conferences, in conjunction with co-sponsor EPS Santa Clara. The organizing committee members were volunteers from local multinational semiconductor companies such as Intel Technology, Infineon, ON Semiconductor, Carsem, Lumileds, Unisem, NXP, Peters, Indium and semi-governmental body

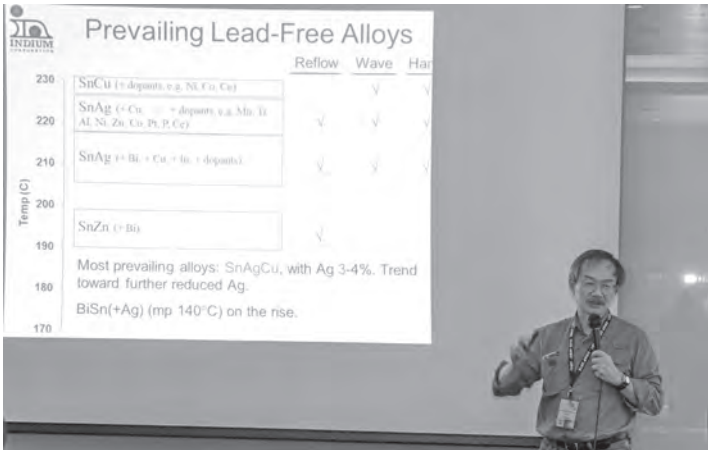
The IEMT2016 organizing committee with their charismatic conference chair in the back row.

CREST. The local universities members in this year's organizing committee were from Universiti Kebangsaan Malaysia (UKM), Universiti Teknologi Malaysia (UTM) and Universiti Sains Malaysia (USM). This year, the 37th International Electronics Manufacturing Technology Conference was jointly organized in concurrent with the 18th Electronic Materials and Packaging (EMAP) Conference on the beautiful city of Penang, a UESCO World Heritage site. G-Hotel was the elegant sea-front venue of the combined conference.

The conference was proud to have invited industry-leaders to share the latest industry trend and technology in its 5 short courses, 8 keynotes and 16 invited papers. There were 80 abstracts accepted for oral papers as well as interactive poster papers. The conference had always attracted >60% of the total abstracts from the industry and 30–40% of those were from abroad. This has served well for the conference as a platform for technology and knowledge exchanges within the electronic manufacturing community. Back in IEMT2014, the focus was on Internet-of-Things (IoT) and its application. This year conference's theme was "Packaging the IoT", an extension of the 2014 topic. This round, the focus was more skewed to the fundamental technologies that drive the development and enabling of IoT hierarchy. The conference provided insights into core technologies such as wire bonding material and processes, chip-to-package interconnection, solder materials and other materials development trends, and new reliability requirements. The new entrant to IEMT-EMAP conference series this year was the inclusion of LED packaging and the optical characteristics. All in all, this was the first time that the Conference had more than 450 participants, a major achievement in terms of attendance. Kudos to the core organizing team, especially the Publicity and Publication Team! Furthermore, there was a total of 21 table top exhibits and a record-breaking sponsorship this year—Fabulous job by the Sponsorship & Exhibit Team. Logistics and management of last minute changes, walk-ins, change of players were handled magnificently by the Secretariat team headed by Wee Teck and Hafiza! Not forgetting the excellent Program Book designed by the Program Chairs. Under the strong leadership of Dr Hin, all these various teams coalesced to handle a much larger crowd than expected.

The three-day event started with four short-course workshops for 144 people on the initial day. These courses were given by renowned technical experts invited from overseas. The courses were *Chip to Package Interconnect Technology: Fundamentals and Future Trend* by Mr. Charlie Lu Tsung-Hsing (Taiwan Printed Circuit Association), *Fan-Out Wafer Level Packaging (FO-WLP)—Innovative and Novel Solutions of Advanced Packaging* by Dr. Seung Wook Yoon (Director of Products & Technology Marketing STATS ChipPac-JCET, Singapore), *Copper Ball Bonding Materials, Intermetallics & Reliability* by Dr. Christopher Breach (ProMat Consultants, Singapore), *Achieving High Reliability for Lead-Free Solder Joints* by Dr. Ning-Cheng Lee (Vice President of Technology, Indium Corporation) and *Trends in Material Development—Upcoming Requirements concerning Reliability* by Dr. Klaus Mueller (Senior Principal Infineon Germany).

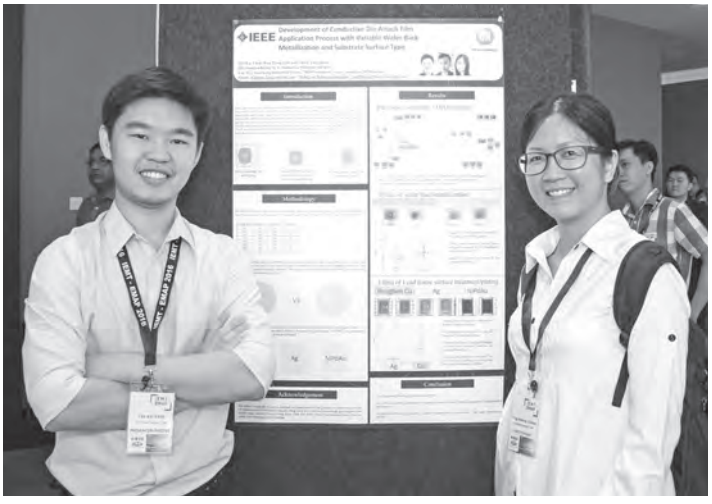
The remaining two days comprised keynote speeches, invited talks, paper and poster presentation sessions from leaders of the industry. The conference was opened with a short address given by the IEEE EPS President representative Dr. William T. Chen (ASE Group USA) who spoke on *Heterogeneous Integration, expounding on the Roadmap to the Brave New Interconnected World*. It was then followed by a series of excellent keynotes, namely the *Development in Internet of Things (IoT) and Opportunities for "Packaging the Iot"* by none other than Mr. Eric Chan (Intel Corporation Malaysia),



1st Day Short-course instructors and students listening attentively to the instructors.

(From left to right) Opening speech by Dr. Hin Tze Yang (Conference Chair), captive audience in Main Conference Hall.

Small sample of the myriad of Exhibitors displaying their products and services, including QDOS, IEEE, Atotech, IEEE Student Body, TechSearch International, Loctite Semiconductor Technologies.



Poster Display showcasing "Development of Conductive Die Attach Film Application Process with Variable Wafer Back Metallization and Substrate Surface Type" by Tan Kai Chat et al from ON Semi-conductor Malaysia.

Panel Level Embedding for Power and Sensor Applications by Dr. Rolf Aschenbrenner (Fraunhofer Institute for Reliability, Micro-integration Berlin (IZM), Germany), *Anisotropic Conductive Films(ACFs): Interconnection Technology for Wearable Electronics Applications* by Professor Kyung Wook Paik (KAIST, Korea) and *The Future of Power Device Packaging: Materials and Assembly Processes* by Dr. Andrew Christopher Mackie (Indium Corp, USA) on Day 2 of the Conference. Final day of the conference witnessed additional exceptional keynotes such as *Material Challenges for Optoelectronic Packages in Lighting Applications* by Dr. David Lacey (R&D Director of OSRAM Opto Semiconductors Malaysia), *Technological Challenges and Market Trends for Power Packaging* by Dr. Pierric Gueguen (Yole Dévelopment, France) and the closing keynote address *Packaging and Integration Technologies for the Era of Internet of Things* by Professor Ricky Lee Shi-Wei (HKUST Hong Kong). Dr. Lacey's keynote was especially interesting to the participants coming from the LED industry as it was clear, simple and the futuristic work displayed was very impressive.

The conference's four-track oral presentation sessions consisted of 64 selected papers and 16 invited papers from prominent guest speakers. Eighteen posters were presented by industry technologists at the main hall along with the exhibitions. The conference provided an opportunity for the participants to mingle and build network in various areas of electronic packaging.

IEMT has always been the battle ground for its prestigious awards. There are 3 Award categories—Best Industry Paper Awards, Best Student Paper Awards and Best Poster Paper Awards. The judges for these awards were experts in the areas of electronic packaging—Dr. Rolf Aschenbrenner, Dr. Klaus Mueller, Mr. William Chen and Dr. Sung Yi. The Best Industry Paper Award went to K.H. Loh et al of Carsem for "*Qualification and Application of Pressure-less Sinter Silver Epoxy"* with the runner up being Min Fee Tai et al from Atotech and UTeM with their submission, "*EMI Shielding Performance by Metal Plating on Mold Compound"*. The Best Student Award went to Robin Ong & Kuan Yew Cheong from USM for their work on "*Non-Destructive Electrical Test Detection On Copper Wire Micro Crack Weld Defect In Semiconductor"* with the Merit Award going to Nadhrah Murad et al for their submission

Awards Judges and Winners of IEMT2016 (left to right): Dr. CK Chee, KH Law & Dr. Klaus Mueller (Best Industry Paper Category); Dr. CK Chee, Dr. Rolf Aschenbrenner & Robin Ong (Best Student Paper Category); Dr. CK Chee, Prof. Ricky Lee, Chong Seng Foo & Jui Ang Tan (Best Poster Category).

Group photo of Invited Guests and Organising committee.

(Top to bottom right) Panaromic view from 59Sixty Restaurant, Malaysian bamboo Pole Dancing, Chinese Lion Dance Performance.

"*Effect of Sintering Parameters on Properties of Sn-4.0Ag-0.5Cu-1.0Ni Solder Alloy"*. The Best Poster was awarded to Chong Seng Foo & Jui Ang Tan from Intel Malaysia for their poster *"Cost Savings Through Innovative and LEAN Engineering Approach for Wireless Modules"*. The runner-up Poster Award was bestowed to Cheng Guan Ong et al from Infineon and UTem for their poster entitled "*Effect of Cu Based Complexes on EFTECH64 and C194 Cu Alloy"*. Congratulations to all the award winners!

No conference was complete without a Gala Dinner. The participants were treated to a sumptuous Buffet Seafood dinner at the 59Sixty situated at the pinnacle of Komtar, the tallest building in Penang. The Penang Heritage scenery was an eye-opener with view of the city layout, the old heritage buildings and the winding quaint Penang lanes. During the dinner, the participants were entertained with a Lion Dance, which was a challenge, given the space constraints, and cultural dance show from the diverse tribes and racial mix. A few of the participants were invited on stage to dance the bamboo dance where the participants had to jump between bamboo poles and not get entangled in the poles. Dr. Chee led our visitor volunteers in demonstrating this—the Malaysian equivalent of pole dancing! Bravo Dr. Chee! Many thanks to all our participants and visitors who made this event a major success!! We'll see you all in the 2018 IEMT Conference!

Paper Submission

The IMPACT 2017 conference will be held in conjunction with TPCA SHOW 2017 on Oct. 25th–27th at Taipei Nangang Exhibition Center. The IMPACT Conference which is organized by IEEE CPMT-Taipei, iMAPS-Taiwan, ITRI and TPCA is the largest gathering of IC packaging and PCB professionals in Taiwan. Looking farther forward to future technology trends, the Intelligent Things fall into several areas: smart application, robot, drones, autonomous vehicles, artificial intelligence and IoT devices. Each application influences a large impact in our daily life. For grasping the latest trend, the IMPACT highlights the theme **"IMPACT on Intelligent Everything"** and will arrange plenary speeches, special sessions, invited talks, industrial sessions, posters and outstanding paper presentations. Furthermore, IMPACT Conference keeps collaborating with international organizations such as ICEP from Japan and iNEMI from U.S.A. We hope this conference will become a remarkable platform to show your technology research and capability.

Important Dates

June 15, 2017
- Abstract Submission Deadline
- 400–500 words

Submit on-line www.impact.org.tw

July 15, 2017
- Abstract Acceptance Notification
- Notice sent via email

August 15, 2017
- Advance Program Online
- Advanced program announcement

August 25, 2017
- Full Paper Submission (Camera-ready Version)
- 4 pages including figures and tables

Submit on-line through conference website and copyright forms due

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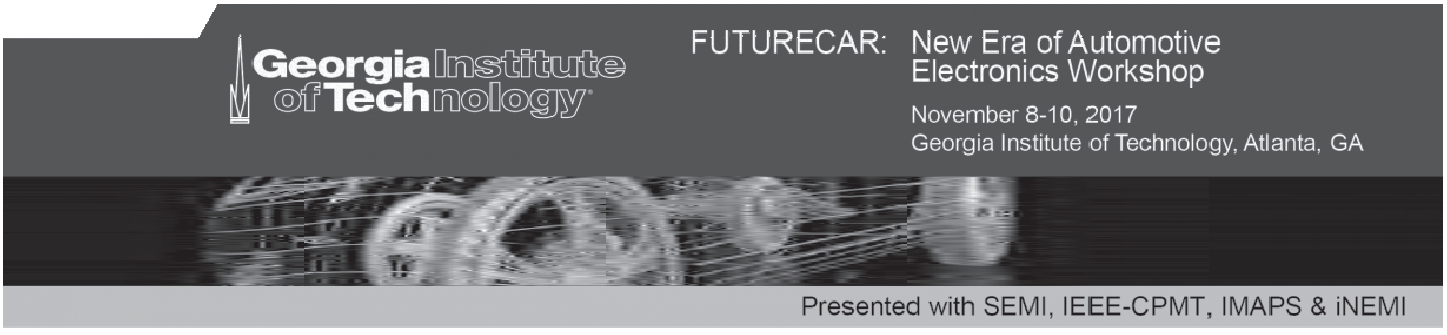
FUTURECAR 2017



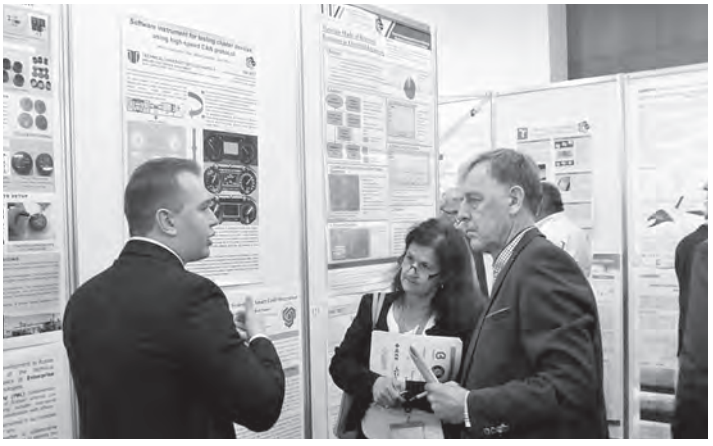
FUTURECAR 2017 – November 8-10, 2017 – Atlanta, GA

Future car electronics such as autonomous driving, in-car smartphone-like infotainment, privacy and security, and all-electric cars, present unparalelled research, development, manufacturing, education and marketing opportunities. They require new paradigms in devices and packaging particularly in materials,tools,processes, substrates,packages, components and integrated functions in R&D and in manufacturing. Georgia Tech and Semi see unprecedented technical challenges and opportunities in electrical, mechanical and thermal designs, and new digital, RF, radar, LiDAR, camera, millimeter wave, high-power and high-temp technologies.

http://prc.gatech.edu/FUTURECAR

ISSE 2017


40th International Spring Seminar on Electronics Technology - ISSE 2017
„High-Tech Electronics for a Better Tomorrow - Theoretical and Practical Aspects"
May 10 – 14, 2017, Sofia, Bulgaria



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For details go to: www.cpmt.ieee.org

Name: 2017 IMAPS Nordic Conference on Microelectronics Packaging (NordPac)
Location: Gothenburg, Sweden
Dates: Jun 18, 2017–Jun 20, 2017

Name: 2017 18th International Conference on Electronic Packaging Technology (ICEPT)
Location: Harbin, China
Dates: Aug 16, 2017–Aug 19, 2017

Name: 2017 39th Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)
Location: Tucson, AZ, USA
Dates: Sep 10, 2017–Sep 14, 2017

Name: 2017 IEEE Holm Conference on Electrical Contacts
Location: Denver, CO USA
Dates: Sep 10, 2017–Sep 13, 2017

Name: 2017 23rd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)
Location: Amsterdam, Netherlands
Dates: Sep 27, 2017–Sep 29, 2017

Name: 2017 12th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)
Location: Taipei, Taiwan
Dates: Oct 25, 2017–Oct 27, 2017

Name: 2017 IEEE CPMT Symposium Japan (ICSJ)
Location: Kyoto, Japan
Dates: Nov 20, 2017–Nov 22, 2017

Name: 2017 IEEE 19th Electronics Packaging Technology Conference (EPTC)
Location: Singapore
Dates: Dec 6, 2017–Dec 9, 2017

Name: 2017 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)
Location: Hangzhou, China
Dates: Dec 14, 2017–Dec 16, 2017

Name: 2018 IEEE 68th Electronic Components and Technologies Conference (ECTC)
Location: San Diego, CA USA
Dates: May 29, 2018–Jun 1, 2018

Name: 2018 7th Electronic System-Integration Technology Conference (ESTC)
Location: Dresden, Germany
Dates: Sep 18, 2018–Sep 21, 2018

Name: 2018 IEEE Holm Conference on Electrical Contacts
Location: Albuquerque, NM, USA
Dates: Oct 14, 2018–Oct 18, 2018

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6 - 10 November 2017
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- **IEEE International Conference on Rebooting Computing (ICRC)** – 8-9 November 2017 – 2nd annual event to discover and foster novel methodologies to reinvent computing technology, including new materials and physics, devices and circuits, system and network architectures, and algorithms and software
- **Industry Summit on the Future of Computing** - 10 November 2017 – A new one-day summit convening great thinkers around the discussion of what we should expect as we enter a new era of computing that is currently un-imaginable. Keynote speakers include:
    - Bernie Meyerson, Chief Innovation Officer, IBM
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    - Dan Hutcheson, CEO and Chairman, VLSIresearch inc.

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Location

The Ritz-Carlton Hotel
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Registration

Register by 29 September 2017 to save. Discounts available for IEEE members and students.

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For more information on 2017 IEEE Rebooting Computing Week, contact Terence Martinez at t.c.martinez@ieee.org.

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2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

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