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Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Chris Bailey
University of Greenwich
London, UK

Summer Newsletter

First and foremost, I would like to thank all our members for your continued support of EPS. The Covid-19 pandemic has brought forward many challenges for all of us. For the society, our most important priority has been the safety and well-being of our members, staff, and volunteers. This has meant that many of our upcoming conferences have moved to an online platform to continue to serve our growing community of electronics packaging engineers.

As I write this column, I am preparing for my attendance at ECTC, our flagship conference in North America. This unique online event, which will be available throughout June, provides an excellent educational opportunity for our members and community. I am delighted to see the innovative ways our conference organizers continue to serve our members and community. For example, ITherm will take place online in July with an exciting program of live and on-demand presentations. ICEPT will take place as a physical event in China in August. And I am looking forward to registering for our European (ESTC) and Asia (EPTC) flagship conferences, which will take place in September and December.

This edition of the newsletter acknowledges the recipients for the 2020 EPS awards. On behalf of the society, I send my congratulations to the EPS award winners and thank them for their outstanding contributions to our society and community.

EPS is strengthening its global reach through the formation of new chapters and student-branch chapters. I am delighted to welcome to the EPS community, the Hudson Valley chapter, and the following student-brach chapters: Fudan University, Michigan State University, SUNY at Binghampton, Florida International University, and the University of Florida.

The EPS technical committees (TC's) and the Technical Working Groups (TWG's) on the Heterogeneous Integration Roadmap continue to take forward the society's exciting activities related to technology. In this newsletter, the Nanotechnology TC presents its activities within EPS and the IEEE Nanotechnology Council and details the contributions that Nanopackaging is making to packaging—from areas such as power delivery to flexible electronics.

Recently the Emerging Technologies TC organized the Future Packaging Vision contest, which provides a forum for young professionals to present their exciting ideas for future packaging technologies. This year we had a large number of very impressive entries, covering technical areas from 3D staking to foldable and biocompatible electronics. My thanks to all the young professionals who took part in this contest.

The Heterogeneous Integration Roadmap goes from strength to strength. The 2019 edition of the roadmap has received 20,000+ downloads to date—an outstanding achievement. This year we will see the second edition of the roadmap, and over the summer, EPS is hosting a series of HIR webinars. Details for our webinars are available on the EPS website. Note that attendance at these webinars contributes to the professional development hours required for a member to receive the EPS certificate.

Finally, I would like to state how proud I am of all the work that our volunteers and staff have been doing in response to the uniquely challenging circumstances we have faced. My sincere thanks to all of them for their efforts, dedication, and commitments to our society and community.

Enjoy this edition of the newsletter, and remember that the presentations at ECTC and ITherm will be available throughout June and July, respectively.

Have a good summer break, and please stay safe and well.

Chris Bailey

NEWSLETTER SUBMISSION DEADLINES

1 December 2020 for Winter issue 2021

15 June 2021 for Summer issue 2021

Submit all material to d.manning@ieee.org

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2022 Term End: Regions 1-6, 7, 9—Rozalia Beica, Kitty Pearsall, Subramanian S. Iyer, Region 8—Tanja Braun, Karlheinz Bock, Region 10—Gu-Sung Kim

Publications

Transactions on Components, Packaging and Manufacturing Technology

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3D/TSV:
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Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

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Circulate your printed or PDF copy of this NEWSLETTER to co-workers.

SFI Logo

Mitsumasa Koyanagi and Peter Ramm Receive the 2020 IEEE Electronics Packaging Award

Mitsumasa Koyanagi
Senior Research Fellow Tohoku University Sendai, Miyagi, Japan

Peter Ramm
Head of Strategic Projects
Fraunhofer EMFT, Bavaria, Germany

"For pioneering contributions leading to the commercialization of 3D wafer and die level stacking packaging."

The IEEE Electronics Packaging Award, sponsored by the IEEE Electronics Packaging Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical com-munity and the profession, benefit to society, and the quality of the nomination.

Mitsumasa Koyanagi's and Peter Ramm's efforts in developing, demonstrating, and commercializing 3D integrated circuit (3DIC) integration processes have played a key role in enabling ever-smaller yet more-powerful devices especially important to mobile communications. 3D integration and packaging involves stacking silicon wafers and interconnecting them vertically so that they behave as a single device, which achieves performance at reduced power and with a smaller footprint than conventional 2D processes. Koyanagi succeeded in fabricating 3D stacked image sensor, 3D stacked memory, and 3D stacked microprocessor test chips using through-silicon vias (TSVs) for the first time. He also demonstrated a four-layer stacked image sensor with quarter video graphics array resolution, a four-layer stacked multicore processor, and a four-layer stacked heterogeneous image sensor with extremely high frame rate. Ramm developed and patented 3D integration approaches with particular focus on die-to-wafer stacking, using low-temperature bonding and vertical integration of IC devices with TSVs, and demonstrated a complete industrial 3DIC integration process. He also published results on key processes such as 3D metallization including robust IMC interconnections and on advanced sensor applications of 3D heterogeneous integration.

An IEEE Life Fellow, Koyanagi is a Senior Research Fellow at Tohoku University, Sendai, Miyagi, Japan.

An IEEE Senior Member, Ramm is the head of Strategic Projects at Fraunhofer EMFT, Munich, Bavaria, Germany.

The 2020 Electronic Packaging Award will be presented at the EPS Luncheon held at the 71st Electronic Components and Technology Conference (ECTC), June 2021, in San Diego, California.

Mitsumasa Koyanagi and Peter Ramm join the recent past recipients of this Award, including Ephraim Suhir (2019), William Chen (2018), Paul Ho and King-Ning Tu (2017), Michael Pecht (2016), and Nasser Bozorg-Grayeli (2015), in receiving this Award.

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www. ieee.org/awards

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2020 IEEE Electronics Packaging Society Award Recipients

Mostafa Aghazadeh
Intel, USA

2020 IEEE EPS Electronics Manufacturing Technology Award
For Sustained Excellence in leading the world's largest Assembly Development Effort to deliver state of the art advanced multi-chip packaging technologies.

Kuo-Ning Chiang
National Tsing Hua University, Taiwan

2020 IEEE EPS Outstanding Sustained Technical Contribution Award
For his leadership, sustained and outstanding contributions to the design-on-simulation technology, AI assisted design and reliability assessment of advanced packaging.

Bing Dang
IBM, USA

2020 IEEE EPS Exceptional Technical Achievement Award
For contributions to the research and development of 2.5D and 3D system integration, interconnect technologies, and material processes.

Katherine (Kitty) Pearsall
Boss Precision, USA

2020 IEEE EPS David Feldman Outstanding Contribution Award
For outstanding service and sustained leadership to the EP Society through value added improvements in the areas of Awards, Education, Chapters, PDC courses, and professional development.

Yew Hoong Wong
University of Malaya, Malaysia

2020 IEEE EPS Outstanding Young Engineer Award
For his contributions to the field of electronic packaging materials and semiconductor fabrication technologies through novel material and process development, as well as continuous service to EPS.

Ziyin Lin
Intel, USA

2020 IEEE EPS Outstanding Young Engineer Award
For outstanding contributions to the development of encapsulation materials and process for advanced flip chip packaging and heterogeneous integration.

Zhuo Li
Fudan University, China

2020 IEEE EPS Outstanding Young Engineer Award
For her outstanding contribution to the materials and process development in the area of flexible and hybrid electronics and the service to the EPS and WIE society.

Seungbae Park
State University of New York at Binghamton, USA

2020 IEEE EPS Regional Contributions Award—Region 1–7 & 9 (Americas)
For outstanding contributions to promote Electronics Packaging Symposium, and unique Industry – Academia Consortium for Smart Electronics Manufacturing research & education into Industry 4.0 initiatives.

Thomas Zerna
TU Dresden, Germany

2020 IEEE EPS Regional Contributions Award—Region 8 (Europe, Middle East, Africa)
For his commitment and role in establishing the ESTC conference, and for his contributions to the EPS Germany Chapter.

Kishio Yokouchi
Jisso-Interconnect Solution Laboratory, Japan

2020 IEEE EPS Regional Contributions Award—Region 10 (Asia and Pacific)
For outstanding contributions to the EPS Region 10, through leading the EPS Japan chapter and chairing the EPS seminar in ECTC for 11 years.

Siddharth Ravichandran
Georgia Institute of Technology, USA

2020 IEEE EPS PhD Fellowship
For recognition of contributions to the development of 2.5D and 3D Glass Packages for Heterogeneous Integration in High-Performance Computing.

IEEE EPS TC Emerging Technologies NEWS

The Emerging Technologies technical committee of the Electronics Packaging Society EPS addresses packaging issues of new and novel technology concepts, which target to advance and sometimes to revolutionize applications in general. This committee places an international focus on the development, characterization, and commercial support for electronics packaging, assembly, and test infrastructure for systems integration. The focus is on key application areas and new emerging technologies such as, fluidics, bio and medical, optics, automotive, harsh environment and military systems, telecommunications and highest frequency, remotely operated, swarm based, opto-electrically heterointegrated, additively manufactured or 3D printed, new materials based and many more. A further topic of high interest is to prepare for the future together with our young members of the electronics packaging community and to involve them as early as possible into the active community work at EPS.

IEEE EPS 2020 Future Packaging Vision Contest
Therefore the president of the IEEE Electronic Packaging Society EPS and the technical chair of emerging technologies have launched the Future Packaging Vision Contest FPVC in 2019 supporting young engineering professionals in industry and academia. FPVC offers them a high-visibility platform, within EPS and at the Electronic Components and Technology Conference, in order to present their visions of the future in their own style and mode of communication.

Given the growing centrality of Packaging to electronic product development and in order to best serve the wider IEEE community, we are very keen to showcase electronics packaging visions and reachout to as many interested young professionals as possible. IEEE EPS very much believes that we need to more actively engage young professionals in the activities of our Society. We are endeavoring to provide them with opportunities to impact the path and future of Electronic Packaging and to prepare them for future leadership roles. We believe that this FPVC can help us to better involve our young colleagues, so that we can learn about their thinking, insights, and priorities, as well as their modes of networking and communication.

This year the FPVC invited more than 100 student authors with accepted papers at ECTC 2020 to join the FPVC and to submit their future packaging visions.

The FPV Award is presented to an individual or a team of not more than three student authors.

The FPV Award Prize: In case of qualified submissions: Up to three FPV Awards will be provided to an individual or team of no more than three: 1st US$1,000; 2nd US$600; 3rd US$300

Student authors have been invited to provide the more generic description of their research field related to their work published in their ECTC 2020 paper and in relation to the IEEE EPS Heterogeneous Integration Roadmap HIR.

The expert reviewer board consisting of representatives of the technical committees of IEEE EPS and ECTC has selected the 6 best future packaging visions out of the in total 15 high quality submissions. The best 3 submissions are awarded with a financial gift of the EPS President and their visions will be published on the EPS web-site. We are very glad to announce the winners of the IEEE EPS Future Packaging Vision Contest 2020 and we cordially invite you to join us in congratulating our six finalists and our three Award winners.

1st EPS FPV 2020 AWARD and US$ 1000 receives **Arsalan Alam, Goutham Ezhilarasu, Randall Irwin,** Samueli School of Engineering, University of California, Los Angeles, CA, USA, for the future packaging vision—**FlexTrateTM: The Future of Flexible Packaging**

This packaging vision covers the work completed on the FOWLP-based flexible packaging platform FlexTrateTM and the vision for the future of flexible packaging with this platform.

FlexTrateTM promises to be the first flexible and biocompatible platform using FOWLP allowing heterogeneous integration without die bonding. The FlexTrateTM platform is practically foldable, enabling form-free electronics. Adaptive patterning eliminates the die shift problem associated with FOWLP, enabling extremely high-density interconnect pitch (<10 μm). The improved thermal conductivity of PDMS will enable a heat dissipation solution for high performance systems. FlexTrateTM will allow development of next generation high-performance flexible applications for example: Ultimate human machine interface platform with AI computing and Form-Free Electronics

2nd EPS FPV 2020 AWARD and US$ 600 receives **SivaChandra Jangam, Zhe Wan, and Niloofar Sharookzadeh**, Sameuli School of Engineering, University of California, Los Angeles, for the future packaging vision—**Packaging for Ultra-Large Scale Cognitive Systems**

The scaling of cognitive systems is limited by interconnect density in packages today. Silicon Interconnect Fabric is a highly scalable, package-less, fine-pitch (<10 μm), heterogeneous integration platform to interconnect massive systems on wafers. The closely-packed dielet assembly helps achieve high bandwidth (>1Tbps/mm) at low latency (<30ps) and power (<0.2pJ/b). Therefore, Si-IF fine-grain computation helps to bridge the gap between cognitive systems and the human brain.

3rd IEEE EPS FPV 2020 AWARD and US$ 300 receives **Sarthak Acharya**, Embedded Internet System Lab (EISLAB), Department of Computer Science, Electrical and Space Engineering (SRT), Luleå Technical University, Sweden-97187 for the future packaging vision—**An Additive Production approach for Microvias and Multilayered polymer substrate patterning of 2.5 μm feature sizes**

This future packaging vision is about a fully additive production approach, which is capable of producing 2.5 micrometer of L/S and microvias of 10 micrometer diameter. Results and process flow of the process is shown in the vision in detail. Future possibilities of the Work and its impact on the research community is presented and mapped with the EPS HIR.

IEEE EPS FPV 2020—Place 4: **Paritosh Rustogi** Next-Generation High-Channel-Density Implant-Connector Technology

This future packaging vision deals with the present day challenges in the packaging of implantable neural interface and their solution to the problem. Research focusses on development of a new implantable connector technology for high-channel application. The scalable implantable neural interface is scalable and supports future development of neural interfaces in channel number and density with its 2-D array design.

IEEE EPS FPV 2020—Place 5: **Lin Hou**, A novel iso-thermal intermetallic compound insertion bonding to improve throughput for sequential 3D stacking

This future packaging vision presents a developed stacking strategy, which allows significantly improvement of throughput for die-to-wafer stacking with a low cost for fine pitch solder joint. It also demonstrated the potential to perform the stacking at solid-state to avoid the solder bridge issue for fine pitch solder joint.

IEEE EPS FPV 2020—Place 6: Cheol Kim Planar-Radial Structured TEC Device for Local Hot Spot Cooling in Mobile Electronics

This future packaging vision proposes an active cooling device using a solid-state thermoelectric cooler TEC with a unique planar-radial structure that can selectively cool only locally generated hot spots and minimize form factor designs with 2D structures, making this cooling device highly applicable to mobile devices.

Please see the full papers and presentations of the winners at the IEEE EPS ECTC 2020 digital event in June 2020. It is **for free** to register this year

TC Emerging Technologies Committee

The technical committee Emerging Technologies (former TC MEMS) website (https://cmte.ieee.org/eps-mems/) is poised to act as the central portal for disseminating recent activities in emerging technologies for packaging applications. Interested colleagues are cordially invited to collaborate with the TC. Our major TC meetings welcome interested guests and take place at the ECTC conference in May and at the ECTC paper selection meeting in November, each year, please join us and visit our website for more information or to contact IEEE EPS TC Co-Chair, Dr. Karlheinz Bock.

Author: Karlheinz Bock

Congratulations to IEEE EPS Senior Members

New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between December 2019 and April 2020.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

For additional information or to apply online: https://www.ieee.org/membership/senior/

David Light, New Hampshire Section, USA
Joseph Soucy, Boston Section, USA
Yoichi Taira, Tokyo Section, Japan
Tom Dory, Phoenix Section, USA
Przemyslaw Gromala, Germany Section
Kaladhar Radhakrishnan, Phoenix Section, USA
Vaishnav Srinivas, San Diego Section, USA

ECTC 2020 Travel Award Winners

Congratulations to the winners of the 2020 ECTC travel award. The award is intended to assist students to attend ECTC. Since ECTC 2020 was virtual, the winners can use their award to attend a future EPS flagship or ECTC 2021.

- **Lin Hou,** KU Leuven
- **Noriyuki Takahashi,** Tohoku University
- **Claudio Alvarez,** Georgia Institute of Technology
- **Musa Mahmood,** Georgia Institute of Technology
- **Stephen Anderson,** Rensselaer Polytechnic Institute
- **S. W. Liu,** National Tsing Hua U.
- **Cheryl Selvanayagam,** Singapore University of Technology and Design
- **Ying Yang,** University of Sherbrooke
- **Pengbo Yu,** Tsinghua University
- **Tian Yu,** Xiamen University

Congratulations to the ECTC Volunteer Award Recipients

The EPS/ECTC Volunteer Award is given to those individuals who contribute to the success of the ECTC by volunteering in one of the conference committees, year after year. Here are the 2020 EPS/ECTC Volunteer Award winners:

Sai Ankireddi	10 years
Prem Chahal	10 years
Bing Dang	10 years
Rabindra Das	10 years
Z. Rena Huang	10 years

Soon Jang	10 years
Ming Li	10 years
Wei-Chung Lo	10 years
Lejun Wang	10 years
Jin Yang	10 years

Myung Jin Yim	10 years
Rajen Dias	25 Years
Erdogan Madenci	25 Years

EPS Major Awards Nomination Period Starts on September 15

For the first time all the EPS Major Award nominations will require line submission. The nomination period to input all the required documents runs from September 15 to January 21. The Electronics Packaging Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and EP Society.

Outstanding Sustained Technical Contributions Award
To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Must have been a member of the IEEE and EP Society for the past three (3) years (2018–2020), and renewed for 2021.

Electronics Manufacturing Technology Award
To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. Work in the management of EPS Conferences or its BoG may be contributory but it is not a requirement for the award.

Eligibility: No need to be a member of IEEE and EP Society.

David Feldman Outstanding Contribution Award

To recognize outstanding contributions to the fields encompassed by the EP Society through executive or managerial directions.

Prize: $2,500 and Certificate

Basis for Judging: Contributions to the organizations or enterprises connected with the field; contributions to EPS Chapter or Board of Governors activities; contributions to the fields encompassed by the EP Society.

Eligibility: Recipient must have been a member of IEEE and EPS for the past five (5) years (2016–2020), and renewed for 2021.

Exceptional Technical Achievement Award

To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the EP Society.

Prize: $2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in EPS's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for the past three (3) years (2018–2020), and renewed for 2021. There are no requirements for service to the IEEE or EP Society.

Outstanding Young Engineer Award

To recognize outstanding contributions to the fields encompassed by the EP Society through invention, technical development, publications, or new product implementation.

Prize: $1,500 and Certificate

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the EPS Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Must have been a member of the IEEE and EPS (member grade or above) for the past three (3) years (2018–2020), and renewed for 2021, and must be 35 years of age, or younger, on December 31, 2020.

Regional Contributions Award

To recognize significant and outstanding leadership and contributions to the growth and impact of EPS programs and activities at the Region level. Maximum of one award annually from each Region/Groups of Regions (3 awards): Regions 1-7 & 9; Region 8; and Region 10.

Basis for Judging: Demonstrated service and leadership in areas that may include but are not limited to Chapter activities, Conference/Workshop activities, Membership Development, Student Programs and Technical Activities. The respective EPS Regional Advisory Committees will receive nominations, evaluate candidates, select a candidate(s), and present candidate(s) to EPS Awards Committee for review and approval.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for the past three (3) years (2018–2020), and renewed for 2021.

Guidelines for Nominators

- A recipient of any EPS Major Award will be eligible for nomination for another EPS Major Award *after two award cycles have passed*. (i.e., Recipient of XX Award in 2018 becomes eligible for nomination for YY Award in 2021). For lists of past awardees, see http://eps.ieee.org/awards.html
- Past recipients of an award are not eligible to receive that same award. For lists of past awardees, see http://eps.ieee.org/awards.html
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- An individual may submit only one endorsement per award but may submit endorsement for more than one award.
- It is the responsibility of the nominator to ensure quality documentation to assist the Awards Committee in evaluating the candidate.
- Outstanding Sustained Technical Contribution Award is designed for the "practitioner", while the Electronics Manufacturing Technology Award intended for "Corporate Leadership."
- Complimentary material, such as candidate's picture, CV, list of publications and/or patents should be submitted separate from the award nomination.
- Self-nominations **will not** be considered.

EPS PhD Fellowship

To promote, recognize, and support PhD level study and research within the Electronics Packaging Society's field of interest.

Prize: A plaque and a single annual award of US$5,000, applicable towards the student's research.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electronic packaging and a proven history of academic excellence, as documented in:

- Nomination by an IEEE EPS Member. Only one nomination per member per year.
- Two-page (maximum) statement by the student describing his or her education and

- Research interests, accomplishments, and impact on the electronics package industry.
- Proof of contributions to the community may consist of open literature publications (preferred) such as papers, patents, books, and conference presentations and reports (available to the public).
- At least one letter of recommendation from someone familiar with the student's work
- Student resume

Eligibility: Candidate must be an IEEE EPS member, at the time of nomination, and be pursuing a doctorate degree within the EPS field of interest on a full-time basis from an accredited graduate school or institution. The candidate must have studied with her/his advisor for at least 1 year, at the time of nomination, to be eligible. A Student who received a Fellowship award from another IEEE Society, within the same year, or is a previous EPS Fellowship winner is ineligible.

All Award nominations must be **online**. Nominations questions can be sent to the Society Awards Program director:

Eric Perfecto
Eric.Perfecto.US@ieee.org

Winners will be notified by April 2021, and the awards will be presented at the 71st Electronic Components and Technology Conference (ECTC), June 1–4, 2021 in San Diego, CA, USA

PUBLICATION NEWS

2019 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 200 published papers and represent the best, based on criteria including originality, significance, completeness and organization. The awards will be presented at the 71st Electronic Components and Technology Conference (ECTC), June 2021.

Subscribers to this publication can access the papers on-line in IEEE Xplore at:

http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870

Advanced Packaging Technologies Category
"Transferable-Tip Technology for Fine-Pitch Probes and Interconnections"
VOLUME 9, ISSUE 9, AUGUST 2019
Steven Wright, Yang Liu

Abstract: A transferable-tip technology has been developed that has applications for wafer-level fine-pitch probe and electrical test of semiconductor devices. The tips are made by filling a mold made in a (100)-oriented Si substrate wafer, with cavities created by anisotropic etch. The tips are very sharp and planar, with a precise cone angle of 70.5°. The metal tips are then transferred to any suitable substrate, using a solder and release process. The tips, used in a probe head, enable electrical contact to large-area microbump arrays at low force. Test structures were fabricated with as many as 250000 tips at the 50-μm pitch. This approach also enables test electronics to be incorporated into the probe head. In this way, high-speed functional tests can be performed that minimize difficulties normally encountered in wiring and shielding many high-frequency signals in the probe head and to external test electronics. This probe tip technology also has potential for improved chip-to-chip interconnections that ensure known-good-dies are added to a chip stack. As compared to other probe contact technologies, the transferable-tip approach is potentially low-cost and amenable to new modes of probing, particularly applicable to chip stacks made with 3-D Si integration and heterogeneous integration.

URL: https://ieeexplore.ieee.org/document/8747370

Components: Characterization and Modeling Category
"Evaluation of Additively Manufactured Microchannel Heat Sinks"
VOLUME 9, ISSUE 3, MARCH 2019
Ivel L. Collins, Justin Weibel, Liang Pan and Suresh V. Garimella

Abstract: Microchannel heat sinks allow the removal of dense heat loads from high-power electronic devices at modest chip temperature rises. Such heat sinks are produced primarily using conventional subtractive machining techniques or anisotropic chemical etching, which restricts the geometric features that can be produced. Owing to their layer-by-layer and direct-write approaches, additive manufacturing (AM) technologies enable more design-driven construction flexibility and offer improved geometric freedom. Various AM processes and materials are available, but their capability to produce features desirable for microchannel heat sinks has received a limited assessment. Following a survey of commercially mature AM techniques, direct metal laser sintering was used in this paper to produce both straight and manifold microchannel designs with hydraulic diameters of 500 μm in an aluminum alloy (AlSi10Mg). Thermal and hydraulic performances were characterized over a range of mass fluxes from 500 to 2000 kg/m 2 s using water as the working fluid. The straight microchannel design allows these experimental results to be directly compared against widely accepted correlations from the literature. The manifold design demonstrates a more complex geometry that offers a reduced pressure drop. A comparison of the measured and predicted performance confirms that the nominal geometry is reproduced accurately enough to predict pressure drop based on conventional hydrodynamic theory, albeit with roughness-induced early transition to turbulence; however, the material properties are not known with sufficient accuracy to allow for a priori thermal design. New design guidelines are needed to exploit the benefits of AM while avoiding undesired or unanticipated performance impacts.

URL: https://ieeexplore.ieee.org/document/8444653

Electrical Performance of Integrated Systems Category
"Stochastic Collocation with Non-Gaussian Correlated Process Variations: Theory, Algorithms and Applications"
Chunfeng Cui and Zheng Zhang
Volume 9, Issue 5, July 2019

Abstract: Stochastic spectral methods have achieved a great success in the uncertainty quantification of many engineering problems, including variation-aware electronic and photonic design automation. State-of-the-art techniques employ generalized polynomial-chaos expansions and assume that all random parameters are independent or Gaussian correlated. This assumption is rarely true in real applications. How to handle non-Gaussian correlated random parameters is a long-standing and fundamental challenge: It is not clear how to choose basis functions and to perform a projection step in a correlated uncertain parameter space. This paper first presents a new set of basis functions to well capture the impact of non-Gaussian correlated parameters and then proposes an automatic and optimization-based quadrature method to perform projection-based stochastic collocation with a few simulation samples in the correlated parameter space. We further provide some theoretical proofs for the complexity and error bound of our proposed method. The numerical experiments on several synthetic, electronic, and photonic integrated circuit examples show the nearly exponential convergence rate of our approach and its significant (700×-6000×) speedup than Monte Carlo. Many other open problems with non-Gaussian correlated uncertainties can be further solved based on this paper.

URL: https://ieeexplore.ieee.org/document/8585087

To recognize the work and efforts of our Associate Editors, EPS instituted the Best Associate Editor Award. The 2020 recipients are

Sushil Bhavnani, Auburn University
Stefano Grivet-Talocia, Politecnico di Torino
Lih-Tyng Hwang, National Sun Yat-Sen University
Chin Lee, UC Irvine
Frank Shi, UC Irvine
Markondeya Pulugurtha, Florida International University

Transactions on Components, Packaging and Manufacturing Technology Reduces Sub to Online Post Time

Thanks to sustained efforts of the entire Editorial committee, the T-CPMT continues to significantly improved reduction in its turnaround time. The 2019 Fourth Quarter Submission to Publication Report indicates the average weeks from paper submission to online post is 17.2 weeks. This is 6 weeks faster than the 2019 Fourth Quarter Report. Relevant statistics:

1st Quarter 2019:
Avg Weeks to First Decision 9.0
Avg. Weeks Submitted to Online Post 17.2

4th Quarter 2018:
Avg Weeks to First Decision 12.6
Avg. Weeks Submitted to Online Post 23.5

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5 Most Popular Articles According to May 2020 Usage Statistics

These are the top 5 most frequently accessed articles in T-CPMT based on Xplore usage data.

3-D Printed Metal-Pipe Rectangular Waveguides
Mario D'Auria; William J. Otter; Jonathan Hazell; Brendan T. W. Gillatt; Callum Long-Collins; Nick M. Ridler; Stepan Lucyszyn
Publication Year: 2015, Page(s): 1339–1349

Reliability Evaluation of SiC Power Module With Sintered Ag Die Attach and Stress-Relaxation Structure
Kazuhiko Sugiura; Tomohito Iwashige; Kazuhiro Tsuruta; Chuantong Chen; Shijo Nagao; Tsuyoshi Funaki; Katsuaki Suganuma
Publication Year: 2019, Page(s): 609–615

Die Attach Materials for High Temperature Applications: A Review
Vemal Raja Manikam; Kuan Yew Cheong
Publication Year: 2011, Page(s): 457–478

Power Noise and Near-Field EMI of High-Current System-in-Package With VR Top and Bottom Placements
Kan Xu; Boris Vaisband; Gregory Sizikov; Xin Li; Eby G. Friedman
Publication Year: 2019, Page(s): 712–718

Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging
John H. Lau; Ming Li; Dewen Tian; Nelson Fan; Eric Kuah; Wu Kai; Margie Li; J. Hao; Yiu Ming Cheung; Zhang Li; Kim Hwee Tan; Rozalia Beica; Thomas Taylor; Cheng-Ta Ko; Henry Yang; Yu-Hua Chen; Sze Pei Lim; Ning Cheng Lee; Jiang Ran; Cao Xi; Koh Sau Wee; Qingxiang Yong
Publication Year: 2017, Page(s): 1729–1738

EDUCATION/CAREER NEWS

Heterogeneous Integration Roadmap (HIR) Webinar Series

The electronics industry has reinvented itself through multiple disruptive changes in technologies, products, applications and markets. Our industry continues to evolve with the rapid migration of logic, memory, and applications to the cloud, the evolution of the Internet of Things (IoT) to the Internet of Everything (IoE), the proliferation of smart mobile devices everywhere, the rise of 5G, the increasing presence of microelectronics in wearables, health applications, and the rapidly evolving issues related to autonomous vehicles applications. Underlying all the changes are the rapid advancement of AI and the increasing abundance of data & data analytics. The pace of innovation is increasing to meet these challenges.

The Heterogeneous Integration Roadmap (HIR), released October 2019, is a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration between industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of Emerging Research Devices and Emerging Research Materials with longer research-and-development timelines. With the release of the 2019 HIR edition, the preparation of the 2020 edition is underway.

We are announcing the Heterogeneous Integration Webinar Series. The series is based upon the content of the 2019 HIR edition. The webinars will be delivered by the authors of the individual roadmap chapters. The primary purposes are to broaden the proliferation of the roadmap content to the profession and industry and to seek feedback from the roadmap users for inclusion into the 2020 edition.

Watch for the invitation or visit this website for schedule details and instructions about how to register.

EPS Certificate of Achievement

In order to further the education of Electronics Packaging Society (EPS) members, the EPS is now offering a Certificate Program. The goal of the program is to give members new to electronics packaging an opportunity for further packaging education, offer continuous education in electronics packaging to existing members, and also to offer students electronics packaging training if they are in a University program that does not include packaging education.

Criteria: Must be an IEEE Electronics Packaging Society Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of EPS Webinars, Professional Development Courses at select EPS Conferences, author of IEEE T-CPMT paper and/or EPS Conference paper, reviewer for IEEE T-CPMT.

Once you have completed any combination of the above and received 15 PDHs, please complete the **certificate form** to request your Electronics Packaging Society Certificate.

Congratulations to these EPS Members on receiving the IEEE Certificate of Achievement from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Shaw Fong Wong, Intel Corporation
Jeffrey C. Suhling, Auburn Unviersity
Siddharth Ravichandran, Georgia Institute of Technology
Agneta Elisabet Ljungbro, Ericsson AB
Omkar Gupte, Georgia Institute of Technology
Joseph Soucy, Charles Stark Draper Laboratory
Chandrasekharan Nair, Intel Corporation
Chintan Buch, Applied Materials Inc.

EPS Distinguished Lecturers are selected from among EPS Fellows, Award winners, and Society leaders, who are members of the technical community and experts in their field. They are available to present lectures and/or courses at EPS events—Chapters, Conferences, Workshops or Symposia; as well as IEEE Student Chapter events.

The EPS Distinguished Lecturer Program (DLP) aims at serving communities interested in the scientific, engineering, and production aspects of materials, component parts, modules, hybrids and micro-electronic systems for all electronic applications.

The Program strives to support EPS Chapters worldwide by helping them to invite leading researchers in their respective fields and IEEE Student Chapters to encourage students to pursue EPS related fields and to join the EPS society. The DLP talk is a major event in the life of the inviting Chapter.

EPS Distinguished Lecturers

Mudasir Ahmad (6/2017–6/2021)
Cisco Systems, Inc.
Topics: Internet of Things (IoT), Advanced Packaging, 2.5D, Heterogeneous Silicon Photonics, Advanced Reliability (Thermo-mechanical, Mechanical Shock), Numerical Modeling, Advanced Thermal Solutions, Stochastic Analysis, Bayesian Inference, Machine Learning, Artificial Intelligence

Muhannad Bakir, Ph.D. (1/2020–1/2023)
School of Electrical and Computer Engineering
Georgia Institute of Technology
Topics: Emerging interconnection architectures and technologies; heterogeneous system design and integration

Avram Bar-Cohen, Ph.D. (1/2020–1/2023)
Raytheon
Topics: Thermal packaging

Karlheinz Bock, Ph.D. (6/2016–6/2020)
Technische Universität Dresden
Topics: Multifunctionality & heterosystemintegration & additive manufacturing (IoT, Industry 4.0, tactile internet), packaging for mechanical, digital and power co-integration (automotive, machines, robots..), 2.5D and 3D electro-optical-RF interposer and board (high performance), heterointegration for flexible, bio, organic and large area electronics (open form factor)

Bill Bottoms, Ph.D. (1/2017–1/2021)
Third Millennium Test Solutions
Topics: Heterogeneous Integration, Semiconductor test technology, Emerging research materials, Packaging of electronic components and systems, the global network and its future requirements, the internet of things and Smart manufacturing

Chris Bower, Ph.D. (1/2017–1/2021)
X-Display
Topics: Novel assembly methods, elastomer stamp micro-transfer-printing, heterogeneous integration, three-dimensional integration, manufacturing of micro-assembled displays and other large-format electronics.

William T. Chen, Ph.D. (1/2020–1/2023)
ASE (U.S.) INC
Topics: Semiconductor and Electronics Industry Trends and Roadmap

Xuejun Fan, Ph.D. (1/2020–1/2023)
Lamar University
Topics: Design, modeling and reliability in micro-/nano- electronic packaging and microsystems

Philip Garrou, Ph.D. (1/2020–1/2023)
Microelectronic Consultants of North Carolina
Topics: Thin film technology; IC packaging and interconnect; Microelectronic materials; 3D-IC integration

Subu Iyer, Ph.D. (6/2017–6/2021)
University of California, Los Angeles
Topics: Heterogeneous Integration; Flexible hybrid electronics; 3D interposer, and wafer scale integration and stacking\

Beth Keser, Ph.D. (1/2020–1/2023)
Intel
Topics: Fan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; photoimageable liquid polymer films

Pradeep Lall, Ph.D. (1/2020–1/2023)
Auburn University
Topics: Semiconductor Packaging, Modeling and Simulation, Reliability in Harsh Environments, Shock/Drop/Vibration, Cu Wirebonding, Flexible Hybrid Electronics, Additive Manufacturing, Prognostics and Health Management, LEDs, Micro CT Measurements

John H. Lau, Ph.D. (1/2020–1/2023)
ASM Pacific Technology
Topics: Electronics and Photonics 2D and 3D packaging and manufacturing

Ravi Mahajan, Ph.D. (6/2016–6/2020)
Intel Corporation
Topics: Advanced Packaging Architectures, Assembly Processes and Thermal Management

James E. Morris, Ph.D. (1/2020–1/2023)
Portland State University
Topics: Electrically conductive adhesives; Electronics packaging; Nanotechnologies

Mervi Paulasto-Kröckel, Ph.D. (6/2016–6/2020)
Aalto University
Topics: MEMS, electronics reliability, automotive components and packaging, implantable electronics, dissimilar materials & interfaces

Eric D. Perfecto, (1/2020–1/2023)
Independent Consultant
Topics: Fine pitch interconnect, chip to chip and chip to laminate connection, UBM and solder selection, chip package interaction and 2.5D fabrication

Mark Poliks, Ph.D. (1/2020–1/2023)
Binghamton University (SUNY)
Topics: Materials and Processes, Advanced Manufacturing, Flexible Hybrid Electronics, High Speed and Additive

Jose Schutt-Aine, Ph.D. (1/2020–1/2023)
University of Illinois
Topics: High-Frequency Measurements, Mixed-Signal Design, High-Performance Computing, electromagnetic Modeling, Signal Integrity, CAD Tools for Interconnects and Packages, Machine Learning for High-Speed System Modeling

Nihal Sinnadurai
Topics: Accelerated Ageing for Reliability Assurance–theory and practical methods—including HAST (my invention originally); The use of encapsulation and plastic packaging and reliability evaluation method; PCB & Hybrid technologies; Thermal management and design

Ephraim Suhir, Ph.D. (1/2020–1/2023)
Topics: Accelerated life testing; Probabilistic physical design for reliability; Bonded assemblies; Thermal stress; Predictive modeling; Fiber optics structures: design for reliability; Dynamic response to shocks and vibrations

Chuan Seng Tan, Ph.D. (6/2019–6/2023)
Nanyang Technologica University
Topics: 3D Integration and packaging, Fine Pitch Cu-Cu Bonding Through Silicon Vias (TSVs), Group IV Semiconductors: Material Growth, Engineered Substrates, and Device Applications

Rao Tummala, Ph.D. (1/2020–1/2023)
Georgia Institute of Technology
Topics: Electronics Packaging

E. Jan Vardaman (1/2020–1/2023)
TechSearch International, Inc.
Topics: International developments in semiconductor packaging, manufacturing and assembly; SiP: Business and technology Trends; drivers in advanced packaging; Flip chip and wafer level packaging

Paul Wesling (1/2020–1/2023)
Topics: Using Xplore, and Google Scholar to Mine IEEE's Online Repository of Technical Information; Origins of Silicon Valley and the EPS

C.P. Wong, Ph.D. (1/2020–1/2023)
Georgia Institute of Technology
Topics: Materials

Jie Xue, Ph.D. (1/2020–1/2023)
Cisco Systems, Inc
Topics: Advanced Packaging for Networking Application; Impact of Internet of Everything (IoE) to Semiconductor Industry ecosystem; High performance substrate technologies; Trends and challenges of Silicon Photonics for datacenter and networking applications

CONFERENCE NEWS

Top Conference Papers based on Xplore Usage

2019 IEEE 69th Electronic Components and Technology Conference (ECTC)

(May 28–31, 2019)

System on Integrated Chips (SoIC(TM) for 3D Heterogeneous Integration
Ming-Fa Chen; Fang-Cheng Chen; Wen-Chih Chiou; Doug C.H. Yu

Active Interposer Technology for Chiplet-Based Advanced 3D System Architectures
Perceval Coudrain; J. Charbonnier; A. Garnier; P. Vivet; Rémi Vélard; A. Vinci; F. Ponthenier; A. Farcy; R. Segaud; P. Chausse; L. Arnaud; D. Lattard; E. Guthmuller; G. Romano; A. Gueugnot; F. Berger; J. Beltritti; T. Mourier; M. Gottardi; S. Minoret; C. Ribière; G. Romero; P.-E. Philip; Y. Exbrayat; D. Scevola; D. Campos; M. Argoud; N. Allouti; R. Eleouet; C. Fuguet Tortolero; C. Aumont; D. Dutoit; C. Legalland; J. Michailos; S. Chéramy; G. Simon

Signal Integrity of Submicron InFO Heterogeneous Integration for High Performance Computing Applications
Chuei-Tang Wang; Jeng-Shien Hsieh; Victor C. Y. Chang; Shih-Ya Huang; T. Ko; Han-Ping Pu; Douglas Yu

3D-MiM (MUST-in-MUST) Technology for Advanced System Integration
An-Jhih Su; Terry Ku; Chung-Hao Tsai; Kuo-Chung Yee; Douglas Yu

Low Temperature and Pressureless Microfluidic Electroless Bonding Process for Vertical Interconnections
Han-Tang Hung; Sean Yang; I-An Weng; Yan-Hao Chen; C. Robert Kao

2019 18th IEEE Intersociety Conference on

Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(May 28–31, 2019)

Cell Tab Cooling System for Battery Life Extension
Heiner Heimes; Achim Kampker; Ahmad Mohsseni; Francesco Maltoni; Jan Biederbeck

Additive Manufacturing of Compact Manifold-Microchannel Heat Exchangers Utilizing Direct Metal Laser Sintering
Hadi Keramati; Fabio Battaglia; Martinus A. Arie; Farah Singer; Michael M. Ohadi

Modeling Performance and Thermal Induced Reliability Issues of a 3nm FinFET Logic Chip Operation in a Fan-Out and a Flip-Chip Packages
Munkang Choi; Xiaopeng Xu; Victor Moroz

Experimental Demonstration of an Additively Manufactured Vapor Chamber Heat Spreader
Serdar Ozguc; Saeel Pai; Liang Pan; Patrick J. Geoghegan; Justin A. Weibel

A Metamodeling Approach for Optimization of Manifold Microchannel Systems for High Heat Flux Cooling Applications
Sevket U. Yuruker; Raphael K. Mandel; Amir Shooshtari; Michael M. Ohadi

2019 IEEE 21st Electronics Packaging Technology Conference (EPTC)

(December 4–6, 2010)

Ultra High Density Package Design and Electrical Analysis in High Performance Computing Application
Tsun-Lung Hsieh; Hung-Chun Kuo; Ming-Fong Jhong; Chih-Yi Huang; Chen-Chao Wang

Innovative Packaging Solutions of 3D Integration and System in Package for IoT/Wearable and 5G Application
Frank Lian; David Wang; Ryan Chiu; Jase Jiang; Yu-Po Wang

Development of FCBGA Substrate with low Dk/Df Material Based on Automotive Reliability Conditions
ShinKi Lee; WooYong Jung; ChangWon Ma; DongSu Lee; YounHo Jung; DaeShin Lee; SangWook Han; Eun-Chul Ahn; YoungHwan Shin; HanSung Lee; HunJung Lim; InSeok Hwang

Process and Design Consideration for Wafer-to-Wafer Hybrid Bonding
I-Ting Wang; KJ Chui; Yao Zhu

Thermal Simulation and Measurement of SiC MOSETs
Jung Kyun Kim

Upcoming Conferences

Dear Members and Patrons of the IEEE Electronics Packaging Society,

With the health and safety of our members and participants being our first priority, please know that our thoughts are with those affected by the COVID-19 outbreak.

We are closely monitoring the developments related to this pandemic and working diligently with the IEEE and our conference organizing committees worldwide, on our preparedness. Some of the conferences sponsored by our society that are scheduled to be held during these challenging few months have been already rescheduled or canceled. Others are coming up in the later part of this year, and we are carefully watching the developments and ready to make swift decisions, as needed.

The following is the current status of the EPS sponsored conferences in the remainder of 2020. As the situation keeps changing dynamically, please reference the EPS Conference webpage for weekly updates

Conferences **financially** sponsored/co-sponsored by the EPS:

ITHERM	May 26–29, 2020	Orlando, FL, USA	In person event canceled—virtual event July 21–23, 2020. Live and on demand content.
ESTC	Sep 15–18, 2020	Vestfold, Norway	Virtual Event September 15–18, 2020
IEMT	Sep 28–30, 2020	Putrajaya, Malaysia	Postponed to September 2021
EPEPS	Oct 4–7, 2020	San Jose, CA, USA	Actively working with IEEE MCE for converting into a hybrid event
HOLM	Oct 4–7, 2020	San Antonio, TX, USA	No change
ICSJ	Nov 9–7, 2020	Kyoto, Japan	No change
EPTC	Dec 2–4, 2020	Singapore	No change—looking into possible hybrid options
EDAPS	Dec 14–16, 2020	Shenzhen, China	No change

Conferences **technically** sponsored/co-sponsored by the EPS:

EuroSimE	Apr 26–29, 2020	Cracow, Poland	Going virtual with live sessions on July 6–7, 2020 and on-demand content from July 6–27, 2020
ASMC	May 4–7, 2020	Saratoga Springs, NY, USA	Postponed to August 23–25, 2020
ISSE	May 13–17, 2020	Demanovska Valley, Slovakia	Virtual Conference May 14–15, 2020
IEDS	May 19–22, 2020	Chengdu, China	Postponed to Nov 11–13, 2020
ICEC	Jun 15–18, 2020	Rorschach, Switzerland	Cancelled. To be held June 7–10, 2021
DTIP			Virtual Event June 15–26, 2020

3D-PEIM	Jun 22–24, 2020	Osaka U, Japan	Biennial—Postponed to Jun 21–23, 2021
ICEPT	Aug 12–15, 2020	Guangzhou, China	No Change—evaluating backup options
EOS/ESD Symposium	Sep 13–18, 2020	Reno, NV, USA	No change
THERMINIC	Sep 23–25, 2020	Berlin, Germany	No Change
MID	Sep 29–30, 2020	Amberg, Germany	No Change
QCE	Oct 12–15, 2020	Denver, CO, USA	No Change
IMPACT	Oct 21–23, 2020	Taipei, Taiwan	No change

TECHNOLOGY

Nanopackaging Provides Breakthrough Solutions for Emerging Electronic and Bioelectronic Systems (P M Raj, Florida International University, Miami)

Several nanopackaging technologies are coming to the forefront because of the increased drive towards heterogeneous system integration with miniaturization, better power efficiency and multiple functions. The Nanopackaging Technical Committee has been active with both the EPS and Nanotechnology Council activities for the past year in highlighting and promoting these advances through focused EPS Website and Newsletter Articles, technical sessions at IEEE NANO and IEEE NMDC, IEEE Nanotechnology Magazine special issues in Nanopackaging and papers at the ECTC. This newsletter highlights the role of nanopackaging in emerging systems, recent advances and committee highlights.

Nanotechnologies for Heterogeneous System Integration: Heterogeneous device and component co-packaging technologies has been the singular focus of the industry to realize future electronic and bioelectronic systems. Such systems will pervade mobile and high-performance computing, 5G- and 6G-enabled high-bandwidth and high-speed networks, IoT (Internet of Things) and connectivity, implantable and wearables for health monitoring and therapy, high-power modules, Advanced Driver Assistance Systems (ADAS) and others. The key packaging technology building blocks to realize such systems are: a) interconnects with computing bandwidth exceeding 10 Tbps and energy of < 0.1 pJ/bit; b) high-efficiency granular power delivery to different voltage domains within the devices; c) seamless RF front-end module integration with antenna arrays, passives, beamforming and transceiver devices in thin packages; d) compact 3D power converters; e) active microelectrode arrays with integrated power and signal conditioning, power and data telemetry in bioelectronics etc. Higher component densities with seamless system component integration is required to realize any of these building blocks and systems, which is enabled by nanopackaging. ***In this newsletter, we highlight some recent nanopackaging advances in the topics of power delivery with nanocapacitors, die-attach materials, 5G and 6G systems and biomedical electronics***.

Nanocapacitors for Power Delivery: Power supply is emerging as a major challenge in realizing future computing systems for both mobile processors because of the size restrictions, and in data processing-intensive applications such as servers or data centers because of the need for high efficiency and performance. Power supply includes power conversion, power delivery and power management. Current approaches create several limitations in each of these sub-systems: 1) power conversion far from the load, limiting the response time, 2) multiple stages of conversion, reducing efficiency, 3) low-density inductors and capacitors leading to large size and 4) large losses due to long interconnections through the board. Advanced substrate-compatible thinfilm or thickfilm processes are being developed to achieve higher power handling with thinner form-factors. Irrespective of the power conversion topologies, capacitors have the most critical role in managing low power power-delivery network impedances from low to higher switching frequencies. Capacitor-based power conversion with switch capacitor networks or hybrid resonant converters are also emerging as alternatives to switching regulator topologies to address the size, electromagnetic interference and integration limitations of thick magnetic components. Recently, CNT-based capacitors have been reported by Smoltek Inc. (https://www.smoltek.com/cnf-mim) to achieve high volumetric capacitance densities. The high surface area of CNT with thin electrodes is the key advantage of this approach. Vincent Desmaris et al., at Smoltek have demonstrated the suitability of carbon nanofiber based MIM capacitors (CNF-MIM) on various substrates such as silicon, glass and alumina for prospective use as discrete or integrated passives on chips or interposers. These capacitor films are only 5 microns thick. However, capacitance densities larger than 300 nF/mm2 have been measured on all substrates including a 30-μm thick Silicon substrate. These ultrathin capacitors featured Equivalent Series Resistance values of less than 40 mOhm, Equivalent Series Inductance below 10 pH and leakage currents as low as 0.004 nA/nF at 1 V with device breakdown at 6 V, which makes them a promising candidate both for highly integrated, multifunctional on-chip and discrete miniaturized electronic components.

Thermal Management: Nanocopper for Thermal Vias, Integrated Heat-Spreaders and thin interconnections: Reliability and performance of electronics is very sensitive to the local

hot-spots from improper heat transfer paths. Without significant advances in board-level heat dissipation, either digital or 5G or power modules will not deliver the anticipated system level performance improvements. Alfred Zinn (CTO, Kuprion Inc, https://www.kuprioninc.com/about) recently reported breakthrough advances in Kuprion's patented nanocopper material platform as a viable solution to board-level thermal management. The low-temperature sintering of nanocopper and additive deposition in printed circuit boards with the formation of very larger-diameter thermal vias provides flexible design and fabrication routes. The shape and geometry of the pastes can be easily adapted with additive technologies. Kuprion Inc. was already able to demonstrate 4 mm diameter vias through a PCB with and processing temperatures around 200 C in just 5–6 min. The resulting vias are over 90% dense with thermal conductivity as high as 290 W/mK and a reduced CTE of just 11 ppm, making this patented technology a game-changer for the electronics industry. These vias demonstrate excellent mechanical properties, surviving adequate thermal shock cycles with no measurable decline in strength.

As power modules migrate to higher power densities, Kuprion's nanocopper is able to provide lowest thermal impedances between the power switches, heat-spreaders and cold-plates, enabling an all-copper, highly-conductive connection from the chip to the heat sink, while also being able to handle high current-densities without electromigration or other electrical reliability issues. Once sintered, the nanocopper material converts to bulk copper for high-temperature operation despite low temperature processing and can be safely reheated many times without softening. Sintered nanocopper is also solderable, making it compatible with current SMT design and processing. Distributed thick copper structures like via arrays will have a major impact on all system applications ranging from 5G, power modules and computing. High-temperature platforms such as LEDs and automotive and power electronics will also benefit from these advances in heat dissipation materials. Nanocopper has been extended to fine-pitch chip-to-package interconnections by Jonas Zurcher et al., in IBM Zurich, with dip-coated copper pillars. Low electrical parasitics and high bonding shear strengths are demonstrated with pitches of 10–20 microns and processing temperatures of 160–200 C.

High-Power Modules: Nanosilver and Nanocopper Die-attach: Jiang Li (currently at Texas Instruments) reports that sintered nanosilver die-attach showed better thermomechanical reliability and lower thermal impedance compared with traditional lead-free solder materials. A four-chip IGBT power module with symmetric double-side cooling planar structure is demonstrated with nanosilver die-attach materials. A structure of asymmetric double-side module with sintered silver bump array is also proposed and validated for power handling and reliability. As an alternative to silver die-attach materials, Mohan Kasyap and Vanessa Smet et al., have been pioneering sintered nanocopper die-attach materials with dealloyed porous nanocopper that can sinter at low temperatures. Large-array fabrication of nanocopper was demonstrated on copper foils with low-temperature processing but with properties approaching that of bulk copper have been achieved. Nanocopper from Kuprion Inc. has been shown to meet all the performance and reliability metrics for SiC die attach on Direct Bonded Copper (DBC) and AlN substrates even with bondline thickness of 2–5 microns and processing at 200 ºC for 4–5 min.

Nanopackaging for 5G and 6G: Millimeter wave or THz-enabled sub-systems will dominate future communication networks for broadband wireless mobile connectivity, vehicle-to-vehicle, vehicle-to-network, IoT, imaging and sensing, and other applications that demand high reliability, and zero perceived latency. For mm-wave enabled 5G packaging, nanotechnologies are also critical for integrated low-loss package-level interconnects with nanometer-scale metal-dielectric interfaces for low mm-wave losses and good adhesion, and integrated thermal management with copper and low-CTE copper nanocomposites. Dielectric nanocomposites are suitable for miniaturizing H walls, E walls, lenses for beam-steering, and frequency-selective surfaces such as Artificial Magnetic Conductors (AMCs) for improved gain. As another demonstration of advances in 5G Nanopackaging, Watanabe, at Georgia Tech – Packaging Research Center, in partnership with Nagase Inc., have extended the use of nanocopper paste for printed short interconnections for 5G transceiver IC assembly. This technology can be realized with simple additive manufacturing. Improved conductivities are achieved by sintering at temperature of 260 °C for low conductive loss and low interconnection parasitics in 5G applications.

Nanopackaging of THz devices can take the communication technologies to beyond the currently-sought 5G wireless communication, with Tbps data rates. In conjunction with spread-spectrum techniques for low-power directional networking, THz communications are more suitable for emerging high-throughput covert networks with a protective covering to eavesdropping and anti-jamming. Other examples of applications resulting from THz technologies are security, medical imaging and high-resolution automotive radar for autonomous vehicles. In spite of these numerous possibilities, several barriers are immediately apparent in the realization of 6G systems. These barriers include low transceiver powers that demand ultra-massive MIMOs for larger communication distances. Sub-THz or 6G communications focus on heterogeneous package integration by incrementally advancing the system components such as precision antenna arrays, low-loss interconnects and waveguides and active devices, where nanotechnologies play a similar role as in 5G. Emerging THz sensing and imaging applications provide an entirely new avenue for nanotechnologies through the heterogeneous integration of THz radiation sources, waveguides and phase shifters, detectors and other system components on a single chip or multichip packages. Compact and high-output power sources and high-responsivity low-noise detectors that can operate at THz band are required to surmount the high path-loss at these frequencies. Key innovations include integration of graphene-based radiation sources and detectors, THz antenna arrays (ex. 1024 elements in 1 mm^2), lenses and intelligent metasurfaces with space-time-frequency coding and low-loss interconnects.

Nanopackaging with Low-Impedance Neural Electrodes: Emerging wearable and implantable biomedical systems that provide health-tracking and therapeutic functions with miniaturization

and high reliability are also benefiting from nanopackaging. Sepehr Soroushiani et al. at FIU have been exploring nanoelelectrodes for neurostimulation because of its combined advantages of high current-injection capacity along with low impedance with smaller electrode footprints. Suitable nanocomposite electrode structures can address the mechanical compatibility issues between the electrode and surrounding tissues for reduced inflammation. These neuroelectrodes can be extended from polymer microinterconnects with seamless connectivity. Along with passive components for power and data telemetry, nanopackaging is also investigated as the avenue for realizing hermetic and rematerable interfaces in biomedical implants.

Hermetic Nanopackaging of Flexible Electronics: With the trend to low-cost flexible electronics for wearables IoT, display and implantable electronics, organic functional materials and their packaging in polymer films is becoming extremely important. Since polymers are not inherently hermetic, they are prone to diffusion of moisture, oxygen, and other reactive ions. For long-term reliability, it is important to protect the systems with inorganic hermetic coatings. Nanoscale barriers can be deposited as ultra-thin conformal coatings and can replace bulky ceramic cases and hermetic cans that are brazed onto the chip carrier substrate in bioelectronics implants. This can eliminate the extra volume in the hermetic package, and also lead to better flexibility and less constraints during implantation. The inorganic coatings that are widely studied are alumina, stack of alumina and SAOL (self-assembled organic layers), stack of alumina/titania and zirconia. Even 100 nm inorganic encapsulation can lower the water vapor transmission rates by 4–7 orders of magnitudes compared to the best thick polymer barriers. Simple alumina layers are easily prone to humidity-assisted degradation because of the internal hydroxide crystallization. For on-body applications, electronic devices are continuously exposed to sweat and are constantly being deformed, which requires a robust and thin encapsulation. Vladimir Pozdin at FIU reports on the use of Atomic Layer Deposited (ALD) Al2Ox film with parylene for ultra-thin device encapsulation. His research demonstrates a cytotoxicity score of 0 for the ALD coatings processed at 100 °C, implying a safe and durable coating for flexible wearable devices.

Other Nanopackaging TC Highlights: IEEE NANO 2020 is originally poised to have exciting presentations in the area of Nanopackaging on topics ranging from nanosilver die-attach materials (Jiang Li, Texas Instruments), CNT nanocapacitors (Vincent Desmaris, Smoltek), Hermitic flexible packaging (Vladimir Pozdin, FIU) and nanocopper additive manufacturing (Alfred Zinn at Kuprion Inc). However, because of the current situation, we expect these papers and other interesting topics will be covered in IEEE NANO 2021. IEEE NANO will instead host a virtual conference in 2020 with selected papers and keynote presentations.

Nanopackaging TC Co-Chair, Dr. Raj has been chosen as the Nanotechnology Distinguished Lecturer for 2020 by the Nanotechnology Council. As a part of this recognition, he will be giving seminars on "Heterogeneous System Component Integration with Nanopackaging" at multiple conferences and society or local chapter events. He is scheduled to give a talk the IEEE NANO Virtual Conference (July 29–31), and the Nanotechnology Council, Northern Virginia and Washington Jt. Sections Chapter on June 16.

The Nanopackaging TC website is poised to act as the central portal for disseminating recent advances in nanotechnologies for packaging applications. Readers are encouraged to report any press releases to us for prompt posting on our website. Contributors are welcome to send their news items to the web coordinators on the website: https://cmte.ieee.org/eps-nano/

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Should we get a critical mass together, a face-to-face meeting could be scheduled at the Electronics Goes Green conference, September 1–3 2020 in Berlin, Germany.

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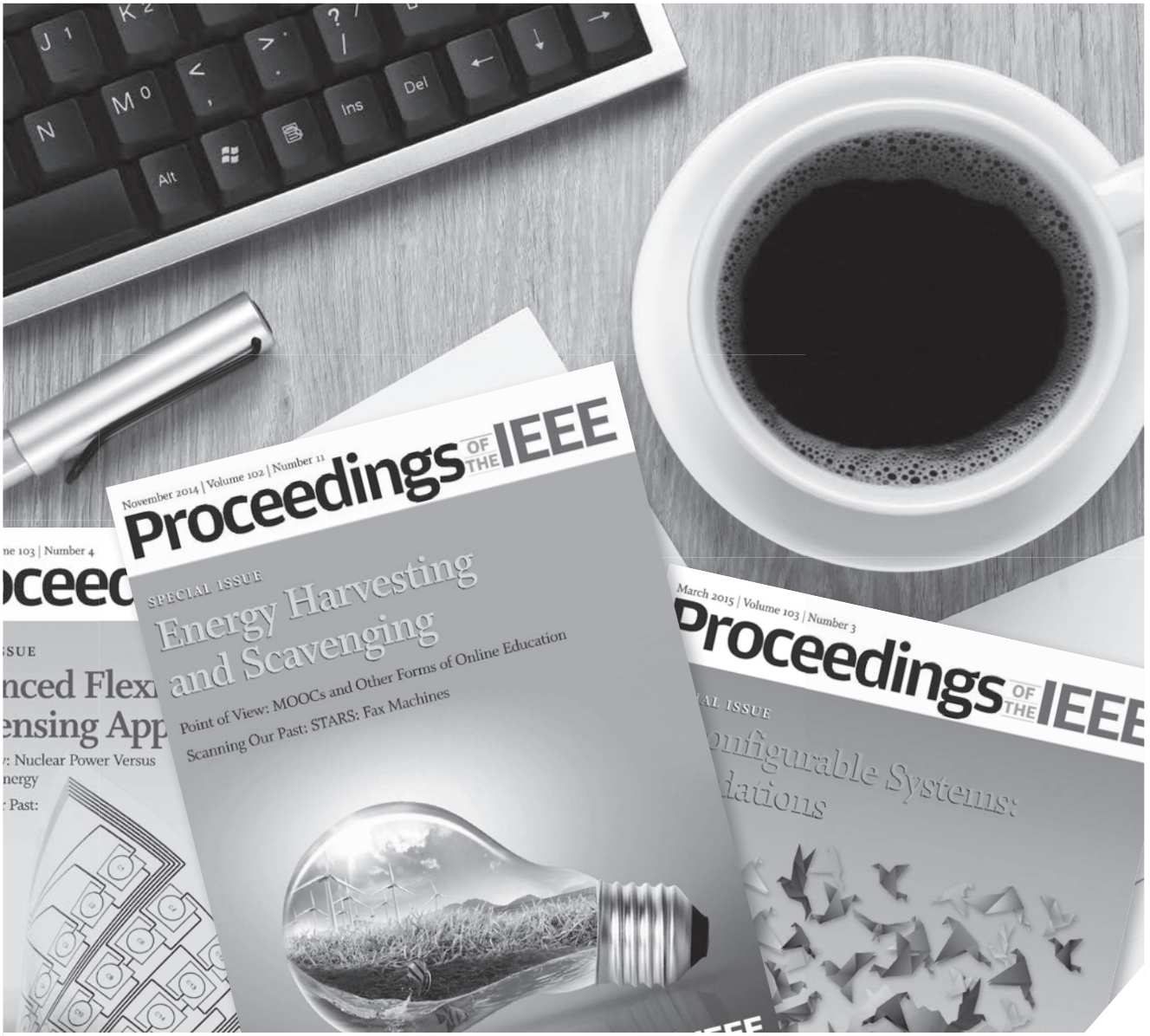

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