IEEE ELECTRONICS PACKAGING SOCIETY Newsletter

JULY 2019
VOL. 41 NO. 2
ISSN 1077-2999

Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Avram Bar-Cohen, PhD, EPS President
Principal Engineering Fellow, Raytheon—Space and Airborne Systems, Arlington, VA

Dear EPS Members:

Some 18 months ago when I became the President of the newly-named Electronic Packaging Society, I set out to accomplish several goals, including:

- Completing the name change and EPS "branding" process,
- Developing a path for the continued growth of our 3 flagship Conferences,
- Strengthening the EPS Chapters and student Branches throughout the world,
- Establishing a pathway to future Society and community leadership for young packaging professionals and other under-represented groups,
- Strongly supporting the preparation of the Heterogeneous Integration Roadmap, and
- Providing additional educational resources and credentials for our Young Professional members.

Working with the 4 primary EPS Functional Teams—Conferences, Membership, Education, and Technology, in addition to the Finance Functional Team—each led by a sitting Vice President and supported by several BOG Directors and Members-at-Large we have made dramatic progress towards each of these goals.

- The EPS name has found broad recognition and acceptance across our community. A plan is being formulated to change the name of our Transactions to TEPS and a 5-year Strategic Plan is under development; EPS now has a LinkedIn site and an informational video on EPS, which will be used in various membership development functions, is nearing completion. In 2018 EPS membership grew by almost 6%, reversing a slowly declining membership trend for the past 4 years.
- ECTC (EPS Global Flagship Conference) set attendance records in 2018 and 2019; EPTC (Asia-Pacific Flagship Conference) set an attendance record in 2018 and is developing a plan to rotate the Conference to other R10 locations; ESTC (Europe-Middle East Flagship Conference), currently on an alternate year schedule with rotation to various European cities, is developing a strategic plan to strengthen and grow the Conference. We are also developing a process for sharing popular PDC's and Best/Outstanding Papers across the 3 Flagship conferences and engaging with sponsors at all our Flagship conferences to create awareness of EPS' global footprint.
- To further engagement with the EPS Sections outside the US, the BOG held its 2018 Fall meeting at the 2018 EPTC in Singapore and is planning to hold its 2020 Fall meeting at ESTC in Norway; in 2018 and the first half of 2019 EPS added 4 new student Branches (UCLA – joint with EDS, Univ Estadual Paulista—Guaratinguetá, Brazil, Singapore University of Technology & Design, and Politehnica Univ Of Bucharest) and 1 revitalized chapter in Korea. Initial efforts are underway to also create an EPS Section in Israel.
- EPS now supports a representative to the IEEE Young Professional and IEEE Women-in-Engineering groups; BOG approved creating a dedicated Young Professional position on the Board in 2020, following the appointment of a Young Professional to a vacant Member-at-Large position in 2019; EPS organized Young Professional events at several Conferences and conducted a Young Professional Packaging Vision Contest, with the winners presenting their respective Visions at a well-attended Panel session at the 2019 ECTC.
- EPS provided financial and administrative support to the Heterogeneous Integration Roadmap team, enabling the inaugural release of the HIR later this summer.
- Earlier this year, EPS introduced a first-of-its kind Certificate program, recognizing completion of 15 Professional Development Hours, through attendance at Professional Development Courses,

(continued on page 3)

NEWSLETTER SUBMISSION DEADLINES

1 December 2019 for Winter issue 2020

15 June 2020 for Summer issue 2020

Submit all material to d.manning@ieee.org

EPS Officers

President: Avram Bar-Cohen, Raytheon, avram.bar-cohen@raytheon.com

President Elect: Chris Bailey, Univ of Greenwich, c.bailey@gre.ac.uk

VP (Technology): Patrick Thompson, Texas Instruments, patrick.thompson@ti.com

VP (Conferences): Beth Keser, Intel, beth.keser@intel.com

VP (Publications): Ravi Mahajan, Intel, ravi.v.mahajan@intel.com

VP (Education): Jeff Suhling, Auburn University, jsuhling@auburn.edu

VP (Finance): Thomas Reynolds, Murata Electronics, Retired, t.reynolds@ieee.org

VP (Membership): Alan Huffman, Micross, Alan.Huffman@micross.com

Sr. Past Pres.: Jean Trewhella, GLOBALFOUNDRIES, jean.trewhella@GLOBALFOUNDRIES.com

Jr. Past Pres.: Jie Xue, Cisco, jixue@cisco.com

Members At Large

2019 Term End: Regions 1-6, 7, 9—Li Li, David McCann, Kitty Pearsall, Subramanian S. Iyer; Region 8—Thomas Brunschwiler, Gilles Poupon

2020 Term End: Regions 1-6, 7, 9—Yan Liu, Sam Karikalan, Xuejun Fan, Patrick McCluskey; Region 8—Grace O'Malley; Region 10—Yoichi Taira

2021 Term End: Regions 1-6, 7, 9—Philip Garrou, Eric Perfecto, Pradeep Lall; Region 10—C. Robert Kao, Chih-Pin (C.P.) Hung, Kishio Yokouchi

Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:
Ravi Mahajan, Intel

Senior Area Editor Special Topics:
Ravi Mahajan, Intel

Senior Area Editor, Electrical Performance:
Dale Becker, IBM

Senior Area Editor, Components: Characterization and Modeling:
Koneru Ramakrishna, Cirrus Logic, Inc.

Senior Area Editor, Advanced Packaging Technologies:
Kuo-Ning Chiang, National Tsing Hua University

Senior Area Editor, Electronics Manufacturing:
Muhannad Bakir, Georgia Institute of Technology

Technical Committee Chairs

Materials & Processes:
Bing Dang, IBM

High Density Substrates & Boards:
Yasumitsu Orii, Nagase & Co.

Electrical Design, Modeling & Simulation:
Dale Becker, IBM

Thermal & Mechanical:
Dereje Agonafer, University of Texas at Arlington

Emerging Technology:
Karlheinz Bock, Technical University Dresden

Nanotechnology:
Americas: Raj M. Pulugurtha, Georgia Institute of Technology, Chair; Europe: Chris Bailey, Univeristy of Greenwich, Asia: Jian Cai, Tsinghua University

Power & Energy:
Patrick McCluskey, University of Maryland

RF & Thz Technologies:
Manos Tentzeris, Georgia Institute of Technology

Green Electronics:
Nils F. Nissen, Fraunhofer

Photonics—Communication, Sensing, Lighting:
Gnyaneshwar Ramakrishna, Cisco

3D/TSV:
Paul Franzon, North Carolina State University

Reliability:
Richard Rao, Microchip

Program Directors

Chapter Programs: Kitty Pearsall, IBM, Retired, kitty.pearsall@gmail.com

Awards Programs: Eric Perfecto, Independent Consultant, Eric.Perfecto.US@ieee.org

Student Programs: Andrew Tay, Singapore University of Technology & Design, andrew_tay@ieee.org

Industry Programs: William T. Chen, ASE, William.Chen@aseus.com

Region 8 Programs: Toni Mattila, Business Finland, toni.mattila@investinfinland.fi

Region 10 Programs: Yasumitsu Orii, Nagase & Co., yasumitsu.orii@nagase.co.jp

Standing Committee Chairs

Fellows Evaluation: John Lau, john.lau@asmpt.com

Long Range / Strategic Planning: Christopher Bailey, c.bailey@gre.ac.uk

Nominations: Jean Trewhella, Jean.Trewhella@globalfoundries.com

Distinguished Lecturers

Program Director: Jeff Suhling, jsuhling@auburn.edu

Lecturers: Mudasir Ahmad, Muhannad Bakir, Ph.D., Avram Bar-Cohen, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., Moises Cases, William T. Chen, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., Subu Iyer, PhD., R. Wayne Johnson, Ph.D., Beth Keser, Ph.D., John H. Lau, Ph.D., Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., Ravi Mahajan, PhD., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Michael Pecht, Ph.D., Eric D. Perfecto, Karl J. Puttlitz, Ph.D., Dongkai Shangguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

IEEE Electronics Packaging Society Newsletter is published quarterly by the Electronics Packaging Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US $1.00 per member per year is included in Society fee for each member of the Electronics Packaging Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE EPS Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854.

Circulate your printed or PDF copy of this NEWSLETTER to co-workers.

SFI Logo

Ephraim Suhir Receives 2019 IEEE Electronics Packaging Award

An IEEE Life Fellow and Professor at Portland State University.

"For seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems."

The IEEE Electronics Packaging Award, sponsored by the IEEE Electronics Packaging Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical com-munity and the profession, benefit to society, and the quality of the nomination.

With over 40 years of pioneering work in modelling and reliability engineering, Ephraim Suhir has enabled electronic packaging engineers to accurately predict stress in advanced packaged components for the design of more reliable devices. He was one of the earliest researchers to introduce the use of rigorous mechanics principles in electronic systems. His closed-form solutions have provided the electronics industry with invaluable tools for ensuring reliability and cost savings during the design process by eliminating errors early in the design process. He has applied his techniques to advanced components and packaged structures such as microelectronics, photonics, photo-voltaics, and thermoelectric modules. Every serious mechanics practitioner and researcher in the electronics packaging field has been influenced by Suhir's groundbreaking contributions.

In addition to several edited books, Suhir has authored three monographs: "Structural Analysis in Microelectronics and Fiber Optics Systems" (Van-Nostrand-Reinhold, 1991); "Applied Probability for Engineers and Scientists" (McGraw-Hill, 1997); and "Human-in-the-Loop: Probabilistic Modeling of an Aerospace Mission Outcome" (CRC Press, 2018). These monographs reflect three novel directions in applied science and engineering, in general, and in electronics and photonics packaging engineering, in particular: application of classical engineering mechanics to critical problems in electronics and photonics; use of applied probability methods in numerous engineering problems; and employment of such methods in various aerospace related missions and situations, when human performance and instrumentation/equipment reliability contribute jointly to the never-zero probability of failure of these missions and off-normal situations. His work in these critical domains has placed Dr. Ephraim Suhir in the upper 2.5% of LinkedIn Research Gate (RG) members, and generated an "all-star"-strength professional profile, with some 14,000 downloads ("reads") and over 4,000 citations of his published work. An IEEE Life Fellow, Suhir is a professor with Portland State University, Portland, OR, USA. He is also on the faculty of the Technical University, Vienna, Austria, and James Cook University, Queensland, Australia.

The 2019 Electronic Packaging Award was presented to Ephraim Suhir at the EPS Luncheon held at the 69th Electronic Components and Technology Conference (ECTC), May 2019, in Las Vegas, Nevada. David Durocher, IEEE Division II Director, presented the Award on behalf of IEEE and EPS.

Ephraim Suhir joins the recent past recipients of this Award, including William Chen (2018), Paul Ho and King-Ning Tu (2017), Michael Pecht (2016), and Nasser Bozorg-Grayeli (2015), in receiving this Award.

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www. ieee.org/awards

---

President's Column (*Continued from page 1*)

Webinars, and authoring and/or reviewing technical papers. The EPS Certificate will help distinguish the unique skills and knowledge of EPS members and will be followed by Topical Certificates and stackable Advanced Certificates in coming years; EPS also established an EPS Ph.D. Fellowship awarded for the first time at the 2019 ECTC.

I hope you will agree with me that, in the past 18 months, we have accomplished much to address our commitment to you—our members—and to the broader electronic packaging community. Please accept my personal thanks for your continued engagement with the IEEE Electronic Packaging Society and I very much hope that—after reading this update—you will not hesitate to share with me (avram.bar-cohen@raytheon.com) your assessment of our efforts. Moreover, I hope you will also find the opportunity to inform me of your interest in joining or starting a new Technical Committee, volunteering to represent EPS on one of the IEEE-wide Initiatives, or becoming a candidate for the EPS Board of Governors. It is only through such "volunteerism" by all of you that your President and Board of Governors can succeed in paving the way for future packaging technologies and continue to drive innovation in the microelectronic industry.

Avram Bar-Cohen

2019 IEEE Electronics Packaging Society Award Recipients

Jie Xue
Cisco Systems, Inc., USA

2019 IEEE CPMT Electronics Manufacturing Technology Award
For over 20 years of technical contributions to the microelectronic packaging industry.

S. W. Ricky Lee
Hong Kong University of Science and Technology (HKUST), Hong Kong

2019 IEEE CPMT Outstanding Sustained Technical Contribution Award
For two decades of continuous contributions and professional leadership in multiple technical fields encompassed by EPS, including solder joint reliability, lead-free transition, 3D IC integration, and LED packaging.

Chuan Seng Tan
Nanyang Technological University, Singapore

2019 IEEE EPS Exceptional Technical Achievement Award
For technical contributions and leadership in 3D packaging and integration, particularly on solder-less Cu-Cu bonding and innovations in TSV technology.

Andrew Tay
Singapore University of Technology and Design, Singapore

2019 IEEE EPS David Feldman Outstanding Contribution Award
For outstanding contributions in leadership in EPS conferences, chapter and Board of Governors over 28 years, notably the development of the EPS flagship Electronics Packaging Technology Conference in Region 10.

Adeel Bajwa
Klicke and Soffa (K&S), USA

2019 IEEE EPS Outstanding Young Engineer Award
For his contributions to interconnects technology, both in fine-pitch and power electronics.

Shaw Fong Wong
Intel Technology Ptd. Ltd., Malaysia

2019 IEEE EPS Regional Contributions Award—Region 10 (Asia and Pacific)
For outstanding and sustained leadership contributions to the IEEE/EPS Malaysia Chapter and to significantly engage and promote close collaboration within R10 technical activities.

SivaChandra Jangam
University of California, Los Angeles

2019 IEEE EPS PhD Fellowship
For contributions to the development of the Silicon Interconnect Fabric as a platform for the fine pitch integration of heterogeneous chips.

Packaging Vision Competition—ECTC 2019

As part of its outreach to Young Professionals, the Electronic Packaging Society sponsored a Packaging Vision 2025 competition in the Winter of 2019 and invited the winners of the Competition to present their views at the 2019 Packaging Vision Panel at the ECTC Conference. The Panel, held at 7:45 pm on Tuesday 5/28, was chaired by Avi Bar-Cohen, IEEE EPS President and Karlheinz Bock, TU Dresden and attracted close to 150 attendees.

The Vision Competition was sponsored by the EPS Emerging Technologies Committee, chaired by Prof. K. Bock of Dresden University (Germany), the effort reflected the recognition that many of our Young Professional members nurture exciting, disruptive ideas but lack the opportunity, the influence, and sometimes the sophistication to communicate these ideas in a persuasive manner. The Panel format was selected to provide Young Professionals with the opportunity to present to a technically-astute audience

and to engage with many of the leaders of the Electronics Packaging community. The Competition welcomed submissions from all IEEE Students, Graduate Students and Young Professionals and two submissions were selected as the winners:

- "Brain-on-a-Package" by Shreya Dwarakanath, Handrasekharan Nair, and Siddharth Ravichandran, from the Georgia Institute of Technology, Atlanta GA, and
- "Will Biocompatible Packaging be the First Step to Become a Cyborg?" by Martin Schubert, Technical University of Dresden, Germany

The winning students were honored at the EPS Award Luncheon at ECTC.

Congratulations to IEEE EPS Senior Members

New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between December 2018 and April 2019.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

For additional information or to apply online: https://www.ieee.org/membership/senior/

Andreas Aal, Germany Section
Richard Beyerle, Cleveland Section, USA
Harish Bhaskaran, United Kingdom and Ireland Section
Premjeet Chahal, Southeastern Michigan Section, USA
Hongsheng Chen, Zhejiang Subsection, China
John Deandrea, Philadelphia Section, USA
Takafumi Fukushima, Sendai Section, Japan
Aurel Gontean, Romania Section
Kalyani K, Podhigai Subsection, India
Ahmed Lakhssassi, Ottawa Section, Canada
Suny Li, Beijing Section, China
David Monk, Phoenix Section, USA
Ramana Pamidighantam, Hyderabad Section, India
Zhou Shudong, Guangzhou Section, China
C David Stokes, Eastern North Carolina Section, USA
Chuan Seng Tan, Singapore Section
Andrew Tay, Singapore Section
Christos Tsamis, Greece Section
Kiyokazu Yasuda, Kansai Section, Japan

ECTC 2019 Travel Award Winners

Congratulations to the winners of the 2019 ECTC travel award. The award is intended to assist students to attend ECTC.

- **Arsalan Alam**, University of California, Los Angeles
- **Muhammad Ali**, Georgia Institute of Technology
- **Claudio Alvares**, Georgia Institute of Technology
- **SivaChandra Jangam**, University of California, Los Angeles
- **Gurvinder Singh Khinda**, Binghamton University
- **Yuki Susumago**, Tohoku University
- **Tiwei Wei**, IMEC
- **Jikai Xu**, Harbin Institute of Technology
- **Tilo Hongwei Yang**, National Taiwan University

Congratulations to the ECTC Volunteer Award Recipients

The ECTC Volunteer Award is given to those individuals who contribute to the success of the ECTC by volunteering in one of the conference committees, year after year. Here are the 2019 ECTC Volunteer Award winners:

Tim Chaudhry	10 Years
Henning Schroeder	10 Years
Shogo Ura	10 Years

Stefan Weiss	10 Years
Amit Agrawal	25 Years
Luu Nguyen	25 Years

Donna M.Noctor	25 Years
Kitty Pearsall	25 Years
Raj Pendse	25 Years

EPS Major Awards Nomination Period Starts on September 15

All of the EPS Major Award nominations will be done via online submission. The nomination period to input all the required documents runs from September 15 to January 21. The Electronics Packaging Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and EP Society.

Outstanding Sustained Technical Contributions Award
To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Must have been a member of the IEEE and EP Society for the past three (3) years (2017–2019), and renewed for 2020.

Electronics Manufacturing Technology Award
To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. Work in the management of EPS Conferences or its BoG may be contributory but it is not a requirement for the award.

Eligibility: No need to be a member of IEEE and EP Society.

David Feldman Outstanding Contribution Award
To recognize outstanding contributions to the fields encompassed by the EP Society through executive or managerial directions.

Prize: $2,500 and Certificate

Basis for Judging: Contributions to the organizations or enterprises connected with the field; contributions to EPS Chapter or Board of Governors activities; contributions to the fields encompassed by the EP Society.

Eligibility: Recipient must have been a member of IEEE and EPS for the past five (5) years (2015–2019), and renewed for 2020.

Exceptional Technical Achievement Award
To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the EP Society.

Prize: $2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in EPS's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for the past three (3) years (2017–2019), and renewed for 2020. There are no requirements for service to the IEEE or EP Society.

Outstanding Young Engineer Award
To recognize outstanding contributions to the fields encompassed by the EP Society through invention, technical development, publications, or new product implementation.

Prize: $1,500 and Certificate

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the EPS Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Must have been a member of the IEEE and EPS (member grade or above) for the past three (3) years (2017–2019), and renewed for 2020, and must be 35 years of age, or younger, on December 31, 20120.

Guidelines for Nominators:

- A recipient of any EPS Major Award will be eligible for nomination for another EPS Major Award *after two award cycles have passed*. (i.e., Recipient of XX Award in 2017 becomes eligible for nomination for YY Award in 2020). For lists of past awardees, see http://eps.ieee.org/awards.html
- Past recipients of an award are not eligible to receive that same award. For lists of past awardees, see http://eps.ieee.org/awards.html
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- An individual may submit only one endorsement per award but may submit endorsement for more than one award.
- It is the responsibility of the nominator to ensure quality documentation to assist the Awards Committee in evaluating the candidate.
- Outstanding Sustained Technical Contribution Award is designed for the "practitioner", while the Electronics Manufacturing Technology Award intended for "Corporate Leadership".
- Complimentary material, such as candidate's picture, CV, list of publications and/or patents should be submitted separate from the award nomination.
- Self-nominations **will not** be considered.

EPS PhD Fellowship:
To promote, recognize, and support PhD level study and research within the Electronics Packaging Society's field of interest.

Prize: A plaque and a single annual award of US$5,000, applicable towards the student's research.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electronic packaging and a proven history of academic excellence, as documented in:

- Nomination by an IEEE EPS Member. Only one nomination per member per year.
- Two-page (maximum) statement by the student describing his or her education and
- Research interests, accomplishments, and impact on the electronics package industry.
- Proof of contributions to the community may consist of open literature publications (preferred) such as papers, patents, books, and conference presentations and reports (available to the public).
- At least one letter of recommendation from someone familiar with the student's work
- Student resume

Eligibility: Candidate must be an IEEE EPS member, at the time of nomination, and be pursuing a doctorate degree within the EPS field of interest on a full-time basis from an accredited graduate school or institution. The candidate must have studied with her/his advisor for at least 1 year, at the time of nomination, to be eligible. A Student who received a Fellowship award from another IEEE Society, within the same year, or is a previous EPS Fellowship winner is ineligible.

All Award nominations must be **online**. Nominations questions can be sent to the Society Awards Program director:

Eric Perfecto
Eric.Perfecto.US@ieee.org

Winners will be notified by April 2020, and the awards will be presented at the 70th Electronic Components and Technology Conference (ECTC), May 26–29, 2020 at the Swan & Dolphin Walt Disney World Resort, Orlando, FL, USA

Heterogeneous Integration Roadmap (HIR) Workshop at ECTC 2019

The HIR Workshop at ECTC on May 28th presented the first public release of material from the 2019 Edition of the HIR. There are 19 presentations which are summary materials from the 2019 edition of the HIR. These will be followed by a rolling release of the full chapters as the peer review process is completed. The summary presentations are available on line at https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2019-edition.html. There were more than 100 participants at the HIR workshop and the event was celebrated with a cake cutting at the end.

In 2019, there has been over 500 attendees have participated in HIR events across the world to date. There are additional events scheduled for the remainder of the year. Please visit the HIR page on the EPS website for a full listing—https://eps.ieee.org/hir.

EPS President, Avram Bar-Cohen cutting the cake to celebrate the first release of the Heterogeneous Integration Roadmap (HIR), joined by contributing members of the HIR.

YP Event at ECTC 2019

The IEEE Young Professional and Graduate Student Survey showed that networking and education are top improvement opportunities among Young Professionals. This year, EPS continues to focus on improving networking opportunities and providing career services to young professional members.

EPS is planning different types of YP meet up events like panel discussion, seminars, and receptions in conferences as well as at meetings of local Sections. Recently, the 2nd ECTC/ITherm Young Professionals networking event took place at Las Vegas on May 28, 2019. Yan Liu, the Electronic Packaging Society Young Professional Representative hosted this event, to connect EPS senior members and young professionals/students. 15 EPS Board of Governor members and more than 60 young professionals joined this event. Each BoG member designed a special EPS trading card, which includes their picture, contact information, employment, technical interest, hobbies etc. During the event, young professionals talked to each senior member and collected their trading cards. This event also provided the information about EPS career service as member resources, including IEEE Mentoring Program, Jobsite and Resume Lab. We would like to thank the funding support from IEEE Young Professional, as well as the great support from EPS Board of Governors and ECTC/ITherm committees.

Yan Liu, EPS BoG member

2019 ECTC Young Professional Networking Event Picture.

2019 ECTC Young Professional Networking Event: EPS Board of Governor Panels, and Their Trading Cards.

As we find ourselves at the beginning of a new year and a new university term full of opportunities, we want to introduce you to our initiative in raising academic awareness amongst future engineers.

Who are "we"? If you didn't get the chance to visit our site (https://edu.ieee.org/ro-upb/), we invite you to discover us as the University of Politehnica Student Chapter of the IEEE Electronics Packaging Society, which formed as a consequence of our vision and wish of changing the academic electronics environment.

Take a look at what we've done to help the community and raise awareness, as one of our first activities as a Student Chapter team.

SIITME Conference: Due to our focus on providing members with opportunities for networking with other students, faculty, and professionals at technical meetings and social events, we encouraged our members to participate at the IEEE 24th International Symposium for Design and Technology in Electronic Packaging. Therefore, on the 27th of Oct, 2018, three of our members presented their first scientific papers.

DA-SPACE-Open Innovation to Raise Entrepreneurship Skills and Public Private Partnership in Danube Region: In the context of our first official EPS meeting, on 29th of November, 2018, we were informed about DA-SPACE, which is a sub-project of the European Interreg project. On the 12th of Dec, 2018, we went to Galati and had our first workshop, as well.

Faculty's open day-As a EPS member, it is our job to coordinate and give future possible engineers a walk-through of our student experience and to objectively present them what the electronics industry might be able to offer. Therefore, on the 5th of Dec, 2018, we took party in the faculty's Open Day activities, as part of final year high-schoolers recruitment in our university.

As for some of the future events, where our team intends to participate and represent the Student Chapter, we present you TIE.

The INTERCONNECTION TECHNIQUES IN ELECTRONICS (TIE) contest is a student professional contest whose objective is to promote technological computer aided design of printed circuit boards and electronic modules. If we caught your attention and you want to know more about the stages or information about the contest, you can find it out more on http://www.tie.ro/.

Follow our newsletter for future projects and events that are coming soon.

PUBLICATION NEWS

2018 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 200 published papers and represent the best, based on criteria including originality, significance, completeness and organization. The awards were presented at the 69th Electronic Components and Technology Conference (ECTC), May 2019.

Subscribers to this publication can access the papers on-line in IEEE Xplore at:

http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870

Components: Characterization and Modeling Category

"Mechanical Reliability of Thick-Film Materials for High Temperature Packaging"
VOL. 8, ISSUE 6, JUNE 2018
Zhangming Zhou, R. Wayne Johnson, Michael C. Hamilton

Abstract: High-temperature electronics are required to reliably operate at 300 °C in gas and oil exploration and downhole drilling for geothermal energy applications. Advances in SiC and GaN devices enabled these applications. Reliable interconnect materials and technology are necessary to build functional circuits in high-temperature packaging. This paper investigated the mechanical reliability of two thick-film conductors (PtPdAu and Au) and two dielectrics at 300 °C with bias. Test vehicles (TVs) were fabricated with thick films as capacitors and aged at 300 °C with a 100-V bias. For the TVs fabricated with PtPdAu and thin dielectrics, adhesion degradation was first observed after 100-h aging with positive bias voltage applied on the top electrode. The adhesion remained relatively constant when vehicles were aged with positive bias voltage applied on the bottom electrode. Increasing the dielectric thickness or reducing the Bi concentration in PtPdAu delayed the first observed adhesion degradation from 100 to 500 h. Aging with alternating polarities also resulted in adhesion degradation. In all tests, no adhesion degradation was observed with the thick-film Au, which did not contain Bi.

URL: https://ieeexplore.ieee.org/document/8365089

AND

"Integrated Sensor System for DNA Amplification and Separation based on Thin Film Technology"
VOL. 8, ISSUE 7, JULY 2018
Francesca Costantini, Giulia Petrucci, Nicola Lovecchio, Marco Nardecchia, Augusto Nascetti
Giampiero de Cesare, Lorena Tedeschi, Claudio Domenici, Albert Ruggi, Pisana Placidi, Andrea Scorzoni
Domenico Caputo

Abstract: This paper presents the development of a lab-on-chip, based on thin-film sensors, suitable for DNA treatments. In particular, the system performs on-chip DNA amplification and separation of double-strand DNA into single-strand DNA, combining a polydimethylsiloxane microfluidic network, thin-film electronic devices, and surface chemistry. Both the analytical procedures rely on the integration on the same glass substrate of thin-film metal heaters and amorphous silicon temperature sensors to achieve a uniform temperature distribution (within ±1 °C) in the heated area and a precise temperature control (within ±0.5 °C). The DNA separation also counts on the binding between biotinylated dsDNA and a layer of streptavidin immobilized into a microfluidic channel through polymer-brushes-based layer. This approach results in a fast and low reagents consumption system. The tested DNA treatments can be applied for carrying out the on-chip systematic evolution of ligands by exponential enrichment process, a chemistry technique for the selection of aptamers.

URL: https://ieeexplore.ieee.org/document/8279487

To recognize the work and efforts of our Associate Editors, EPS instituted the Best Associate Editor Award. The 2019 recipients are

Hsien-Chie Cheng, Feng Chia University
Wen-Yan Yin, Zhejiang University
Tzong-Lin Wu, National Taiwan University
John McBride, University of Southampton
John Shea, Schneider-Electric
Bing Dang, IBM T. J. Watson Research Center

T-CPMT Reduces "Sub to Online Post"

Thanks to sustained efforts of the entire Editorial committee, the T-CPMT has recently achieved a significant reduction in its paper review turnaround time. The 2019 First Quarter "Submission to Publication Report" indicates that the average duration for TCPMT from paper submission to online post is 22.2 weeks. This is almost 11 weeks faster than reported in the 2018 Second Quarter Report. Relevant statistics:

1st Quarter 2019:
Avg Weeks to First Decision 12.1
Avg. Weeks Submitted to Online Post 22.2

2nd Quarter 2018:
Avg Weeks to First Decision 13.6
Avg. Weeks Submitted to Online Post 33.0

5 Most Popular Articles According to May 2019 Usage Statistics

These are the top 5 most frequently accessed articles in T-CPMT based on Xplore usage data.

3-D Printed Metal-Pipe Rectangular Waveguides
Mario D'Auria; William J. Otter; Jonathan Hazell; Brendan T. W. Gillatt; Callum Long-Collins; Nick M. Ridler; Stepan Lucyszyn
Publication Year: 2015, Page(s): 1339–1349

Reliability Evaluation of SiC Power Module With Sintered Ag Die Attach and Stress-Relaxation Structure
Kazuhiko Sugiura; Tomohito Iwashige; Kazuhiro Tsuruta; Chuantong Chen; Shijo Nagao; Tsuyoshi Funaki; Katsuaki Suganuma
Publication Year: 2019, Page(s): 609–615

Die Attach Materials for High Temperature Applications: A Review
Vemal Raja Manikam; Kuan Yew Cheong
Publication Year: 2011, Page(s): 457–478

Power Noise and Near-Field EMI of High-Current System-in-Package With VR Top and Bottom Placements
Kan Xu; Boris Vaisband; Gregory Sizikov; Xin Li; Eby G. Friedman
Publication Year: 2019, Page(s): 712–718

Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging
John H. Lau; Ming Li; Dewen Tian; Nelson Fan; Eric Kuah; Wu Kai; Margie Li; J. Hao; Yiu Ming Cheung; Zhang Li; Kim Hwee Tan; Rozalia Beica; Thomas Taylor; Cheng-Ta Ko; Henry Yang; Yu-Hua Chen; Sze Pei Lim; Ning Cheng Lee; Jiang Ran; Cao Xi; Koh Sau Wee; Qingxiang Yong
Publication Year: 2017, Page(s): 1729–1738

EDUCATION/CAREER NEWS

EPS Certificate of Achievement

In order to further the education of Electronics Packaging Society (EPS) members, the EPS is now offering a Certificate Program. The goal of the program is to give members new to electronics packaging an opportunity for further packaging education, offer continuous education in electronics packaging to existing members, and also to offer students electronics packaging training if they are in a University program that does not include packaging education.

Criteria: Must be an IEEE Electronics Packaging Society Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of EPS Webinars, Professional Development Courses at select EPS Conferences, author of IEEE T-CPMT paper and/or EPS Conference paper, reviewer for IEEE T-CPMT.

Once you have completed any combination of the above and received 15 PDHs, please complete the certificate form to request your Electronics Packaging Society Certificate.

Congratulations to these EPS Members on receiving the IEEE Certificate of Achievement from the IEEE Electronics Packaging Society and completing the required number of professional development hours.
Jinto George, University of Sherbrooke, Canada
Arkaprovo Das, Simyog Technology Pvt. Ltd., India
Chuan Seng Tan, Nanyang Technological University, Singapore
Koushik Ramachandran, GLOBALFOUNDRIES, USA
Jonas Zuercher, ESPROS Photonics AG, Switzerland
David Dahl, Hamburg University of Technology, Germany
Prof. Shashikant Patil, SVKMs NMIMS Shirpur Campus, India
Eric Perfecto, Independent Consultant, USA
Beth Keser, Intel, USA

EPS Distinguished Lecturers are selected from among EPS Fellows, Award winners, and Society leaders, who are members of the technical community and experts in their field. They are available to present lectures and/or courses at EPS events—Chapters, Conferences, Workshops or Symposia; as well as IEEE Student Chapter events.

The EPS Distinguished Lecturer Program (DLP) aims at serving communities interested in the scientific, engineering, and production aspects of materials, component parts, modules, hybrids and micro-electronic systems for all electronic applications.

The Program strives to support EPS Chapters worldwide by helping them to invite leading researchers in their respective fields and IEEE Student Chapters to encourage students to pursue EPS related fields and to join the EPS society. The DLP talk is a major event in the life of the inviting Chapter.

EPS Distinguished Lecturers

Mudasir Ahmad (2017–2021)
Cisco Systems, Inc. San Jose, CA USA
Topics: Internet of Things (IoT), Advanced Packaging, 2.5D, Heterogeneous Silicon Photonics, Advanced Reliability (Thermo-mechanical, Mechanical Shock), Numerical Modeling, Advanced Thermal Solutions, Stochastic Analysis, Bayesian Inference, Machine Learning, Artificial Intelligence

Muhannad Bakir, PhD. (2015–2019)
Georgia Institute of Technology, Atlanta, GA USA
Topics: Emerging interconnection architectures and technologies; heterogeneous system design and integration

Avram Bar-Cohen, PhD. (2015–2019)
University of Maryland, College Park, Maryland USA
Topics: Thermal packaging

Karlheinz Bock, PhD. (2016–2020)
Technische Universität, Dresden, Germany
Topics: Multifunctionality & heterosystemintegration & additive manufacturing (IoT, Industry 4.0, tactile internet…), packaging for mechanical, digital and power co-integration (automotive, machines, robots..),2.5D and 3D electro-optical-RF interposer and board (high performance), heterointegration for flexible, bio, organic and large area electronics (open form factor)

Bill Bottoms, PhD. (2017–2021)
Third Millennium Test Solutions, Santa Clara, CA USA
Topics: Heterogeneous Integration, Semiconductor test technology, Emerging research materials, Packaging of electronic components and systems, the global network and its future requirements, the internet of things and Smart manufacturing

Chris Bower, PhD. (2017–2021)
X-Celeprint Inc. North Carolina, USA
Topics: novel assembly methods, elastomer stamp micro-transfer-printing, heterogeneous integration, three-dimensional integration, manufacturing of micro-assembled displays and other large-format electronics

Moises Cases (2015–2019)
The Cases Group, LLC, Austin, Texas, U.S.A.
Topics: Signal and power distribution integrity for complex high-speed multiple board system designs; Modeling, simulation and verification of integrated circuits, electronic packages and system interconnect technologies; High-speed and low powers systems interconnect design methodology and tools; Digital system electrical designs, timings and integration; High-speed I/O architectures and designs; Service science management and engineering applied to engineering services

William T. Chen, PhD. (2015–2019)
ASE (U.S.) INC
Santa Clara, CA USA
Topics: Semiconductor and Electronics Industry Trends and Roadmap

Xuejun Fan, PhD. (2015–2019)
Lamar University, Beaumont TX USA
Topics: Design, modeling and reliability in micro-/nano- electronic packaging and microsystems

Paul D. Franzon, PhD. (2015–2019)
NC State University, Raleigh, NC USA
Topics: 3DIC and 3D Packaging Application,Design and CAD; I/O Macromodeling, including IBIS; High-Speed, Low Power Chip to Chip Communications

Philip Garrou, PhD. (2015–2019)
Microelectronic Consultants of North Carolina, Research Triangle Park, NC USA
Topics: Thin film technology; IC packaging and interconnect; Microelectronic materials; 3D-IC integration

Subu Iyer, PhD. (2017–2021)
University of California, Los Angeles, Los Angeles, CA USA
Topics: Heterogeneous Integration; Flexible hybrid electronics; 3D interposer, and wafer scale integration and stacking

R. Wayne Johnson, PhD. (2015–2019)
Tennessee Tech University, Cookeville, TN USA
Topics: Extreme Environment Electronics

Beth Keser, PhD. (2015–2019)
Intel, Neubiberg, Germany
Topics: Fan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; photoimageable liquid polymer films

John H. Lau, PhD. (2015–2019)
4ASM Pacific Technology, Hong Kong
Topics: Electronics and Photonics 2D and 3D packaging and manufacturing

Ning-Cheng Lee, PhD. (2015–2019)
Indium Corporation of America, Clinton, NY USA
Topics: Lead-free soldering including solderalloys, surface finishes, components, substrates, and other materials; Processes,reliability, failure modes, and troubleshooting;Advanced applications including packaging, and ultra-fine pitch applications

S. W. Ricky Lee, PhD. (2015–2019)
Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong
Topics: Solder Joint Reliability, 3D IC Integration, and LED Packaging

Johan Liu, PhD. (2015–2019)
Chalmers University of Technology, Gothenburg, Sweden
Topics: Micro and nano-electronic electrically conductive adhesives

Ravi Mahajan, PhD. (2016–2020)
Intel Corporation, Arizona, USA
Topics: Advanced Packaging Architectures, Assembly Processes and Thermal Management

James E. Morris, PhD. (2015–2019)
Portland State University, Portland, Oregon USA
Topics: Electrically conductive adhesives; Electronics packaging; Nanotechnologies

Kyung W. Paik, PhD. (2015–2019)
Korea Advanced Institute of Science & Technology,
Daejon, Korea
Topics: Electrically conductive adhesives (ACF, NCF, ACP, NC)

Mervi Paulasto-Kröckel, PhD. (2016–2020)
Aalto University, Helsinki, Finland
Topics: MEMS, electronics reliability, automotive components and packaging, implantable electronics, dissimilar materials & interfaces

Michael Pecht, PhD. (2015–2019)
University of Maryland, College Park, MD USA
Topics: Prognostics and reliability of electronic products and systems

Eric D. Perfecto, PhD. (2015–2019)
Independent Consultant, Poughkeepsie, NY USA
Topics: Fine pitch interconnect, chip to chip and chip to laminate connection, UBM and solder selection, chip package interaction and 2.5D fabrication

Karl J. Puttlitz, PhD. (2015–2019)
Puttlitz Engineering Consultancy, LLC, Wappingers Falls, NY USA
Topics: Flip Chip Issues/Technology; Area Array(1st & 2nd Level) Issues/Technology; Lead-free Issues/Technology

Dongkai Shangguan, PhD. (2015–2019)
National Center for Advanced Packaging Co., LTD., Wuxi, China
Topics: Materials, reliability, lead-free, microelectronics packaging, board assembly, electronics manufacturing

Nihal Sinnadurai, PhD. (2015–2019)
Suffolk, UK
Topics: Accelerated Ageing for Reliability Assurance-theory and practical methods—including HAST (my invention originally); The use of encapsulation and plastic packaging and reliability evaluation method; PCB & Hybrid technologies; Thermal management and design

Ephraim Suhir, PhD. (2015–2019)
Los Altos, CA USA
Topics: Accelerated life testing; Probabilistic physical design for reliability; Bonded assemblies; Thermal stress; Predictive modeling; Fiber optics structures: design for reliability; Dynamic response to shocks and vibrations

Rao Tummala, PhD. (2015–2019)
Georgia Institute of Technology, Atlanta, GA USA
Topics: Electronics Packaging

Walter Trybula, PhD. (2015–2019)
Trybula Foundation, Inc., Austin, TX USA
Topics: Emerging Technology, Advanced Lithography, Nanotechnology, Nano manufacturing, Nanomaterials, Environmental issues of Nanotechnology, Business Requirements of Nanotechnology

E. Jan Vardaman, PhD. (2015–2019)
TechSearch International, Inc., Austin, TX USA
Topics: International developments in semiconductor packaging, manufacturing and assembly; SiP: Business and technology Trends; drivers in advanced packaging; Flip chip and wafer level packaging

Paul Wesling (2015–2019)
Saratoga, CA USA
Topics: Using Xplore, and Google Scholar to Mine IEEE's Online Repository of Technical Information; Origins of Silicon Valley and the EPS

C.P. Wong, PhD. (2015–2019)
Georgia Institute of Technology, Atlanta, GA, USA
Topics: Materials

Jie Xue, PhD. (2015–2019)
Cisco Systems, Inc, San Jose, CA, USA
Topics: Advanced Packaging for Networking Application; Impact of Internet of Everything (IoE) to Semiconductor Industry ecosystem; High performance substrate technologies; Trends and challenges of Silicon Photonics for datacenter and networking applications

Kishio Yokouchi, PhD. (2015–2019)
Fujitsu Interconnect Technologies Ltd., Nagano City, Nagano, Japan
Topics: Thermal management technologies; Embedded passive component technologies; Chip to chip optical interconnection technologies

The 69th ECTC—Another Stellar Year in Las Vegas

This year's IEEE Electronic Components and Technology Conference (ECTC) was held at the Cosmopolitan Hotel in Las Vegas, Nevada from May 28 to 31. The conference brought together a total of 1,563 industry professionals, academics, and students in attendance from 25 countries.

The general attendance was the second highest following the 2018 ECTC. The professional development courses on Tuesday broke the record for attendance with 516 attendees. There were 44 sponsors with 100% retention from last year's ECTC in San Diego. The sponsorship revenue broke the record with an astounding 39% increase over the previous record set in 2018. The strong industry support is yet further evidence of ECTC's status as the world's leading packaging conference. The conference featured 358 papers in 36 oral sessions and 5 interactive poster sessions. Five special sessions on specific technical focus areas and two networking receptions with invited panelists were held. The ECTC Technology Corner showcased a multitude of product and service vendors covering the entire advanced packaging technology space. Once again this year, exhibitor booth space was fully sold out early in the conference year which underscores the critical role that packaging and interconnect technologies play in the microelectronics world.

2019 ECTC Panel Session was chaired by Avi Bar-Cohen, the IEEE EPS President, and Karlheinz Bock, TU Dresden, titled "Future (Visions) of Electronic Packaging.

The excellent event management team for the 69th ECTC.

The preparations for the next ECTC starts as soon as the current ECTC ends. Abstract submission begins in August with due date in mid-October. Unlike most conferences, the technical subcommittees for the ECTC meet up for abstract review and decisions on acceptance/rejection in the first week of November. The 69th ECTC followed the same schedule; reviews started in October with more than 200 professional volunteers serving in the technical subcommittees. A total of 549 submitted abstracts were reviewed leading to acceptance of 358 papers. In the 2019 ECTC, 54% of the submitted abstracts came from academia and research institutions, and the rest (46%) from the industry. A total of 25 countries were represented further demonstrating the strong international flair of the conference.

Technical Program Committee gathered in Dallas, Texas for the 2-day annual planning meeting on November 8 and 9, 2018 for the development of the conference program. The executive committee and the technical subcommittees, more than 100 professional volunteers, worked together to form sessions of great interest and relevance. The session chairs communicated with the authors of the accepted abstracts, and reviewed each submitted manuscripts for technical quality and timely completion. The IEEE Computer Society Conference Publishing Services was used to receive and process manuscripts accompanied with the IEEE CrossCheck system to ensure high level of original content.

ECTC kicks off on the Tuesday after the Memorial Day, prior to the commencement of technical sessions that are slated to begin on Wednesday. First day features the professional development courses (PDCs), special sessions, and workshops. The ECTC 2019 delivered a total of 18 PDCs, nine in the morning and the other nine in the afternoon, with an all-time record breaking 516 attendees. The courses covered a diverse set of topics that focused, among others, on fundamentals such as Flip Chip Technologies and Wafer-Level Chip-Scale Packaging, on latest technology such as Polymers and Nanocomposites for Electronic and Photonic Packaging, and on modeling for reliability. Seven of the 18 PDCs were new, speaking to the dynamism and relevance of ECTC PDCs.

Concurrent with the PDCs, on Tuesday, ECTC 2019 also held the all-day Heterogeneous Integration Roadmap Workshop. The workshop was moderated by industry leaders William Chen of ASE, Bill Bottoms of 3MT, and Ravi Mahajan of Intel. The workshop coincided with the completion of the first edition of the Roadmap; Technical Working Groups reported out their work products and their plans for the next edition. Heterogeneous Integration Roadmap Workshop covered topics of high interest such as 5G, Artificial Intelligence (AI), Internet of Things (IoT), and Internet of Everything (IoE).

Tuesday also featured two special sessions and one evening plenary panel on Tuesday. The first special session, titled "Transient Electronics: A Green Revolution for Packaging?," took place between 9:00 and 11:30 AM, and was moderated by Hong Yeo of Georgia Institute of Technology, and Mikel Miller of EMD Performance Materials. Guest speakers were John Rogers from Northwestern University, Paul Kohl from Georgia Institute of Technology, and Mihai Irimia-Vladu from Joanneum Research Forschungsgesellschaft, mbH. The session provided intriguing concepts of novel materials, processes, and packaging technologies

are being developed to realize a new class of sensors and electronics that can degrade or vanish on command. The speakers shared their thoughts on the use of Transient Electronics in defense, intelligence, and applications focusing on electronic waste.

The second special session of Tuesday was hosted by Rena Huang of Rensselaer Polytechnic Institute, and Soon Jang of ficonTEC Corporation. The title of the session was "Photonics on the Cutting-Edge of Technology" with the goal of capturing the latest technology advancements in the fast evolving photonics areas. Panelists were Jason Eichenholz, Luminar Technologies, Inc., Charles Kuznia, Ultra Communication, Inc., Roy Mead, Ayar Labs, Bert Offrein, IBM Research, and Mark Thompson, PsiQuantum. Discussions focused on optical neuromorphic computing, Si photonics for optical quantum computing, heterogeneous integration, advanced LiDARs for autonomous vehicles, and optical time domain reflectometer (OTDR) integration into fiber optic transceivers.

The President's Panel was held on Tuesday evening at 7:45 p.m., chaired by Avi Bar-Cohen, IEEE EPS President; and Karlheinz Bock, TU Dresden with the title "Future (Visions) of Electronics Packaging." The panel explored the future path of packaging science and technology and proposed possible scenarios for 2025. Panelists Shreya Dwarakanath, Chandrasekharan Nair, and Siddharth Ravichandran, Georgia Institute of Technology focused on "Brain-on-a-Package" while panelist Martin Schubert, TU Dresden shared his thoughts on whether biocompatible packaging will be the first step to become cyborg.

Tuesday provided two networking opportunities. The first networking event was sponsored by Texas Instruments as the ECTC Student Reception. Student attendees of ECTC 2019 took advantage of the opportunity to mingle and network with industry leaders, in hopes of getting guidance for their job search. It is worth noting that the IEEE EPS has awarded 10 students travel awards towards their expenses for attending ECTC 2019 for the first time this year. The second one, 2019 Young Professionals Panel and Reception, was chaired by Yan Liu of Medtronic and organized in conjunction with the co-located EPS ITHERM Conference. The panel paired young professionals and students with IEEE Electronic Packaging Society Board of Governors members providing an excellent opportunity to network.

Annual General Chair's Speakers Reception took place during 6–7 p.m., allowing speakers and session chairs to socialize prior to the start of the technical presentations the next day.

At the beginning of each day, the Speakers' Breakfast takes place. In addition to providing good food and various beverages, the breakfast serves as preparation of all involved for what is ahead during the day. The Tuesday breakfast was hosted by the ECTC PDC Chair Kitty Pearsall who delivered important information to the PDC instructors and proctors. On Wednesday, Thursday and Friday, the ECTC 2019 Program Chair Nancy Stoffel, hosted the breakfast, and provided instructions and guidance to the speakers and session chairs.

The technical sessions started on Wednesday following the ECTC tradition of six sessions running in parallel, both in the morning and in the afternoon each day. Wednesday morning sessions were "Wafer-Level Fan-Out Process Integration," "Next-Generation Wirebonding and Die Attach," "RDL and Additive Manufacturing," "Advancements in Automotive and Power Devices," "Bonding Manufacturing Technologies," and "Emerging Flexible Hybrid Electronics."

The 2019 ECTC Executive Committee members from left to right: Rozalia Beica/DuPont, Assistant Program Chair, Nancy Stoffel/GE, Program Chair, Christopher Bower/X-Celeprint Inc. Vice General Chair, and Mark Poliks/Binghamton University, General Chair.

John Rogers (left), Director of Center for Bio-Integrated Electronics, Northwestern University, receives a recognition award as a Keynote Speaker from Mark Poliks (right) from Binghamton University, 69th ECTC General Chair.

Patrick Thompson/Texas Instruments hosting the ECTC Student Reception.

In the afternoon the following topics were covered "Advances in Flip Chip Packaging," "Material and Process Trends in FOWLP and PLP," "Wearables and Thin-Package Reliability and Chip Package Interaction," "Dicing and Encapsulation Technologies," "Automotive and Harsh-Environment Reliability," and "Advanced Photonic Devices and Packaging." The wafer level fan-out attracted large number of professionals. The ECTC Mobile App was the only platform for rating the presentations/papers during the ECTC 2019.

Young Professionals Panel and Reception provided ample opportunity for networking.

Speakers' Breakfast—Nancy Stoffel (in the back) providing guidelines to speakers and session chairs.


Luncheons provided further opportunity to strengthen the packaging community bonds including the Women's Networking table.

The ECTC Luncheon Keynote Speech was delivered by John Rogers from Northwestern University. Prof. Rogers summarized the key ideas and presented specific examples in wireless monitoring for neonatal intensive care, and in capture, storage, and biomarker analysis of sweat, in his talk titled "Soft Electronic and Microfluidic Systems for the Skin." Prof. Rogers explained how these state-of-the-art devices can integrate with the skin in a physically imperceptible fashion to provide continuous, clinical quality information on physiological status. His talk was inspiring and intellectually stimulating. Following the Keynote Speech, awards for best and outstanding papers, both in oral presentation sessions and interactive sessions, from ECTC 2018 were presented by the ECTC 2019 Vice General Chair, Chris Bower.

The Cosmopolitan, Las Vegas, allowed the parallel sessions, Interactive Presentations, and exhibits to be in a continuous line, making it convenient for attendees to switch back and forth between these activities. The Technology Corner exhibits were thus well-attended. Both the exhibitors and the attendees reported a high level of satisfaction about their exhibit experience. On Wednesday evening, the exhibitors hosted a reception, providing further opportunities for future business relationships and collaborations.

One of the many unique gems that ECTC offers is the Interactive Presentations sessions in which the speaker and the audience find efficient communication platform that is decided by the individual participants. The Interactive Presentation sessions this year were also highly regarded for their quality and the alternative delivery they offered. There were five Interactive Presentations sessions, morning and afternoon on Wednesday and Thursday, and morning Student Interactive Presentations session on Friday.

Continuing from the inaugural panel and reception in ECTC 2018, ECTC / ITHERM Women's Panel and Reception was held Wednesday evening during the ECTC 2019. The panel was hosted by Kristina Young-Fisher, GLOBALFOUNDRIES, and Christina Amon, University of Toronto. This year's topic was "Unleashing the Power of Diversity in Our Workforce," carrying the discussion to include diversity in addition to women in workplace. The panel included a stellar line up in Monica Jackson, GE Aviation, Dereje Agonafer, a member of National Academy of Engineering, University of Texas at Arlington, Jean Trewhella, GLOBALFOUNDRIES and past CPMT President, and Rolf Achenbrenner, Fraunhofer IZM. The conversation included unique perspectives from these distinguished panelists on the power of diversity in a high performing workplace, strategies to build a diverse workforce, and tools for inclusion and engagement. While the panel discussed the creation of policies and programs to increase representation along with metrics to assess progress throughout career progression, and associated challenges, the question and answer portion at the end of the panel was highly active with attendee participation. Due to this high interest and mutually active conversation, the panel ran significantly longer than the scheduled duration. This year's ECTC / ITHERM Women's Panel and Reception demonstrated the importance of the topics discussed and made sure the conversation will continue in the 70th ECTC in Orlando, Florida.

The ECTC Plenary Session on Wednesday evening, Chaired by Tanja Braun, Fraunhofer IZM, was titled "Sensors and Packaging for Autonomous Driving." The key expert panelists on this topic were Scott Chen, Advanced Semiconductor Engineering,

Inc., Przemyslaw Jakub Gromala, Robert Bosch GmbH, Tu-Anh Tran, NXP Semiconductors, and Nathan Brese, DuPont. The advances in automotive infrastructure and communication technologies in combination with the artificial intelligence provided the backdrop. The discussion focused on the challenges and demands for sensors and packages for autonomous driving along the value chain.

The technical sessions during the morning of Thursday included "Technologies Enabling 3D and Heterogeneous Integration," "Fine-Pitch Solderless Bonding," "High-Bandwidth Packaging," "Advanced Materials for High-Speed Electronics," "Materials and Design for Reliability of Next-Generation Packages," and "Warpage and Material Performance." The Thursday afternoon sessions covered "MEMS, Sensors, and IoT," "Fan-Out and Heterogeneous Integration," "5G, mm-Wave, and Antenna-in-Package," "Advanced Substrates and Interconnect Technology," "High-Bandwidth 3D and Photonic," and "Advancements in Solder Joint Characterization and Reliability Evaluation."

The IEEE EPS Society President, Avi Bar-Cohen, hosted the luncheon on Thursday and presented the EPS Society Awards. The recipients were presented with a plaque and received warm applause from the audience. Ephraim Suhir, Portland State University, was awarded the IEEE EPS Technical Field Award For seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems.

ECTC / ITHERM Women's Panel and Reception hosted by Kristina Young-Fisher, GLOBALFOUNDRIES, and Christina Amon, University of Toronto. This year's topic was "Unleashing the Power of Diversity in Our Workforce," with distinguished panelists Monica Jackson, GE Aviation, Dereje Agonafer, a member of National Academy of Engineering, University of Texas at Arlington, Jean Trewhella, GLOBALFOUNDRIES and past CPMT President, and Rolf Achenbrenner, Fraunhofer IZM.

A record breaking 516 attendees to the 18 Professional Development Courses delivered during 69th ECTC.

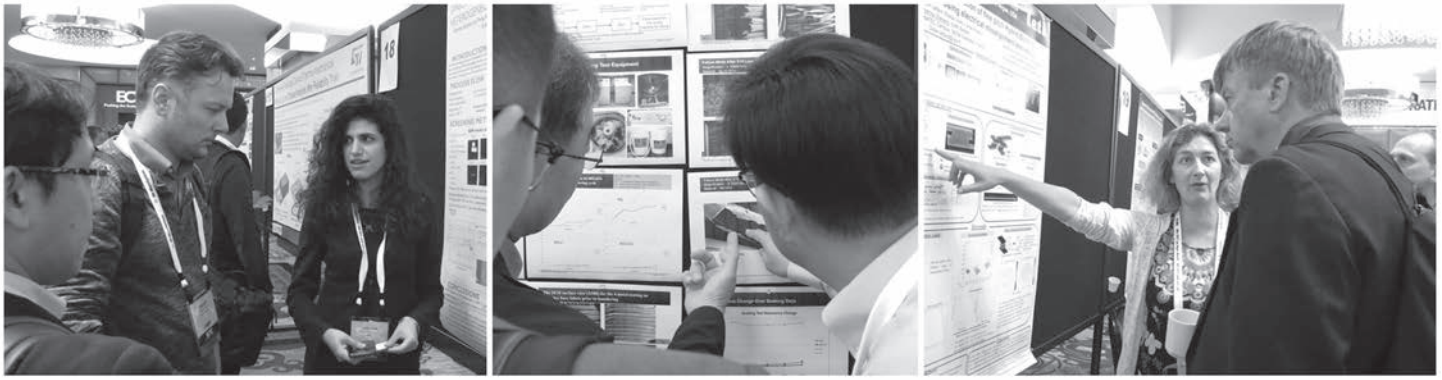
Rozalia Beica, Program Chair for ECTC 2020, hosted the ECTC 2019 Technical Program Committee meeting on Thursday evening during which she presented key statistics of the 69th ECTC and the calendar for the run up to the 70th ECTC in Orlando, Florida. The EPS Representative on the ECTC Executive Committee, C.P. Wong, introduced Ibrahim Guven, Virginia Commonwealth University, as the Assistant Program Chair of the 70th ECTC. The ECTC Technical Program Committee meeting during the conference marks an important milestone: celebration of yet another successful technical program. It provides information to the volunteer professional members of the packaging community who are working hard to maintain the high quality content in ECTC. This meeting also provides opportunity for potential new members to attend and apply for subcommittee membership.

The 69th ECTC Gala Reception followed the Technical Program Committee meeting, which is the signature reception of ECTC, bringing together the conference attendees, exhibitors, sponsors, and their guests. The success of the 69th ECTC was collectively celebrated with the accompanying great food and beverages that were provided by the Gala Reception Gold and Silver sponsors.

The 2019 IEEE EPS Seminar was chaired by Yasumitsu Orii, Nagase, Japan, and Shigenori Aoki, LINTEK on Thursday night; the seminar was very well-attended. This year's topic was "Roadmap of IC Packaging Materials to Meet Next-Generation Smartphone Performance Requirements" with panelists Koichi Hasegawa, JSR, Kenji Nishiguchi, Risho Kogyo Co., Ltd., Yoshio Nishimura, Ajinomoto Fine-Techno Co., Inc., Toshihiko Nishio, SBR Technology Company, Eiichi Nomura, Nagase ChemteX Corporation, and Mike Sakaguchi, Tatsuta Electric Wire & Cable Co., Ltd. The panel outlined the product requirements for the smartphones for 2025-2030 timeline in the era of 5G and 6G. Expert panelists from above material development companies shared their approaches to meet the projected smartphone system requirements including materials for fan-out wafer-level and panel-level packaging, molding materials, high-speed substrates, and low-loss substrates.

The last day of ECTC 2019, Friday, featured yet another full schedule of technical topics and the Student Interactive Presentations. The morning technical sessions of Friday were "Wafer Level Packaging and Fan-In/Fan-Out Structures & Materials," "High-Speed Signaling for High-Performance Computing and Memory," "Advanced Biosensors and Bioelectronics," "Embedded

The 69th ECTC hosted 102 exhibitor booths at the Technology Corner.



69th ECTC had five Interactive Presentation (IP) sessions with a total of 106 presentations, including 22 in the Student IP Session.

and Integrated Technologies," "Electromigration and Innovative Reliability Test Methods," and "Assembly and Process Modeling." The Friday lunch continued long-held ECTC raffle tradition with Alan Huffman taking the MC role with an outstanding performance. Friday afternoon technical sessions covered "Automotive and Power Packaging," "Power and Panel Assembly," "Fan-Out, Flip Chip, and WLCSP," "Emerging Materials and Processing," "New Interconnects for Package Scaling," and "RF and Power Components and Modules."

With record breaking sponsorship and PDC attendance, high-quality technical content, second highest number of attendees, and ever strong exhibitor participation, the 69th ECTC was a great success. The ECTC Executive Committee would like to take this opportunity to thank all the attendees, exhibitors, and conference sponsors for their support as well as all the committee members and chairs who are volunteering their time to help organize the sessions and make ECTC such a success every year. Special thanks also to our event management.

The 70th ECTC will be held at Walt Disney World Swan and Dolphin Resort, Lake Buena Vista, Florida, USA, May 26–29, 2020. Chris Bower from X-Celeprint Inc. will be the General Chair of this conference. The Call for Papers and PDC Proposals will be available at www.ectc.net, and the abstract submission will close on October 6, 2019. So get those abstracts ready and submit them as soon as abstract submission opens online early August 2019.

We are looking forward to see you all in Orlando in 2020!

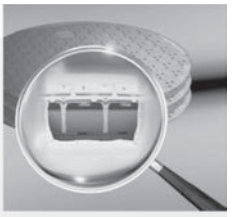
Ibrahim Guven
Assistant Program Chair,
IEEE ECTC 2019

IEEE ELECTRONICS PACKAGING SOCIETY

IEEE 3DIC 2019

International 3D Systems Integration Conference

October 8th – 10th, 2019, Sendai, JAPAN



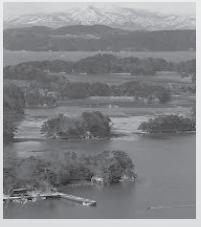
3DIC 2019 will cover all **3D integration** topics, including 3D/2.5D process technology, materials, equipment, circuits technology, design methodology and applications. The conference invites authors and attendees to submit and interact with researchers from all around the world. Papers are solicited in subject topics, including, but not limited to, the following:

3D/2.5D Integration Technology

***3D/2.5D IC Circuits Technology*:**

***3D/2.5D Applications*:**

***3D/2.5D Design and Test Methodology*:**



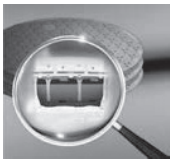
Conference web site: **www.3dic-conf.org**

The deadline for abstract submission is ***June 24, 2019***.
Abstracts are to be **1 page text (500 words) and 1 page figures**.

【2019 Conference Co-Chairs】
T. Tanaka (Tohoku Univ)
P. Franzon (NCSU)

【Organizing Committee】
Asia: T. Tanaka (Tohoku Univ), K. Lee (SK-hynix), K. N. Chen (NCTU), M. Koyanagi (Tohoku Univ)
USA: P. Franzon (NCSU), B. Patti (Tezzaron), M. Bakir (GA Tech), T. Karnik (Intel)
Europe: P. Ramm (Fraunhofer EMFT), E. Beyne (IMEC), P. Vivet (CEA-Leti), B. Vigna (STMicro)

IEEE 3DIC 2019



International 3D Systems Integration Conference
October 8th – 10th, 2019, Sendai, Japan

Call for Papers

The IEEE International 3D Systems Integration Conference (3DIC) will be held at the Hotel Metropolitan Sendai and Miyagino Ward Cultural Center in Sendai, Japan in October 8th-10th, 2019. The deadline for abstract submission is ***June 24, 2019***. Abstracts are to be 1 page text (500 words) and 1 page figures.

3DIC 2019 will cover all **3D integration** topics, including 3D/2.5D process technology, materials, equipment, circuits technology, design methodology and applications. The conference invites authors and attendees to submit and interact with researchers from all around the world. Papers are solicited in subject topics, including, but not limited to, the following:

3D/2.5D Integration Technology: Through Si Vias (TSV), Wafer thinning, Wafer alignment, Wafer bonding, Wafer dicing, Interposer (Si/Glass), Optical interconnection, FOWLP, Monolithic 3D integration, Heterogeneous 3D/2.5D integration

3D/2.5D IC Circuits Technology: SOC, Memory, Processor, DSP, FPGA, RF and μ-wave/mm-wave, Analog circuits, Biomedical circuits

3D/2.5D Applications: Artificial Intelligence, Machine Learning, Deep Learning, Imaging, IoT, Memory, Processors, Communications, Networking, Wireless, Biomedical

3D/2.5D Design and Test Methodology: CAD, Synthesis, Design flows, Signal and power integrity analysis and design in 3D/2.5D, Thermal design and analysis, Test and design for test, Mechanical stress and reliability design and analysis

2019 Conference Co-Chairs:
T. Tanaka (Tohoku Univ), P. Franzon (NCSU)

Organizing Committee

Asia: T. Tanaka (Tohoku Univ), K. Lee (SK-hynix), K. N. Chen (NCTU), M. Koyanagi (Tohoku Univ)

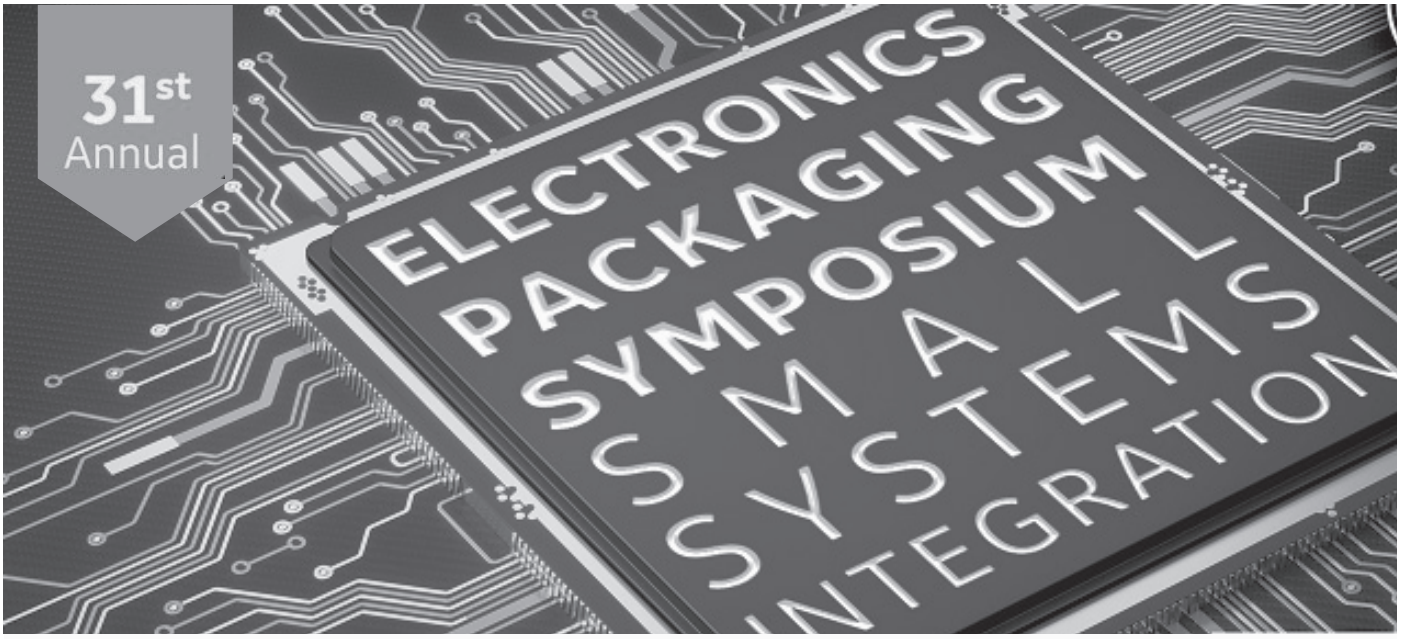
USA: P. Franzon (NCSU), B. Patti (Tezzaron), M. Bakir (GA Tech), T. Karnik (Intel)

Europe: P. Ramm (Fraunhofer EMFT), E. Beyne (IMEC), P. Vivet (CEA-Leti), B. Vigna (STMicro)

Conference web site: www.3dic-conf.org

IEEE ELECTRONICS PACKAGING SOCIETY

From 2020, 3DIC will be held in USA every year.



SEPTEMBER 5 - 6, 2019

GE RESEARCH | NISKAYUNA, NY

The 31st Annual Electronics Packaging Symposium-Small Systems Integration, provides a forum that brings together leaders in academia, industry, and government, to share quality, up-to-date information through different lenses on trending electronics packaging topics, and provide opportunities to network, share ones expertise, learn, and build partnerships.

This year's program includes keynote speakers, 12 sessions with technical presentations, a half-day IEEE EPS Heterogeneous Integration Roadmap workshop on September 6, a student poster session with students from local Universities in NY, and exhibits from leading companies.

Session Topics

- 2.5/3D Packaging
- mm Wave in Packaging
- Automotive & Harsh Environments
- Bioelectronics
- Flexible & Additive Electronics
- Materials for Packaging & Energy Storage
- MEMS
- Photonics
- Power Electronics
- Sensors, Embedded Electronics & IoT
- Thermal Challenges
- Wearable and Flexible Electronics for Medical Applications

CALL FOR SPONSORS AND EXHIBITORS

SPONSOR PACKAGE
$2,500

- 3 complimentary registrations
- 1 (6 foot) table & 2 chairs with 2 days exhibit time
- 1 full-page color add in program
- Company name and logo on website and conference signs

EXHIBITOR PACKAGE
$1,000

- 1 complimentary registration
- 1 (6 foot) table & 2 chairs with 2 days exhibit time
- Company name listed in program and on website

REGISTER AT WWW.BINGHAMTON.EDU/IEEC/2019EPS

2018 SYMPOSIUM

380+	52	12	54	53
ATTENDEES	INVITED SPEAKERS	TECHNICAL SESSIONS	STUDENT POSTERS	EXHIBITORS

REGISTER NOW!

CONTACT US: EPSYMPOS@BINGHAMTON.EDU

Conference hosted by:

EPTC 2019

21st Electronics Packaging Technology Conference
4th-6th Dec 2019, Marina Bay Sands, Singapore

IEEE EPS Flagship Conference in Asia Pacific Region

CALL FOR PAPERS

ABOUT EPTC

The 21st Electronics Packaging Technology Conference (EPTC 2019) is an international event organized by the IEEE RS/EPS/EDS Singapore Chapter and co-sponsored by IEEE Electronics Packaging Society (EPS). EPTC 2019 will feature keynotes, technical sessions, short courses, forums, an exhibition, social and networking activities, including a banquet for all attendees. It aims to provide a good coverage of technology developments in all areas of electronics packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet with leading international experts.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in the Asia Pacific and is well attended by experts in all aspects of packaging technology from all over the world. EPTC is the flagship conference of IEEE EPS in Region 10.

CONFERENCE TOPICS

You are invited to submit abstract(s), presenting new developments in the following categories:

- **Advanced Packaging:** Advanced Flip-chip, 2.5D & 3D, PoP, embedded passives & actives on substrates, System in Packaging, Embedded chip packaging technologies, Panel level packaging, RF, Microwave & Millimeter-wave, Power and Rugged Electronics Packaging, etc.
- **TSV/Wafer Level Packaging:** Wafer level packaging (Fan in/Fan out), Embedded chip packaging, 2.5D/3D integration, TSV, Silicon & Glass interposer, RDL, Bumping technologies, etc.
- **Interconnection Technologies:** Au/Ag/Cu/Al Wire-bond / Wedge bond technology, Flip-chip & Cu pillar, Solder alternatives (ICP, ACP, ACF, NCP, ICA), Cu to Cu, Wafer level bonding & die attachment (Pb-free), etc.
- **Emerging Technologies:** Packaging technologies for MEMS, biomedical, Optoelectronics, Internet of things, Photovoltaic, Printed electronics, Wearable electronics, Photonics, LED, etc.
- **Materials and Processing:** Advanced materials (such photoresist, polymer dielectrics, solder, die attach, underfill), Substrates, Lead-frames, PCB for advanced packaging, Assembly processes using advanced materials, etc.
- **Assembly and Manufacturing Technology:** Assembly equipment automation and improvements. Embedded/Hybrid Package Manufacturing Processes. Warpage Control and Management in Board Level Assembly, Thin Die/Package Handling and Assembly. Large/Ultra Large Package (SiP, SIM, MCP) Integration and Processing. Panel Level Manufacturing. Smart Manufacturing technology. Data analytics. Advanced metrology. Machine learning.
- **Electrical Simulation & Characterization:** Power plane modeling, Signal integrity analysis by simulations and characterization, 2D/2.5D/3D package level high-speed signal design, Characterization and test methodologies.
- **Mechanical Simulation & Characterization:** Thermo-mechanical, Moisture, Fracture, Fatigue, Vibration, Shock and drop impact modeling and characterization. Process modeling. Chip-package interaction, etc.
- **Thermal Characterization & Cooling Solutions:** Thermal modeling and simulation, Component, system and product level thermal management and characterization
- **Quality, Reliability & Failure Analysis:** Component, board, system and product level reliability assessment, Interfacial adhesion, Accelerated testing, Failure characterization, etc.

IMPORTANT DATES

Online abstract submission start	**25th Apr 2019**
Closing of abstract submission	**15th July 2019**
Notification of acceptance	**30th August 2019**
Submission of manuscript	**30th September 2019**

Please check on http://www.eptc-ieee.net for latest update.

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited which describe original and unpublished work. The abstract should be at least 500-750 words long and clearly state the purpose, methodology, results (including data, drawings, graphs and photographs) and conclusions of the work. Authors can indicate preference of oral or poster presentation.
All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.
The abstracts must be received by 15th July 2019. Authors must include their affiliation, mailing address, telephone number and email address. Authors will be notified of paper acceptance and publication instructions by 30th August 2019. The final manuscript for publication in the conference proceedings is due on 30th September 2019. The conference proceedings is an official IEEE publication and accepted papers that are registered and presented (oral & poster) will be available in IEEE Xplore.

BEST PAPER AWARDS

Awards will be given to the best oral papers from Academia, Industry, Students, and to the best interactive papers. More details can be found at http://www.eptc-ieee.net

CALL FOR SHORT COURSES

The conference program includes short courses which will be conducted by leading experts in the field. Details will be updated in the conference website. Attendees are entitled to one PDC course. Proposals for short courses can be submitted to pdc@eptc-ieee.net

CALL FOR EXHIBITION / SPONSORSHIP PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment and services to the microelectronics packaging and manufacturing, will be held during the conference. For details, please email to exhibition@eptc-ieee.net and sponsorship@eptc-ieee.net.

EPTC 2019: website: http://www.eptc-ieee.net Email: secretariat@eptc-ieee.net Join us on: Linkedin [EPTC OC]

Organized by
IEEE Singapore RS/EPS/EDS Chapter

General Chair
Wui Weng Wong
AMD
generalchair@eptc-ieee.net

Technical Chair
Eric Phua
SgEC
techchair@eptc-ieee.net

Sponsored by
IEEE ELECTRONICS PACKAGING SOCIETY

****

EDAPS 2019 Conference Announcement

****

IEEE EDAPS 2019 (Dec. 16-18, 2019, Kaohsiung, Taiwan)

IEEE Electrical Design of Advanced Packaging and Systems, The Grand Hi-Lai Hotel, Kaohsiung, Taiwan, Dec. 16-18, 2019, http://edaps.org

Dear Colleagues:

You are cordially invited to share your latest research results related to electrical design of advanced packaging and systems, which include on-chip, packages, and systems, such as SI/PI, EMI/RFI, 5G hardware, Applications of AI/Machine learning on electrical design, and Array antennas at IEEE EDAPS 2019 conference in Kaohsiung, Taiwan.

CALL FOR PAPERS

The IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) Symposium has been one of main events in South Asia and Asia Pacific design communities, which attracts world class designers and researchers to share their most recent results related to modeling, simulation, and electrical design at on-chip, package, and system/module levels. The symposium consists of tutorials, paper presentations, industry exhibition, and poster presentations. The technical program of the symposium addresses the current technical issues facing design in IC, SiP/SoP packaging, EMI/EMC, RF isolation, and most importantly applications of AI/Machine learning in the next generation design of 3D IC (SoC, RF CMOS, RF SoC), FO/InFO PoPs, heterogeneous RF-passives systems, and EDA tools with AI-assisted smart.

Taiwan is famously known as Silicon Island, which has played a leading role in design, fabrication, and manufacturing services at chip, package, and board levels. Let's all participate this highly anticipated event where knowledge sharing and cordial exchanges between the academia and industry will surely take place.

IEEE EDAPS 2019 will be held in Kaohsiung, Taiwan on Dec. 16-18, 2019. Topics of interest include, but are not limited to:

– 3D IC/3D Stacked IC, SI, PI, EMC systems

– AI-based electrical design for SoC, SiP, and Board designs

– Homogeneous RF CMOS and RF SoC, and chiplet designs

– Heterogeneous Integrated RF-passives systems (Front End) design for 5G mobility

– Measurement techniques and Systems (including 5G antennas and AI for design)

– Antennas for 5G, Integration of Security and AI chip

KEYNOTE SPEAKERS

- Douglas C.-H. Yu, VP, TSMC (A recipient of Presidential Science Prize in 2017)
- Recruiting other Keynote speakers on topics such as Applications of AI/Machine learning in optimizing EDA design and manufacturing, Low power memory for portable devices

---
TUTORIAL TOPICS

- Moises Cases on Mixed-signal Design and Testing
- Recruiting other tutorial speakers on topics such as 5G chipset, Semiconductor IP, chiplet & homogeneous integration, and Advances in EDA and measurement techniques

---
PUBLICATION HIGHLIGHTS

IEEE proceedings, indexed by

– IEEE Xplore

IMPORTANT DATES

Tutorial Session Proposals Due: July 26, 2019

Author Notification

September 20, 2019

Regular Presentation (Main Tracks):

Paper Submission Deadline

August 5, 2019

Author Notification

September 20, 2019

Conference Registration Starts:

September 20, 2019

SUBMISSION

Authors are invited to submit their original research work that has not previously been submitted or published in any other venues. Papers should be prepared in IEEE format and submitted via submission system.

IEEE formatting information:
http://www.ieee.org/conferences_events/conferences/publishing/templates.html

Submission system:
https://conferences.ece.illinois.edu/submit/go.asp?id=1339

– Tutorial sessions consist of topics organized by TPC and/or topics proposed by researchers in the community. Proposed tutorial topics can be submitted to the Technical Program Chair and Co-chair (Profs. Lin and Lu) of the conference. A proposal should include title, theme, scope, number of papers, and presenters and organizations. See http://edaps.org/tutorials.php for submitting tutorial proposals.

– Regular papers (3 pages) in the main tracks should explore a specific technology problem and propose a complete solution to it, with experimental results. They are orally presented under each main track in front of audience.

– Poster papers (also 3 pages in length) have the same technical requirements as those for the regular papers. The papers are succinctly summarized on a panel, and the audiences are able to discuss interactively with the author(s) in front of the panel.

All accepted papers in regular main tracks and posters will included into IEEE Xplore Digital Library. Selected papers will be invited to submit full extended form to be considered for Special issue publication in prestigious IEEE Transactions on Components, Packaging and Manufacturing Technology (CPMT).

BEST PAPER AWARDS

The award committee will select Best Paper/Poster Award(s) and present the winners with an Award Certificate.

ORGANIZING COMMITTEE

Honorary General Chair
CP Hung, *ASE*/Douglas C.-H. Yu, *TSMC* (in alphabetical order)

General Chair
Lih-Tyng Hwang, *NSYSU*, Taiwan

Technical Program Chair
Ding-Bing Lin, *NTUST*, Taiwan, Hsin-Chia Lu, *NTU*, Taiwan

Publication Chair
Hsin-Chia Lu, *NTU*, Taiwan

Award Chair
Hsin-Chia Lu, *NTU*, Taiwan

Treasurer
Chao-Hsiung Tseng, *NTUST*, Taiwan

INTERNATIONAL ADVISORY COMMITTEE

Madhavan Swaminathan, *GaTech,* USA
Jose Schutt-Aine, *UIUC*, USA
Paul Franzon, *NCSU,* USA
Hideki Asai, *Shizuoka U,* Japan
Kemal Aygun, *Intel*, USA
Dale Becker *IBM,* USA
Wendem Beyene, *Intel*, USA
Eric Beyne, *IMEC, Belgium*
Flavio Canavero, *Politecnico di Torino*, Italy
Shen-Li Fu, *I-Shou U.*, Taiwan
Jason Tzyy-Sheng Horng, *NSYSU,* Taiwan
Lijun Jiang, *HKU*, Hong Kong
C. Robert Kao, *NTU,* Taiwan
Joungho Kim, *KAIST,* S. Korea
An-Yu Kuo, *Cadence,* USA
Ricky Shih-Wei Lee, *HKUST,* Hong Kong
Erping Li, *ZJU,* China
Yuan-Liang Li, *Intel*, Taiwan
En-Xiao Liu, *IHPC*, Singapore
Mike Ma, *Amkor*, Taiwan
Junfa Mao, *SJTU,* China
Ivan Ndip, *F-IZM,* Germany
Dan Oh, *Samsung,* S. Korea
Bahgat G. Sammakia, *SUNY*, USA
Rohit G. Sharma, *IIT Ropar,* India
Manos M. Tentzeris, *Ga Tech,* USA
Chuei-Tang Wang, *TSMC*, Taiwan
Ruey-Beei Wu, *NTU,* Taiwan
Tzong_Lin Wu, *NTU,* Taiwan
Wen-Yan Yin*, ZJU,* China

TECHNICAL PROGRAM COMMITTEE

Ding-Bing Lin, *NTUST*, Taiwan, Chair
Hsin-Chia Lu, *NTU*, Taiwan, Co-chair
Flavio Canavero, *Politechico di Torino*, Italy
Joungho Kim, *KAIST*, S. Korea
Erping Li, *ZJU*, China
Han-Nien Lin, *FCU,* Taiwan
Wei-Chung Robert Lo, *ITRI*, Taiwan
Jose Schutt-Aine, *UIUC*, USA
Rohit Sharma, *IIT Ropar*, India
Guang-Hwa Shiue, *CYCU*, Taiwan
Bin-Chyi Tseng, *ASUS*, Taiwan
Tzong-Lin Wu, *NTU*, Taiwan
Wen-Zhou Wu, *Mediatek*, Taiwan
Kuo-Chung Yee, *TSMC*, Taiwan

IEEE ESTC EPS VESTFOLD 2020

Electronics System-Integration Technology Conference

15th-18th September 2020
Vestfold, Norway

Call for papers

The Electronics System-Integration Technology Conference (ESTC) is the premier international event in the field of electronics packaging and system integration. The conference is organized every two years in Europe and is supported by IEEE-EPS in association with IMAPS-Europe.

This international event brings together both academics and industry leaders to present and discuss the state-of-the-art as well as the future trends in electronics packaging and integration technologies. ESTC offers excellent opportunities for knowledge exchange and networking with international experts in the field.

The ESTC 2020 will take place from 15th to 18th September 2020 in Vestfold, Norway, where the "Norwegian Centre of Expertise" in Micro- and Nanotechnologies is established. The industry cluster in Vestfold, together with the University of South-Eastern Norway (USN), represents a major portion of Norway's activities in the field. High-end devices for aerospace, medical, maritime and industrial applications are quality products from the region, with a strong focus on packaging, system integration and reliability.

Vestfold, Norway, welcomes you with its proud maritime traditions, as the centre of Viking cultural heritage, and with a pleasant climate. The conference venue will be at the beautiful Tønsberg Pier. Communication to Vestfold is easy, with direct train from Oslo Airport (OSL), as well as the local airport (Sandefjord Torp – TRF) with direct connections to several major European destinations.

Website open for abstract submission:
1st December 2019

Abstract submission deadline:
16th February 2020

Notification of acceptance:
31st March 2020

University of South-Eastern Norway · IEEE · IMAPS Europe · IEEE Electronics Packaging Society · Norwegian Centres of Expertise NCE Micro- and Nanotechnology

General Chair: Knut E. Aasmundtveit (USN), **Executive Chair: Kristin Imenes** (USN), **Technical Program Chair: Paul M. Svasta** (CETTI, Romania)

estc-conference.net

2019 IWLPC

16th International Wafer-Level Packaging Conference

Presenting the 16th annual International Wafer-Level Packaging Conference:

Advanced Packaging in the New Connected World

DoubleTree by Hilton Hotel ● San Jose, California USA

Set your sights for Silicon Valley on October 22-24, 2019

Save the Dates!

Conference: October 22- 23

Exhibits: October 22-23

Professional Development Courses: October 24

Special Events!

Keynote Presentations

Panel Discussion

Networking Reception

Interactive Poster Sessions

Don't miss out on Silicon Valley's premier event! Register now!

Chip Scale Review®
ChipScaleReview.com
The Future of Semiconductor Packaging

www.iwlpc.com
Tel: +1-952-920-7682

SMTA

Sponsorships
Kim Newman
knewman@chipscalereview.com

Exhibit
Hannah Terhark
hannah@smta.org

Conference
Jaclyn Sarandrea
jaclyn@smta.org

Top Conference Papers Based on 2018 Usage

2018 IEEE 68th Electronic Components and Technology Conference (ECTC)

(May 29 2018–June 1, 2018)

A 77GHz Antenna-in-Package with Low-Cost Solution for Automotive Radar Applications
Cheng-Yu Ho; Sheng-Chi Hsieh; Ming-Fong Jhong; Chen-Chao Wang; and Chun-Yen Ting

Heterogeneous Integration Technology Demonstrations for Future Healthcare, IoT, and AI Computing Solutions
John Knickerbocker; R. Budd; B. Dang; Q. Chen; E. Colgan; L.W. Hung; S. Kumar; K. W. Lee; M. Lu; J.W. Nah; R. Narayanan; K. Sakuma; V. Siu; B. Wen

Mm-Wave Antenna in Package (AiP) Design Applied to 5th Generation (5G) Cellular User Equipment Using Unbalanced Substrate
Ying-Wei Lu; Bo-Siang Fang; Hsuan-Hao Mi; Kuan-Ta Chen

A Compact 27 GHz Antenna-in-Package (AiP) with RF Transmitter and Passive Phased Antenna Array
Mei Xue; Liqiang Cao; Qidong Wang; Delong Qiu; Jun Li

InFO_AiP Technology for High Performance and Compact 5G Millimeter Wave System Integration
Chuei-Tang Wang; Tzu-Chun Tang; Chun-Wen Lin; Che-Wei Hsu; Jeng-Shien Hsieh; Chung-Hao Tsai; Kai-Chiang Wu; Han-Ping Pu; Douglas Yu

2018 17th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(May 29–June 1, 2018)

Thermal Performance Comparison of Advanced 3D Packaging Concepts for Logic and Memory Integration in Mobile Cooling Conditions
Herman Oprins; Vladimir Cherman; Eric Beyne

The Heat Conduction Renaissance
Aditya Sood; Eric Pop; Mehdi Asheghi; Kenneth E. Goodson

Analysis of Thermal Characteristics of Gallium Oxide Field-Effect-Transistors
Jialuo Chen; Zhanbo Xia; Siddharth Rajan; Satish Kumar

Artificial Neural Network Based Prediction of Temperature and Flow Profile in Data Centers
Jayati Athavale; Yogendra Joshi; Minami Yoda

Thermal Management Strategies for a High-Frequency, Bi-Directional, On-Board Electric Vehicle Charger
Kshitij Gupta; Carlos Da Silva; Miad Nasr; Amir Assadi; Hirokazu Matsumoto; Olivier Trescases; Cristina H. Amon

2018 7th Electronic System-Integration Technology Conference (ESTC)

(September 18–21, 2018)

Roles and Requirements of Electronic Packaging in 5G
Ivan Ndip, Klaus-Dieter Lang

Embedding and Interconnecting of Ultra-Thin RF Chip in Combination with Flexible Wireless Hub in Polymer Foil
Golzar Alavi; Sefa özbek; Mahsa Rasteh; Markus Grözing; Manfred Berroth; Jan Hesselbarth; Joachim N.Burghartz

Silver Sintering in Power Electronics: The State of the Art in Material Characterization and Reliability Testing
Marco Schaal; Markus Klingler; Bernhard Wunderle

Curved Full-Frame CMOS Sensor: Impact on Electro-Optical Performances
Bertrand Chambion; Stephane Caplet; Jan Martin Kopfer; Aurelie Vandeneynde; Wim Diels; Alexandre de Kerckhove; Patrick Peray; David Henry

Future Interconnect Materials and System Integration Strategies for Data-Intensive Applications
Pushkar Apte; Tom Salmon; Richard Rice; Mark Gerber; Rozalia Beica; Jeff Calvert; Dave Hemker; Yezdi Dordi; Manish Ranjan; Suresh Ramalingam; Jaspreet Gandhi; Alireza Kaviani; Subhasish Mitra; Philip Wong; Vincent Lee Stanford; Mohamed El-Sabry

2018 IEEE 20th Electronics Packaging Technology Conference (EPTC)

(December 4–7, 2018)

Innovative Packaging Solutions of 3D System in Package with Antenna Integration for IoT and 5G Application
Mike Tsai; Ryan Chiu; Eric He; J. Y. Chen; Royal Chen; Jensen Tsai; Yu-Po Wang

Pluggable Silicon Photonic MEMS Switch Package for Data Centre
How Yuan Hwang; Jun Su Lee; Johannes Henriksson; Kyungmok Kwon; Tae Joon Seok; Ming C. Wu; Peter O'Brien

Study on Electrical Performance and Mechanical Reliability of Antenna in Package (AIP) with Fan-Out Wafer Level Packaging Technology
F.X. Che; Zihao Chen

Dual-band Differential Outputs CMOS Low Noise Amplifier
Atsuhiro Hamasawa; Haruichi Kanaya

Ceramic Interposers for Ultra-High Density Packaging and 3D Circuit Integration
Arash Adibi; Aria Isapour; Mohsen Niayesh; Ammar Kouki

Upcoming EPS Sponsored and Cosponsored Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the EPS sponsors and supports a number of global and regional conferences, workshops and other techical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through IEEE Xplore.

Name: 2019 20th International Conference on Electronic Packaging Technology(ICEPT)
Location: Hong Kong, China
Date: Aug 11, 2019–Aug 15, 2019

Name: 2019 31st Electronics Packaging Symposium
Location: NIskayuna, NY USA
Date: Sep 5, 2019–Sep 6, 2019

Name: 2019 IEEE Holm Conference on Electrical Contacts
Location: Milwaukee, WI USA
Date: Sep 14, 2019–Sep 18, 2019

Name: 2019 41st Annual EOS/ESD Symposium (EOS/ESD)
Location: Riverside, CA USA
Date: Sep 15, 2019–Sep 20, 2019

Name: 2019 22nd European Microelectronics and Packaging Conference & Exhibition (EMPC)
Location: Pisa, Italy
Date: Sep 16, 2019–Sep 19, 2019

Name: 2019 25th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)
Location: Lecco, Italy
Date: Sep 25, 2019–Sep 27, 2019

Name: 2019 IEEE Electronic Design Process Symposium (EDPS)
Location: Milpitas, CA USA
Date: Sep 26, 2019–Sep 27, 2019

Name: 2019 International 3D Systems Integration Conference (3DIC)
Location: Sendai, Japan
Date: Oct 8, 2019–Oct 10, 2019

Name: 2019 International Wafer Level Packaging Conference (IWLPC)
Location: San Jose, CA USA
Date: Oct 22, 2019–Oct 24, 2019

Name: 2019 14th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)
Location: Taipei, Taiwan
Date: Oct 23, 2019–Oct 25, 2019

Name: 2019 IEEE CPMT Symposium Japan (ICSJ)
Location: Kyoto, Japan
Date: Nov 18, 2019–Nov 20, 2019

Name: 2019 IEEE 21st Electronics Packaging Technology Conference (EPTC)
Location: Singapore
Date: Dec 4, 2019–Dec 6, 2019

Name: 2019 Electrical Design of Advanced Packaging and Systems (EDAPS)
Location: Kaohsiung, Taiwan
Date: Dec 16, 2019–Dec 18, 2019

Name: 2020 Pan Pacific Microelectronics Symposium (Pan Pacific)
Location: Kohala Coast, HI USA
Date: Feb 10, 2020–Feb 13, 2020

Name: 2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)
Location: Lake Buena Vista, FL USA
Date: May 26, 2020–May 29, 2020

Name: 2020 IEEE 70th Electronic Components and Technology Conference (ECTC)
Location: Lake Buena Vista, FL USA
Date: May 26, 2020–May 29, 2020

PROFESSIONAL AWARDS & RECONGITION

Lamar University Professor and EPS Board of Governors member, Xuejun Fan, Ph.D., has been awarded the Mary Ann and Lawrence E. Faust Endowed Professorship in Engineering for his research in multi-physics and multi-scale modeling and characterization of heterogeneous electronic system. Fan received the University Professor Award in 2018. He has received the Outstanding Sustained Technical Contribution Award in 2017 and Exceptional Technical Achievement Award in 2009 from IEEE Electronic Packaging Society. He became an IEEE Fellow in 2019.

Election to the National Academy of Engineering is one of the highest professional honors accorded an engineer. Members have distinguished themselves in business and academic management, in technical positions, as university faculty, and as leaders in government and private engineering organizations. Members are elected to NAE membership by their peers (current NAE members). EPS member Dereje Agonafer was awarded this honor in February 2019.

TECHNOLOGY

Innovation: Hardware to Software and Back through AI

Introduction

After decades of the electronics revolution, one often hears people posit that electronic hardware has become a commodity product and that business growth has moved to software. The companion statement is something like "Moore's Law is dead." This newsletter article will investigate the veracity of this quip and highlight new directions in hardware brought about by implementation of Artificial Intelligence (AI).

Something is in the Wind

Current vernacular uses words such as "AI," "the cloud" and "cyber security" rather than the hardware-focused buzz word "nanotechnology" touted for the previous two decades. Google Trends plots Internet hits on topics, serving as a measure of public interest in a topic. In Figure 1, the relative worldwide popularity of the "nanotechnology" (red) is contrasted to software terms like "the cloud" (yellow) and "cyber security" (blue), using Google Trends. This plot shows evidence that the previously popular hardware term is being replaced by the software terms.

Microeconomics

Microeconomics provides two ideal models that bracket business behavior (above and below): the commodity supplier vs. the monopoly.

In microeconomics, a "commodity" product is a product that has many suppliers and is substitutable across these suppliers. Therefore, each individual seller has no control of price. A seller can only decide how many products to produce. This market structure is known as "pure competition" or as the "price taker." The supply-demand curve is shown as in Figure 2. As a consequence of this microeconomics consequence, a commodity manufacturer will focus effort on minimizing manufacturing and distribution costs.

The opposite situation to being a "price taker" is the market structure of the monopoly where the one seller sets the price. An inventor who is granted broad patent rights enjoys a temporary monopoly. The legal theory is that economic growth is promoted by the government's intervention in the free market by means of a well-regulated patent office that provides such a temporary monopoly in exchange for divulging the invention to the public.

Many investors or owners hope to enjoy the freedom and profitability of a business that is as close as possible to a monopoly. This investor desire drives research and development into new technology products.

Supporting Indicators

The growth of software over hardware is reflected not just in popular gossip or but in many other indicators. First, the worldwide energy consumption for data centers (i.e., the cloud) is estimated between two and three percent of all energy consumption, about the same percentage as energy used in all agriculture. Therefore, there is some supporting

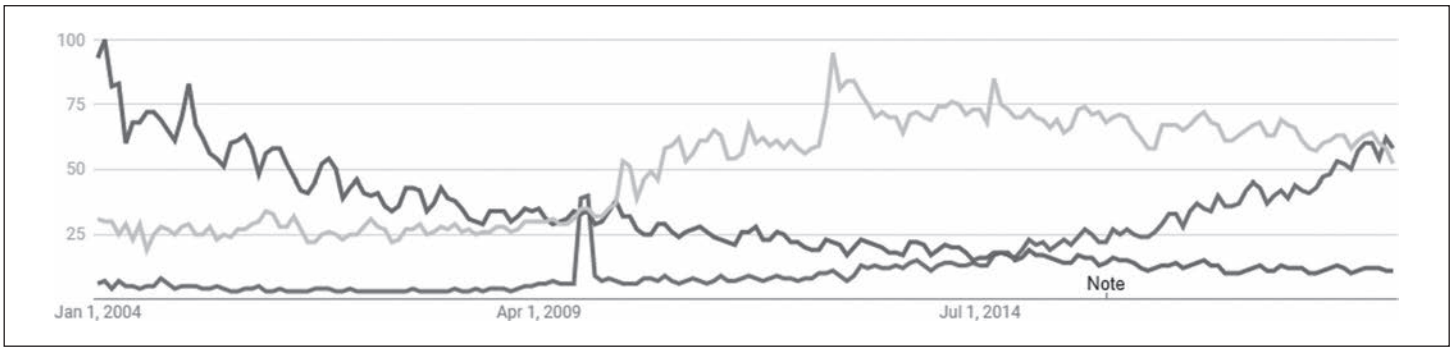


Figure 1. Relative Popularity of Hardware vs. Software Terms.

data of software-driven business growth from a thermodynamics perspective. Second, support is provided by the job market in the United States [Note this same trend is likely worldwide, but I will use readily available US data.] The United States Department of Labor's Bureau of Labor Statistics (BLS) states "The change in employment is expected to be tempered by slow growth or decline in most manufacturing industries in which electrical and electronics engineers are employed." The BLS says there were 324,600 people employed in Electrical and Electronics Engineering jobs in 2018 with an average pay of 99,070 US$ per year. This contrasts to 1.26 million Software Developer jobs with an average pay of 105,590 US$. In 2013, the National Science Foundation's most recent data, reported that 1.1 million bachelor's degrees were granted in computer/information science while only 0.62 million bachelor's degrees were granted in electrical engineering. Therefore, there is supporting evidence of the growth of software over hardware from the labor market.

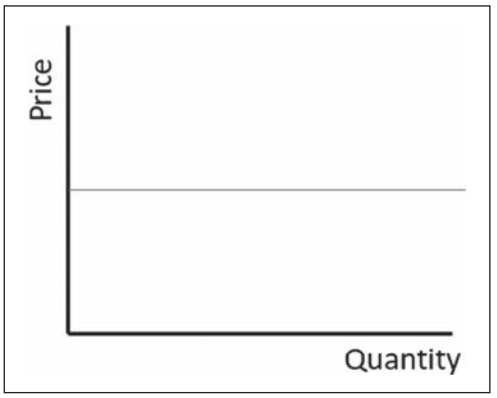


Figure 2. What "Commodity" Means in Economics.

Integrated Circuits and Hardware Innovation

Certainly, the origin of electronics-based computing from the Antanasoff-Berry computer, the Konrad Zuse Z3, the Colossus, and Mauchly's ENIAC is now a lifetime ago. Even the building blocks of computing technologies, such as the integrated circuit, DRAM and flash memory, are approximately 50 years old.

IEEE EPS readers are well aware of the technical responses to limits inherent to transistor density in integrated circuit design over recent decades such as stalling of CPU clock speeds across product vintages and the introduction of multiple cores in CPUs. The mounting cost of entry into the semiconductor fab business has resulted in industry consolidation and the growth of fabless business model (fabless means that the IC designer outsources device fabrication to another firm typically known as a "foundry"). So, the earlier quip is based on some basic truth; the electronics industry's (1970s to 2000s) business growth model, based on Moore's Law. Has moved towards fitting the commodity model.

In response, IEEE EPS members have led a technical response to this challenge by introducing an exciting set of packaging innovations that have enabled continued electronics products evolution. In the previous print newsletter "President's Column," Dr. Avram Bar-Cohen wrote about some of these innovations in the context of IEEE EPS conferences and publications. These innovations are most easily witnessed as embodied in our modern high-performance cellphones.

All that said, there seems to be no known device technology, i.e. hardware, that will provide the year-to-year performance boosts of the past, despite massive investment. Instead, the work of IEEE EPS members will be providing much of the improvements in digital electronics, at least in the near term.

Business's Love Affair with Software

From the labor market data provided above, it seems that business leaders see integrating software as the best business growth strategy. In our now dominant dot-com business model, software is used to embody a business practice. Typically, a computer runs a website providing a front-end interface to a customer, a data base back-end manages the order, bank-to-bank secure transaction handles payment, and a distribution model (often outsourced) provides the service.

The reader may not be aware that dot-com business model originated not just from the introduction of a popular commercial web browser in 1994 but from a legal decision. As may be familiar to the reader, United States patents fall into three categories of plant, utility and design patents. Most engineering patents are utility patents and were, prior to this time, primarily focused on hardware innovation. The tale of IBM's early interest, and eventual rejection, in Dr. Gary Kildall's CP/M operating system for inclusion in their personal computer in 1980 often rests, in part, on the weakness of patent law relative to software at that time. In a landmark 1998 decision regarding a data processing system for managing a financial service, known as "State Street Bank & Trust Co. v. Signature Financial Group, Inc.," the court allowed patents of business methods and the number of business method patents exploded. Although this thread could lead to an interesting legal discussion, it is sufficient to simply note that the list of the largest corporations, by market capitalization, is adorned with business software corporations. In plain words, business has fallen in love with software investment and created an investor "fashion" craze for software products.

Artificial Intelligence (AI)

Art sometimes presages science. Films such as the 1968 film *2001 Space Odyssey* with the computer HAL and the 1983 film *WarGames* with computer WOPR predated Artificial Intelligence (AI) today as embodied in IBM's Watson (2008), Apple's Siri (2011). When in 2005 Stanford's robotic Volkswagen Touareg named Stanley won the DARPA Grand Prize by transiting a defined 142-mile course through the Mohave Desert, autonomously, AI moved from fiction to reality.

The electronics trade newsletter *EETimes* has reported a number of integrated circuit companies working on exciting AI accelerator products. AI is moving away from the so-called Von Neuman computing architecture which has been the basis of all CPUs sold today. The brain does not seem to operate on Von Neuman architecture, and the brain is far more energy efficient than any CPU. The same should be expected in AI hardware.

Since implementation of AI is both a software and hardware challenge, it naturally falls upon IEEE EPS members who are skilled at integration. AI provides a unique opportunity for new product development, although it constitutes a challenging multidisciplinary opportunity.

Conclusion

The electronics hardware market has matured, but much exciting new opportunity is just around the corner. One of these opportunities is due to the work of Computer Scientists on AI. The business world is excited about AI. IEEE EPS should be excited too, because AI accelerators will spawn growth in hardware innovation making science fiction into reality.

Dan Donahoe
IEEE Senior Member

IEEE Electronics Packaging Society
Denise Manning, Executive Director
445 Hoes Lane
Piscataway, NJ 08854 USA

Getting the Most out of IEEE and EPS Membership: eBooks

Did you know that IEEE members now have access to more than 220 eBooks from the IEEE Press collection through IEEE Xplore, including: handbooks; introductory and advanced texts; reference works; professional books.

Follow 3 simple steps:

1. Log in to IEEE Xplore http://www.ieeexplore.ieee.org/Xplore/guesthome.jsp using your IEEE Member Web account.
2. Under the "Browse" heading in the left-hand navigation, click on "Books".
3. Select the "Classics" tab from the top of the page. Under this tab you will find a listing of all the Free titles.

Here are a few examples of available books in pdf format: (more added every year)

1. *Lead-Free Electronics: iNEMI Projects Lead to Successful Manufacturing* by E. Bradley, C. Handwerker, J. Bath, R. Parker and R. Gedney; Publication Date: 2007
2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

For more information visit: http://www.ieee.org/membership_services/membership/products/ebookclassics.html