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Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Chris Bailey
University of Greenwich
London, UK

As we begin a new year, I would like to thank all our members for your continued support of EPS. With the Covid-19 pandemic affecting many of us, the year 2020 has undoubtedly been a year that many of us would like to forget. Thankfully, with the distribution of vaccines starting worldwide, this pandemic will hopefully be behind us soon. Although this has been a challenging year, I am delighted that our society has progressed steadily towards its strategic goals throughout the last year in our areas of membership, chapters, conferences, education, technology, publications, and awards.

Sadly at the end of 2020, we heard the tragic news of the passing of our colleague, mentor, and EPS junior past president—Professor Avi Bar-Cohen. As many of you know, Avi was a leader in thermal sciences and contributed significantly to innovations in thermal management for electronics packaging throughout his career. He will be missed, but his dedication and outstanding contributions to our community continue to inspire us all. A section in the upcoming CPMT transactions will celebrate Avi's lifes work.

Recently, Avi worked with our colleague Vasudeva Atluri to secure donations to endow the society's highest award—the EPS technical field award. I am pleased to confirm that the IEEE Board of Directors has approved the renaming of this endowed award as the Rao Tummala Technical Field Award in honor of Professor Rao Tummala's extensive technical achievements in our field of Electronics Packaging. The awards first recipient will be at ECTC 2022.

In this edition of the newsletter, you can read how we are progressing towards our membership goals. Both Alan Huffman (VP Membership) and Professor Andrew Tay (Student Program Director) detail membership benefits, how to become involved with our chapters worldwide, and some of the latest developments taking place with our growing portfolio of student branch chapters. In terms of education, Professor Jeff Suhling (VP Education) and our functional team for education have been working on our exciting certificate program and a new EPS resource center that will contain webinars and other educational materials for our members. Further details on these will be made available on the website.

Our society's goals for technology are also progressing well. Dave McCann (VP Technology) and our functional team for technology have been working closely with our technical committees, who are providing insightful material for our newsletter on specific topics in their specialized areas. In this edition of the newsletter, you can read contributions from our Emerging Technologies, 3D/TSV, and Reliability technical committees. The 2020 edition of the Heterogeneous Integration Roadmap (HIR) will also be made available early in the new year on the society website. My thanks to all our members on the twenty-three HIR technical working groups for making the roadmap an outstanding success.

For EPS, the most important priority is our members, staff, and volunteers' safety and well-being. Hence, many of our meetings and conferences have switched to online platforms while travel restrictions are in place. Recently we held our two regional flagship conferences—ESTC (Europe) and EPTC (Asia)—using online platforms with excellent participation from authors, keynote speakers, and delegates. We have come a long way in learning and experiencing what these online platforms can offer, and their capabilities continue to be enhanced. Led by Sam Karaikalan (VP conference), and looking at our conferences post-covid, we are investigating how mixed physical and online conferences could be organized for those conferences interested in running their events in this hybrid format. Guidance for our conference organizers will be made available on the website in 2021.

The end of 2020 also saw newly nominated members join our board of governors (BoG). My sincere thanks to Beth Keser, Grace O'Malley, and Adeel Bajwa, whose terms ended in 2020, for their

(continued on page 17)

NEWSLETTER SUBMISSION DEADLINES

15 June 2021 for Summer issue 2021

1 December 2021 for Winter issue 2022

Submit all material to d.manning@ieee.org

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2023 Term End: Regions 1-6, 7, 9—Mark Poliks, Annette Teng, Patrick McCluskey, Jin Yang, Region 8—Steffen Kroehnert, Region 10—Yoichi Taira, Young Professional—Yan Liu

Publications

Transactions on Components, Packaging and Manufacturing Technology

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Lecturers: Ramachandra Achar, Mudasir Ahmad, Kemal Aygün, Muhannad Bakir, Ph.D., W. Dale Becker, Wendem Beyene, Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., William T. Chen, Ph.D., Xuejun Fan, Ph.D., Philip Garrou, Ph.D., Subu Iyer, PhD., Beth Keser, Ph.D., Pradeep Lall, Ph.D., John H. Lau, Ph.D., Madhu Iyengar, Ravi Mahajan, PhD., James E. Morris, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Eric D. Perfecto, Mark Poliks, Ph.D., Jose Schutt-Aine, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Chuan-Seng Tan, Ph.D., Rao Tummala, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

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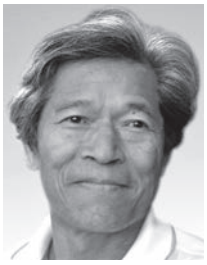
Chin C. Lee Receives the 2021 IEEE Electronics Packaging Technical Field Award



CHIN C. LEE
University of California, Retired
Irvine, CA USA

"For contributions to new silver alloys, new bonding methods, flip-chip interconnect, and education for electronics packaging."

The IEEE Electronics Packaging Award, sponsored by the IEEE Electronics Packaging Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

The 2021 Award will be presented virtually at the 71st Electronic Components and Technology Conference (ECTC), June 2021

Chin C. Lee's innovative bonding methods and materials and new packaging technologies have been integral to developing high-temperature and high-power electronics. His work on silver wire bond reliability resulted in a wider process window, lower cost, and higher yield in packaging components. He also discovered that silver alloy is anti-tarnishing, which has had enormous economic and technical impact for applications including optics, astronomy telescopes, and LED packaging. His fluxless soldering technology has enabled numerous bonding designs and is critical to packaging electronics for applications where oxidation effects from solder materials can be problematic. Lee also developed solid-state flip-chip interconnects and formulated quantum bonding theory. He established a materials and manufacturing technology graduate program in 2007 at the University of California, Irvine, which was one of a few such programs at that time.

An IEEE Life Fellow, Lee is a professor (retired) with the University of California, Irvine, CA, USA.

2020—Mitsumasa Koyanagi and Peter Ramm
"*For pioneering contributions leading to the commercialization of 3D wafer and die level stacking packaging*"

2019—Ephraim Suhir
"*For seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems.*"

2018—William Chen
"*For contributions to electronic packaging from research and development through industrialization, and for his leadership in strategic roadmapping*."

2017—Paul Ho and King-Ning Tu
"*For contributions to the materials science of packaging and its impact on reliability, specifically in the science of electromigration*."

2016—Michael Pecht
"*For visionary leadership in the development of physics-of-failure-based and prognosticsbased approaches to electronic packaging reliability*."

2015—Nasser Bozorg-Grayeli
"*For contributions to the advancement of microelectronic packaging technology, manufacturing, and semiconductor ecosystems*."

2014—Avram Bar-Cohen
"*For contributions to thermal design, modeling, and analysis, and for original research on heat transfer and liquid-phase cooling*."

2013—John Lau
"*For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging*."

2012—Mauro J Walker
"*For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and coopera-tive leadership in industry, government, academia, and profes-sional organizations*."

2011—Rao R. Tummala
"*For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging*."

2010—Herbert Reichl
"*For contributions to the integration of reliability in electronics sys-tems, and leadership in research and education in electronics packaging*."

2009—George G. Harman
"*For achievements in wire bonding technologies*."

2008—Karl Puttlitz Sr. and Paul A. Totta
"*For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages*."

2007—Dimitry Grabbe
"*For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards*."

2006—C. P. Wong
"*For contributions in advanced polymeric materials science and processes for highly reliable electronic packages*."

2005—Yutaka Tsukada
"*For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process*."

2004—John W. Balde
"*For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing*."

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www. ieee.org/awards

Renaming the IEEE Electronics Packaging Technical Field Award

The IEEE Electronics Packaging Award was established in 2002, and has been financially sponsored since its inception by the IEEE Electronics Packaging Society (EPS), formerly the IEEE Components, Packaging, and Manufacturing Technology Society (CPMTS). Recipient selection is administered through the Technical Field Awards Council of the IEEE Awards Board. The Award is presented to an individual or a team of not more than three, for outstanding contributions to advancing components, electronic packaging, or manufacturing. The award consists of a bronze medal, certificate, and cash prize of US$10,000.

In the evaluation process, the following criteria are considered: enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless, and micro-electromechanical systems (MEMS).

The IEEE EPS approved a proposal to change the name of the IEEE Electronics Packaging Award to the IEEE Rao Tummala Electronics Packaging Award at its Board of Governors meeting in November 2019. Professor Tummala is a visionary technologist, who provided unparalleled leadership in the industry (IBM), academia (Georgia Tech), professional societies (EPS and IMAPS), and around the globe in packaging research, technology development, manufacturing, and products, as well as in education, and in industry-academic collaborations. His efforts served to define the field of modern electronic packaging and his combined impact on the electronic industry, academia, and professional societies around the globe places him at the forefront of the packaging profession.

Beginning with the 2022 nomination process, the award will be renamed the IEEE Rao R. Tummala Electronics Packaging Award and endowed through the IEEE Foundation.

Newly-Elected and Appointed Members of the Electronics Packaging Society Board of Governors

In 2019, EPS members elected new Members- at-Large to the EPS Board of Governors for the three-year term of 1 January 2021 through 31 December 2023.

REGIONS 1-6, 7 & 9

F. PATRICK MCCLUSKEY (StM'85-M'91-SM'15) (B.S.('84) Lafayette College; M.S.('86) and Ph.D. ('91), Materials Science and Engineering, Lehigh University) is a Professor of Mechanical Engineering at the University of Maryland, College Park and the Mechanical Engineering Department's Division Leader for Design and System Reliability. He has over 25 years of research experience in the areas of thermal management, reliability, and packaging of electronic systems for use in extreme temperature environments and power applications. His research has been sponsored by NSF, NASA, DOE, DOD, ARL, ONR, along with leading component, module, and OEM manufacturers in the aerospace, automotive and energy industries.

Dr. McCluskey has authored/co-authored three books and four US patents, as well as over 150 peer-reviewed technical articles with over 3000 citations, including over 40 articles in IEEE journals and major EPS conferences, such as ECTC and iTHERM. He has also served as technical program or general chair of IEEE conferences on high temperature electronics and integrated power electronic packaging (e.g. 3D-PEIM), as well as being the organizer of the President's panel session on Power Module Integration at ECTC 2016. Dr. McCluskey has provided a short course on integrated thermal packaging of power electronics at ECTC and iTHERM since 2013.

He is an associate editor of the IEEE Transactions on Components, Packaging, and Manufacturing Technology, and is currently the chair of the EPS Technical Committee on Energy and Power Electronics, where he has led a team in writing the Integrated Power Packaging chapter of the IEEE Heterogeneous Integration roadmap. He has been a senior member of IEEE EPS since 2015 and an at-large member of the Board of Governors of the Electronic Packaging Society since 2018, where he has been active in the Education Committee, assisting in the development of guidelines for the EPS certificate program. He is a fellow of IMAPS and a member of ASME.

STATEMENT OF INTEREST

As heterogeneous integration of diverse components supplants Moore's law as the driver for performance improvement, a unique opportunity is presented to the electronics packaging community to lead next generation electronics products development. Continuing for another term on the Board of Governors will allow me to expand my work with the Education Committee with a focus on working with universities to develop and promote a heterogeneous integration focused electronic packaging curriculum consisting of Webinars and Courses for incorporation into university undergraduate and graduate programs and EPS certificates. Such a curriculum would highlight some of

the newer, non-traditional packaging technologies, such as integrated thermal and power packaging and 3D packaging using additive manufacturing. Another goal will be to work with the conferences and publications groups to develop new and expand existing conferences and publication venues to address these critical emerging packaging technologies needed to support heterogeneous integration. I would also use my contacts in the Power Electronics community to further collaborations with the IEEE Power Electronics Society (PELS) to enhance the impact of these efforts. Through these efforts, I hope to assist in making IEEE EPS the leading society for next generation electronics development.

MARK POLIKS (M'04) is Empire Innovation Professor of Engineering, Professor of Systems Science and Industrial Engineering, Professor of Materials Science and Engineering and Director of the Center for Advanced Microelectronics Manufacturing (CAMM) at the State University of New York at Binghamton. In 2006, he established the first research center (CAMM), to explore the application of roll-to-roll processing methods to flexible electronics and displays, with equipment funding from the United States Display Consortium (USDC) and the Army Research Lab. His research is in the areas of industry relevant topics that include high performance electronics packaging, flexible hybrid electronics, medical and industrial sensors, materials, processing, aerosol jet printing, roll-to-roll manufacturing, in-line quality control and reliability. He has received more than $20M in research funding from Federal, New York State and corporate sources and more than $30M in equipment funding from federal and state sources. He is the recipient of the SUNY Chancellor's Award for Excellence in Research. He leads the New York State Node of the DoD NextFlex Manufacturing USA and was named a 2017 NextFlex Fellow. He has authored more than one-hundred technical papers and holds forty-six US patents. Previously he held senior technical management positions at IBM Microelectronics and Endicott Interconnect. Poliks is a member of technical councils for the FlexTech Alliance, NBMC and NextFlex, and on the NextFlex Governing Council. He is an active member of the IEEE Electronics Packaging Society Electronic Component and Technology Conference and served and the 69th ECTC General Chair. Poliks received dual undergraduate degrees, with honors, in chemistry and mathematics from the University of Massachusetts and a Ph.D. from the University of Connecticut in materials science and engineering. He was a McDonnell-Douglas post-doctoral fellow working on solid-state magnetic resonance at Washington University, St. Louis before starting his career at IBM.

STATEMENT OF INTEREST

I have been an active member of IEEE and the CPMT Society/ Electronics Packaging Society for sixteen years. During this time, I have served the IEEE EPS ECTC community as a subcommittee member and subcommittee chair (for both materials and processing and interactive presentations), an executive committee member including ECTC General Chair in 2019 and currently serving as junior past general chair. My career has been nearly exclusively dedicated to advancement of materials, processing, fabrication and performance of electronics packaging. I have worked the first half of my career in industry (at the IBM Corporation and Endicott Interconnect) while part-time as a research professor and the second half as a full professor and tenured faculty member at the State University of New York, Binghamton. During this time, the importance of electronics packaging has continued to rise and is currently one of the primary means to achieve continued improvements in systems integration and performance. The IEEE Electronics Packaging Society has a unique opportunity to grow in size, importance and relevance within the larger IEEE community; EPS growth is essential to help to foster dialog and collaboration within the industry on the advancement of packaging and interconnect technologies. I seek to continue my active role in IEEE EPS and to work together with the EPS BOG and its members to help grow the outreach of EPS through new membership, industry roadmap working groups, conferences, peer-reviewed publications and professional education worldwide.

ANNETTE TENG (M'97-SM'01) is the Chief Technology Officer at Promex Industries, a manufacturer of electronic and medical components in Silicon Valley, since 2014. She has spent most of her career in electronic component packaging and manufacturing in both corporate and academic environments. Born in Borneo (Malaysia), she left at 16 to attend Sweet Briar College in Virginia. After Graduating from University of Virginia with a Ph.D. in Materials Science, she moved to Silicon Valley and started her career in the IC world at Signetics. She has worked in components packaging and assembly at Philips Semiconductor, Linear Technology Corp. and Corwil Technology. Prior to joining Promex, she was Package Assembly Manager at Silanna in Australia for 3 years.

She also worked at Hong Kong University of Science and Technology and helped launch their electronics packaging programs from 1997 to 2000. During that time, membership grew and many engineers and researchers working in packaging from Hong Kong chose ECTC to present their papers. Since returning to Silicon Valley in 2000, she had been an officer of the local Santa Clara Valley chapter, which was the main organizer for IEMT. Following trends where manufacturing moved from US to Asia, the IEMT was moved to Malaysia, which has now become the premier packaging conference in Malaysia celebrating its 39th year in 2020. She has published and presented papers at ECTC and MEPTEC in the areas of dicing, thinning, die attach films and package delamination. She has been active in IEEE-EPS Chapter activities in Silicon Valley since 2000 and is currently the Chair of the IEEE-EPS Santa Clara Chapter.

Dr. Teng is the 2018 recipient of IEEE EPS Regional Contributions Award and 1999 IEEE CPMT Presidential Award.

STATEMENT OF INTEREST

I have been very active and interested in membership and chapter development for IEEE EPS regional chapter. I am committed to ensure that the EPS chapter is relevant to packaging community

through dissemination of knowledge and providing opportunities for all who are interested in electronic packaging.

JIN YANG (M'09-SM'17) is a thermal architect with Intel Corporation located in Oregon USA. His research areas include, electronic and photonics packaging, and advanced package, component and system thermal management and microelectronics cooling. He has over 10 years of experiences in the areas of microelectronics manufacturing, electronic packaging and electronics cooling since he obtained his PhD degree in 2008. He was a senior staff engineer with Assembly, Test Technology Development (ATTD), Intel Corporation focused on next-generation disruptive thermal-mechanical technology development for meeting novel electronic package needs. He holds 14 US patents in the areas of electronic packaging and microelectronic cooling and has published over 30 peer-reviewed journal and conference papers. Prior to join Intel Corporation, Jin Yang obtained a PhD degree from Georgia Tech in Atlanta in the area of electronic packaging. Before that, he obtained his master degree and bachelor degree from Texas A&M University (College Station, TX) and Tsinghua University (Beijing, China) respectively.

Jin is an elected IEEE senior member and serves technical sub-committee chair of IEEE EPS (electronic packaging Society) ECTC and track chair of IEEE ITHERM. He has been a member of IEEE ECTC Assembly and Manufacturing Technology (AMT) committee since 2010 and served as assistant chair and chair for this committee for 2019 and 2020 respectively. During the last four years, he has served as track chair for IEEE IHTERM since 2016.

Outside IEEE, Dr. Yang has a long history of continued service to ASME community in the area of electronic and photonic packaging and has taken a leadership role in ASME Electronic and Photonic Packaging Division (EPPD). He serves as General Chair of InterPACK'2020 conference, flagship conference of ASME Electronic and Photonic Packaging Division (EPPD) and served as program co-chair and track chair in the last four years. He is Associate Editor of ASME Journal of Electronic Packaging (JEP). He once received Journal of Electronic Packaging Associate Editor of the Year Award. He is also a member of K-16 (K-16: Heat Transfer in Electronic Equipment). I served in ASME EPPD Technical Committee in 2009-2010. I also served as a liaison for over three years for SRC (Semiconductor Research Corporation) projects between the research institutions and participating companies and helped expedite research work and collaboration between them.

STATEMENT OF INTEREST

If I get an opportunity to be selected onto the EPS Board of Governors, I would like to participate and contribute to the activities in the areas of technology and conferences. In the area of electronic packaging, there is a strong connection to the industry and technology convolution and commercialization seems crucial to apply novel ideas and technology to the real applications and solving technical challenges the industry is facing. One program I contributed to has been in full HVM production through 5 years of pathfinding and development with an investment of $1.5 billion. One program I led goes into HVM production, which saves over tens of millions of dollars per year for the industry through the innovation and continued development. Meanwhile, if given an opportunity to be selected into EPS Board of Governors, I would like to contribute to the activities of conference EPS/IEEE organizes. One area is to establish a more active collaboration in the conference/event organized by IEEE with ASME technical division, including Electronic and Photonic Division since many professionals make their contributions to the area of electronic packaging through both IEEE EPS and ASME EPPD.

REGION 8

STEFFEN KROEHNERT (M'11) is a well-known component of the Packaging Community for more than 10 years. He is President & Founder of ESPAT-Consulting based in Dresden, Germany. Steffen is providing a wide range of consulting services around Semiconductor Packaging, Assembly, Interconnect Technologies and Test, mainly for customers in Europe. Utilizing his large network in industry, institutes and academic, he also supports small- and medium-sized companies as well as innovative Start-ups to find the right packaging solutions for their products and setup the supply chain from prototypes to small series and High Volume Manufacturing (HVM). Until June 2019, he worked for 22 years in different R&D, engineering and management positions at large IDMs and OSATs in Germany and Portugal, namely Siemens Semiconductors Regensburg (1997-1999), Infineon Technologies Regensburg and Dresden (1999-2006) and Qimonda Dresden and Porto (2006-2009), where Steffen was instrumental in developing FBGA packaging technology for DRAM products. As Director of Technology, he helped setting up and making visible the company NANIUM Porto and Dresden (2009-2017), the largest OSAT in Europe, where Steffen has been heading R&D during introduction of System-in-Package (SiP) and technology transfer and scaling from 200mm to 300mm reconstituted wafer format of the leading Fan-Out Wafer Level Packaging Technology embedded Ball Grid Array (eWLB) from Infineon Technologies. After acquisition of NANIUM by Amkor Technology served as Senior Director Technology Development in Porto and Dresden (2017-2019) working with the European Business Development team. Steffen founded and chaired the European SEMI integrated Packaging, Assembly and Test - Technology Community (ESiPAT-TC) inside SEMI Europe from 2016-2020, serving now as co-chair. His excellence in developing and innovating electronics packaging for semiconductor devices has resulted in authoring and co-authoring of 23 patent filings and many technical papers in the field of Packaging Technology. He co-edited the book "Advances in Embedded and Fan-Out Wafer Level Packaging Technologies". Since 2011, Steffen is co-chair of the Advanced Packaging Conference (APC) committee at SEMICON Europe, which is built of 22 packaging experts from European industry, institutes and academic. Steffen is active member of several technical and conference committees at IEEE EPS, IMAPS, SMTA and SEMI. He holds a M.Sc. degree in Electrical Engineering and Microsystems Technologies from the Technical University of Chemnitz, Germany.

STATEMENT OF INTEREST

With more than 20 years in the Semiconductor Packaging, Assembly, Interconnect and Test industry, and active participation in and contribution to industry associations such as SEMI, IEEE EPS, IMAPS and SMTA, I have developed a wide range of knowledge and experience and a very large network, allowing me now to consult mainly small- and medium-sized companies in the field, but also large EDA, Material and Equipment suppliers, in terms of packaging technologies, roadmaps and strategy. I'm focusing on the importance of the collaboration of the complete supply chain and promote a close collaboration. The EPS is a major element supporting the communication between the different players, and fostering collaboration along the semiconductor supply and value chain, and therefore, I want to actively contribute to, but also influence the work of the EPS, representing the European packaging community, supporting events, promoting new memberships, continuous learning, education in the field also to recruit the experts of the future, which have to work more interdisciplinary than ever before. In 2013, I initiated the Industry Interest Group ESPAT with up to 70 member companies, which later in 2015 became the SEMI Special Interest Group (SIG) European SEMI integrated Packaging, Assembly and Test (ESiPAT), today called Technology Community (TC), which I have been chairing for the last 4 years. This TC has the main objective to promote, maintain, strengthen and grow Semiconductor Packaging, Assembly, Interconnect and Test in Europe.

REGION 10

YOICHI TAIRA (M'89-LS'20) received his B.S. degree from Kyoto University and Ph.D. degree from University of Tokyo, both in Physics. From 1983 to1988, he was an Associate Professor with the Institute for Laser Science, University Electro-Communication, Tokyo. From 1988 to 2015, he was a Research Staff with IBM Research mostly in Tokyo. From 1989 to 1990, he was with IBM T.J. Watson Research Center. In 1998, he became an IBM Senior Technical Staff Member. Since 2015, he has been a Visiting Professor with Keio University. He is also involved in photonic packaging at IBM TJ Watson Research Center. He has been involved in various science and technology areas including technology research on various aspect of lasers including femtosecond laser technology, nonlinear optics, high power laser and UV lasers; VLSI design of memory and CPU; flat panel display technology including liquid crystal and organic light emitting materials; chip packaging including flip chip packaging, underfilling, chip cooling and chip stacking; high performance computer architecture including optical interconnects; nanometer precision fine molding technology, silicon photonic chip packaging and optically transparent adhesives He is the author of 5 books, more than 160 articles, and more than 60 inventions.

Some of the activities he is involved in for governing and administration of academic, society and related organizations include: Chair of IEEE EPS Japan Chapter; Auditor of Japan Institute of Electronics and Packaging (JIEP); General Chair of the 2017 Annual Meetings of Japan Institute of Electronics and Packaging; Chair of Optical Packaging Technology Committee in Japan Institute of Electronics and Packaging; Member of ECTC Materials and Processing Program Subcommittee.

His technical interest includes: Laser science and it application to computer communication; Sensors using optics; Display technology; Precision assembly of electronics/opto-electronic components; Chip cooling and systems cooling; System and network architecture and technology; Technology enabling advanced packaging.

STATEMENT OF INTEREST

I will contribute to EPS for its healthy growth through communications and collaborations between members in the region and worldwide and enhance technical activities.

YOUNG PROFESSIONAL

YAN LIU (M'14) is a Program Manager at Medtronic Inc. in Tempe, Arizona at United States. She has been working in the Process Development, Manufacturing Integration and Release Product Engineering groups, focusing on both new product introduction and release products of implantable medical devices, as well as developing new electronic packaging solutions and processes for implantable pacemakers, defibrillators, neurostimulator and other therapies.

Yan received her Ph.D degree in Materials Science & Engineering at Georgia Tech. Her research interest was microelectronics and photonics packaging. She published over 30 peer reviewed journal papers and is a referee for 10 journals including IEEE Transactions on CPMT. She received the Black Belt Certification of Design for Reliability and Manufacturability (DRM). She was the Young Professional Representative in IEEE Electronics Packaging Society in 2018 and a Member at Large since 2019, focusing on engaging young professionals in the EPS community. She initiated and led various Young Professional Events locally and at electronic packaging conferences, e.g. ECTC and ICEPT. She is also a subcommittee member of ECTC Materials and Processing since 2016. She received the IEEE Phoenix Section Outstanding Young Professional Award in 2017, the IEEE CPMT Outstanding Young Engineer Award in 2016, and the Best Paper Award of IEEE Transactions on Components, Packaging and Manufacturing Technology in 2014.

STATEMENT OF INTEREST

Engage, develop and increase the young professional (YP) members (target by 100% in 3 years) at different regions of EPS. Continue the YP events at EPS flagship conferences. Form the YP volunteer group to provide networking, career development, mentoring and job opportunities to YPs at different regions.

Congratulations to IEEE EPS Senior Members

New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between June and November 2020.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: https://www.ieee.org/membership/senior/

Mehmet Arik, Turkey Section
Noraini Othman, Malaysia Section
Anggoro Widiawan, Indonesia Section
Ramesh Kuchibhatla, Seattle Section
Michael Cosley, Chicago Section
Saranraj Karuppuswami, Southeastern Michigan Section
Nandish Mehta, Santa Clara Valley Section
Mitul Modi, Phoenix Section
Benson Chan, Binghamton Section
Stephen Consolazio, Chicago Section
Arkaprovo Das, Bangalore Section
Yuji Iwai, Santa Clara Valley Section
Jakub Korta, Poland Section
Dishit Parekh, Schenectady Section
Paragkumar Thadesar, San Diego Section

Congratulations to the 2021 Newly Elevated IEEE Fellows

Listed below are new IEEE Fellows who are members of the EPS. See a list of all EPS members who are IEEE Fellows in the IEEE Fellows Directory.

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Deepak Goyal
for contributions to fault isolation and failure analysis

Daoqiang Lu
for development of materials and manufacturing processes for mobile devices

Gamal Refai-Ahmed
for leadership in thermal management of electronics product development

EPS Membership Benefits

As the new year begins, all of us with the Electronics Packaging Society want to wish you the best for 2021. The new year also means we are closing in on the end of the membership renewal period in February, so now is a good time to provide our members some reminders of the benefits that come with their IEEE and EPS membership and provide updates on some of the membership-related activities that EPS is working on.

Saying that 2020 was a challenging year is an understatement, and IEEE and EPS provide a number of resources that are available to our members that can be helpful in both their professional and personal lives. Your EPS membership allows you to access an extensive library of online webinars on a variety of electronic packaging topics that are free for EPS members to access and view at any time. These webinars will soon be available through a new IEEE digital library interface that will be activated in early 2021. The EPS Certificate Program recognizes members for participating in webinars and other EPS technical activities through the accumulation of Professional Development Hours. The EPS Certificate Program is not only a way for members to acknowledge their technical efforts; it can also be an excellent professional development opportunity for managers and leaders to consider for their employees. EPS members receive online access to our society's journal, the IEEE Transactions on Components, Packaging and Manufacturing Technology, as part of their membership and receive discounts to a number of other IEEE journals as well. IEEE provides a number of helpful membership benefits in the form of discounts on various products and services, including technical publications and books, insurance, and IEEE society events and conferences. A complete list of these benefits can be found on the IEEE website at https://www.ieee.org/membership/benefits/index.html.

Hopefully, you saw the EPS survey that was emailed to all our members in December and took a few minutes to fill out. This survey will help us understand our member's opinions on the various

member benefits and programs offered by EPS and will serve to inform members about benefits they may not have known about. The results of this survey are expected in early January and we will be providing a summary of the findings and actions soon after.

One of our primary membership focus areas for 2021 will be in identifying and supporting members who are eligible for elevation to Senior Member. Members who have been in an IEEE-designated field for a total of 10 years and have demonstrated 5 years of significant performance are eligible to apply for elevation to Senior Member online. If you know someone who would be a candidate for elevation to Senior Membership, we hope you will suggest and support his or her application!

Finally, we want to mention our chapters and student chapters around the world. Getting involved in a chapter is a great way to network with other professionals in your area. The growth in our student chapters over the last 2 years has been tremendous with students and advisors organizing new chapters. EPS has established a program to provide financial assistance to existing and new student chapters. IEEE student members are also eligible for a special one-time 50% discount elevation from Student to Member grade upon their graduation through the IEEE Student Transition Elevation Partnership (STEP) program.

If you have questions or concerns about your EPS membership and the benefits that are included, please reach out to us…we want to help you get the most out of being part of EPS!

Alan Huffman
VP Membership

Student Chapter Promotion Programs

by Dr Andrew Tay, EPS Director of Student Programs

To promote the formation and continuation of EPS student chapters, EPS has recently initiated a couple of promotion programs. The Student Chapter Promotion Program (SCPP) is aimed at the formation of new student chapters while the Student Chapter Continuation Program (SCCP) is aimed at helping existing student chapters to remain viable.

Student Chapter Promotion Program (SCPP)

Under the SCPP, six students from any university which has an IEEE student branch who are willing to serve as executive committee (exco) members in a new student chapter will be given free IEEE+EPS student memberships. The exco must ensure that their student chapter remains viable for the year. This includes the organization of at least two technical activities per calendar year, holding of annual elections and timely submission of required activity and financial reports every year.

Additionally, faculty members who are willing to serve as Advisors to new student chapters will also be given free IEEE+EPS eMemberships where available, otherwise regular memberships will be provided. The Advisor's duties include advising on student chapter activities, endorsing financial statements where necessary, ensuring that annual election of new student exco members are held before end December, and required reports are submitted by the student exco in a timely manner every year.

An evaluation on the performance of subsidized student exco members and Advisors will be conducted in January each year based on reports submitted. Non-performing students and Advisors will not be subsidized for another year. While Advisors may be subsidized every year, student exco members can only be subsidized a maximum of two times in order to encourage a healthy succession of student leaders in the chapter.

The first phase of the SCPP for 5 new student chapters was launched in May 2019 and was over-subscribed by one. All 6 applicants were eventually approved. They are: Michigan State University, University of Florida, University of Maryland, Fudan University, State University of New York at Binghamton and Florida International University

A second phase of the SCPP to facilitate the formation of 10 more new student chapters in 2020/21 was launched in December 2019. Any student or faculty who are interested to form new EPS student chapters in their universities, *whether they are currently IEEE members or not*, can submit applications to the EPS Director of Student Programs, Dr Andrew Tay by emailing him at andrew_tay@ieee.org listing the names and email addresses of 6 students from the same university who are committed to serve as exco members in the new student chapter, and the name and email address of a faculty who is committed to serve as the chapter Advisor. To date, under this second phase, 3 EPS student chapters have been established in the TU Cluj-Napoca, Romania; Georgia Institute of Technology, USA; University of Waterloo, Canada. One more university, Wuhan University, China, has been supported and is presently awaiting IEEE approval of their petition to form a new EPS student chapter.

Student Chapter Continuation Program (SCCP)

Another program, the Student Chapter Continuation Program (SCCP) has also been initiated to facilitate the continuation of existing EPS student chapters. Similar free IEEE+EPS memberships will be given to six students in a university with an existing EPS student chapter who are willing to serve as executive committee (exco) members in the student chapter, and to a faculty who agrees to serve as the Advisor to the student chapter. For this initial launch, any student or faculty who are interested to continue the existing EPS student chapter in their universities, *whether they are currently IEEE members or not*, can submit applications to the EPS Director of Student Programs, Dr Andrew Tay by emailing him at andrew_tay@ieee.org listing the names and email addresses of 6 students from the same university who are committed to serve as exco members in the student chapter, and the name and email address of a faculty who is committed to serve as the chapter Advisor. The existing EPS student chapters are at Tsinghua University, Politechnica Univ of Bucharest, Universidade Federal do ABC, Singapore University of Technology & Design, Universidade Estadual Paulista—Guaratingueta, San Jose State University and University of California-Los Angeles.

Annual Subsidy for Student Chapters

To support the organisation of technical activities by student chapters, the exco may apply for subsidies of US$1000 per annum from EPS. For new chapters in their first year, the subsidy is US$1500.

Technical Webinars by Electronics Packaging Society (EPS) Organized by Universiti Malaysia Perlis (UniMAP) in Conjunction with IEEE Day 2020

(Compiled by Ir. Dr. Banu POOBALAN)

IEEE Day is an annual celebration event hosted by Universiti Malaysia Perlis (UniMAP) and several IEEE societies including Electronics Packaging Society (EPS). IEEE Day for the first time in the history was celebrated when engineers worldwide and IEEE members gathered to share their technical ideas in 1884. IEEE Day celebration carries the theme, which emphasizes on Leveraging Technology for a Better Tomorrow. While the world benefits from what's new, IEEE focuses on what's next. IEEE Day is celebrated on the first Tuesday of every October as an annual event. In the year of 2020, for the 11th consecutive year, IEEE Day worldwide celebration was initiated on Tuesday (6th October 2020) and continued throughout the first two weeks in October.

In conjunction with IEEE Day 2020, EPS once again succeeded in its mission of constantly motivating the local engineering community with technical knowledge sharing session from the internationally respected speakers. However, due to the Covid-19 pandemic, this year, the technical sharing was conducted via online webinars.

It's our honor to have invited semiconductor packaging industry's notable speakers, presenting three topics of interest: (1) First Speaker: Dr Andy Mackie (Principal Engineer & Manager, Thermal Interface Material Applications, Indium Corporation) on "What's Driving—Automotive Electronics Assembly and Packaging" (2) Second Speaker: Prof Chris Bailey (President, IEEE Electronics Packaging Society) on "Overview of the IEEE Electronics Packaging Society" (3) Third Speaker: Dr Ravi Mahajan (Director, Technology & Manufacturing Group Intel Corporation) on "Direction and Opportunities in Heterogeneous Integration using Advanced Packaging".

Dr Andy Mackie covered the introductory overview of advanced automotive packaging technology trends, main market players and a prospective outlook on related future growth. This talk was attended by over 200 participants; mainly from industry, academic and international backgrounds. Prof Chris Bailey highlighted on the overview of IEEE EPS, achievements, membership benefits and packaging technology advancement. This talk was attended mainly by academics, industry key players and Heterogeneous Integration with some international participants. The third speaker Dr Ravi Mahajan discussed about the technology opportunities and challenges in heterogeneous integration of Interconnect in 2D and 3D. This talk was well received by industry, academicians and international participants.

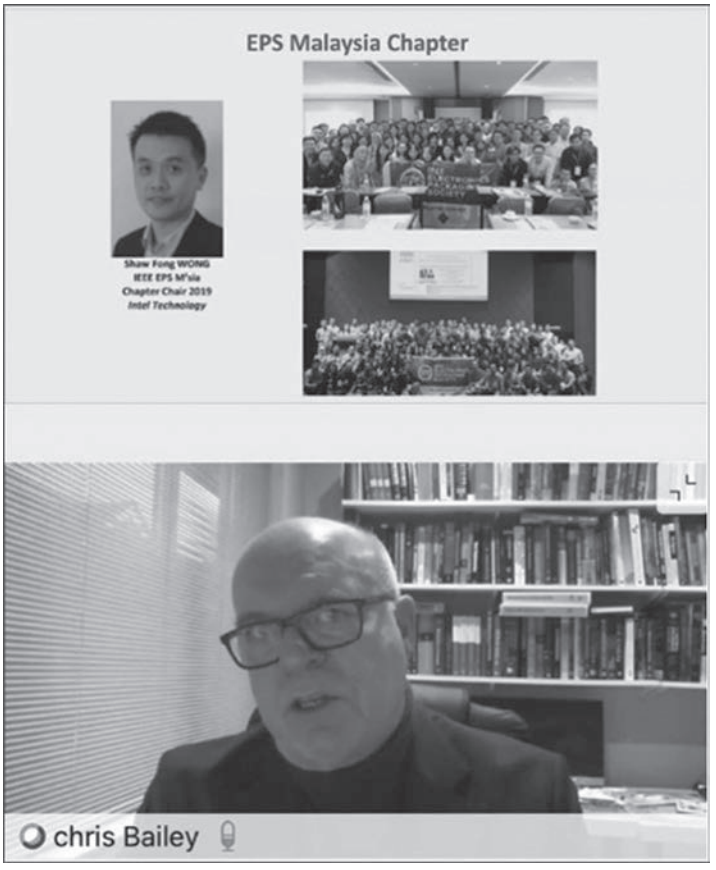


Figure 2. The webinar delivered by Prof Chris Bailey from president of IEEE Electronics Packaging Society.

We would also like to thank Universiti Malaysia Perlis (UniMAP) for the continued commitment and support of this annual event. We are looking forward for a grand IEEE Day 2021 event next year once COVID-19 is behind us!!!

Technical Webinars by Electronics Packaging Society (EPS)

(Compiled by Ir. Dr. Banu POOBALAN)

EPS Webinar Series 2020/21 event hosted by Electronics Packaging Society (EPS) Malaysia Section consist of a string of webinars conducted online as a knowledge sharing platform for participants from all over the world in the industry

Figure 1. The webinars schedules, topic titles and speakers information.

and academic fields. The Webinar Series 2020/21 initiated in the month of December 2020 and it will be continued throughout the year of 2021.

It's our honour to have invited one of the semiconductor packaging industry's notable speakers, Dr HongWen Zhang presenting topic entitled "The Evolution of Lead-free Solder Alloys". Dr. HongWen Zhang is Manager of the Alloy Group in Indium Corporation's Research & Development Department. His focus is on the development of lead-free solder materials and the associated technologies for high-temperature and high-reliability applications. Dr. Zhang has extensive experiences in various aluminum (Al) alloys and fiber/particle-reinforced Al-based composite materials, and Al-rich and ZrHf-based amorphous alloys. The webinars schedule, topic title and speakers information as per presented in Figure 3.

This talk highlighted the evolution of lead-free solder alloys. As the world is moving towards green manufacturing, lead-free soldering, originally driven by RoHS (Restriction on the use of Hazardous Substances in electrical and electronic equipment) of Europe, the Sn-rich alloys, including SnAgCu, SnAg and SnCu were becoming the mainstream for electronic industry. While the electronic industry keeps advancing rapidly towards miniaturization, two more important drivers actually dictate the evolution of lead-free solders—low cost, and high reliability. This talk briefed the evolution of lead-free solders after the implementation of lead-free soldering in industry from 2006, covering (1) the first generation high-Ag SAC solders; (2) the low Ag/zero Ag Sn-rich solders; (3) the high-reliable SAC solders; (4) the low temperature lead-free solders and (5) high temperature lead-free bonding materials. In each session, the market need, the pros and cons of the representative materials in each group were discussed. This webinar was attended mainly by academics and industry key players with some international participants.

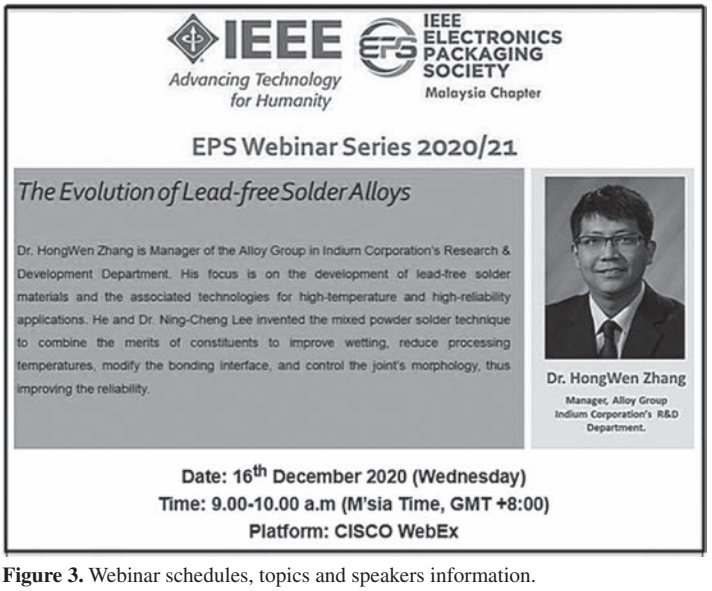
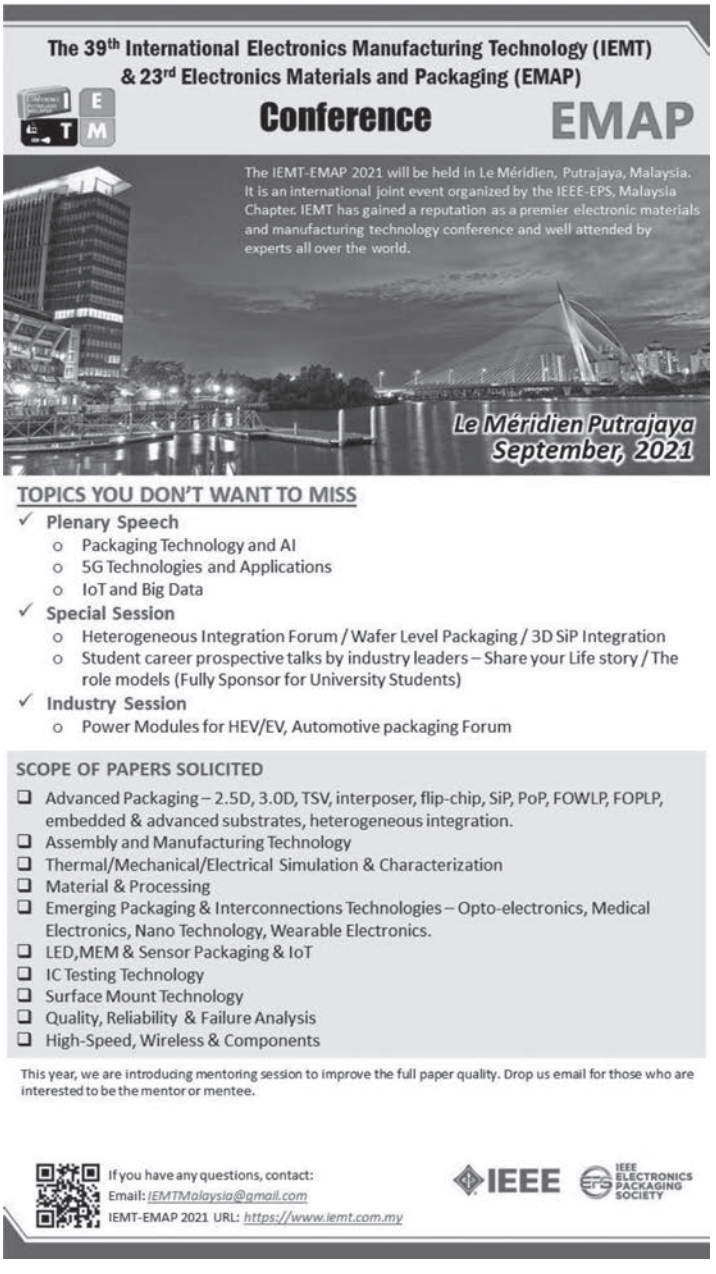


Figure 3. Webinar schedules, topics and speakers information.

In summary, this technical webinars were very informative, of all participants truly get inspired by the quality and quantity of late-breaking developments of emerging lead-free solder alloys technologies. We on behalf of EPS Malaysia Section would also like to thank Dr HongWen Zhang for his commitment and valuable sharing via this series webinars.

39th International Electronics Manufacturing Technology (IEMT) & 23rd International Electronics Materials and Packaging (EMAP) Conference 2021



Call for Papers
Special issue in the memory of Professor Avram Bar-Cohen

Professor Avram Bar-Cohen, past President of IEEE Electronics Packaging Society, and past Editor-in-Chief of the IEEE Transactions on Components and Packaging Technologies passed away on October 10, 2020. He was a giant in the field of thermal management, and made seminal research and professional contributions over a five decade period. Professor Bar-Cohen's research focused on several areas in microsystems packaging. His work on air cooling focused on optimization of natural and forced air cooling devices, and sustainability and life cycle considerations of thermal management devices. His work spanned the spectrum from fundamental research to emerging applications, including 2.5D and 3D heterogeneous integration, radio frequency, opto-electronics, and power electronics devices and systems.

Professor Bar Cohen's research on two-phase heat transfer focused on submerged condensers, pool boiling of dielectric coolants, enhanced surfaces, flow boiling in microgaps, and flow regime characterization in microchannels. With the ongoing move towards heterogeneous integration and three-dimensional packaging technologies, Professor Bar-Cohen recognized the potential of evaporative cooling for such applications. While serving as Program Manager for the Defense Advanced Projects Research Agency (DARPA), he initiated the IceCool Fundamentals program for the exploration of high exit vapor quality two-phase cooling for emerging microelectronics architectures. During 2020, he co-organized a workshop under the sponsorship of the Office of Naval Research to assess understanding of evaporative thermal management and identify research gaps and barriers to implementation of this cooling technique, with a particular focus on fundamental understanding of high vapor quality two-phase flows.

A Special Issue of the IEEE Transactions on Components, Packaging and Manufacturing Technology is planned for publication in 2021. Papers on analytical, numerical, and experimental investigations of thermal management of microsystems are solicited for this Special Issue. Topics include, but are not limited to, the following.

Computational simulations of single and two-phase cooling
Air cooling enhancements
Optimization of air cooled systems
Sustainability considerations in design of thermal packaging
Thermal management of 2.5D and 3D heterogeneous microsystems
Thermal management of emerging radio frequency, optoelectronics, and power electronics devices and systems
Fundamentals of boiling processes in micro/nanoscale devices and systems
Two-phase thermal management devices
Novel metrology techniques for two-phase flow
Materials and surface enhancements in boiling
Capillary flow driven two-phase devices
Multi-disciplinary cross-cutting topics in liquid cooling, including fluids, reliability, erosion modeling

The Special Issue is planned to be published in July 2021, in memory of Professor Bar-Cohen's 75th birthday. The publication deadlines are:

Draft manuscript submission: January 30, 2021
Author notification on manuscripts: March 15, 2021
Revised manuscripts due: April 15, 2021
Final decision on manuscripts: April 30, 2021
Final manuscripts due: May 15, 2021

The following organizers of the Special Issue may be contacted for further information or questions.

Dr. Sushil H. Bhavnani
Henry M. Burt, Jr. Professor
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Auburn University
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Professor and McKenney/Shiver Distinguished Chair
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Electronics Packaging Society Section Within IEEE Access

The Electronics Packaging Section within IEEE *Access* will draw on the expert technical community to continue IEEE's commitment to publishing the most highly-cited content. The Journal peer-review process targets a publication period of 6 weeks for most accepted papers. This journal is fully open and compliant with funder mandates, including Plan S.

This is an exciting opportunity for your research to benefit from the high visibility of IEEE *Access*. Your work will also be exposed to 5 million unique monthly users of the IEEE *Xplore*® Digital Library.

Scope

The IEEE Electronics Packaging Society section in IEEE Access covers the scientific, engineering, and production aspects of materials, components, modules, hybrids and micro-electronic systems for all electronic applications, which includes technology, selection, modeling/simulation, characterization, assembly, interconnection, packaging, handling, thermal management, reliability, testing/control of the above as applied in design and manufacturing. Examples include optoelectronics and bioelectronic systems packaging, and adaptation for operation in severe/harsh environments. Emphasis is on research, analysis, development, application and manufacturing technology that advance state-of-the-art within this scope.

Get Published in the New Electronics Packaging Society Section of IEEE Access

Go to: https://mc.manuscriptcentral.com/ieee-access

Select the Electronics Packaging Society (EPS) Section from the pull-down menu of "Manuscript type" in the first page of the submission process.

Author Information and Instructions

EPS is committed to supporting authors and researchers with IEEE Author Tools including the IEEE Publication Recommender, IEEE Graphics Analyzer, LaTeX Analyzer and more. Discover the tools available at the IEEE Author Center - https://ieeeauthorcenter.ieee.org/ieee-author-tools/.

The EPS is regarded as a trusted and unbiased source of technical information for dialog and collaboration to advance technology within the computing community. EPS is led by researchers and technology professionals who are at the center of respected electronics packaging communities where readers and authors already come together.

The articles in this journal are peer reviewed in accordance with the requirements set forth in the IEEE Publication Services and Products Board Operations. Each published article is reviewed by a minimum of two independent reviewers using a single-blind peer review process, where the identities of the reviewers are not known to the authors, but the reviewers know the identities of the authors. Articles will be screened for plagiarism before acceptance.

Article Processing Charge (APC): US$1,750

IEEE Members receive a 5% discount.
IEEE Society Members receive a 15% discount.
These discounts cannot be combined.

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Dale Becker, IBM Inc., USA
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Publication Year: 2015, Page(s):1339–1349

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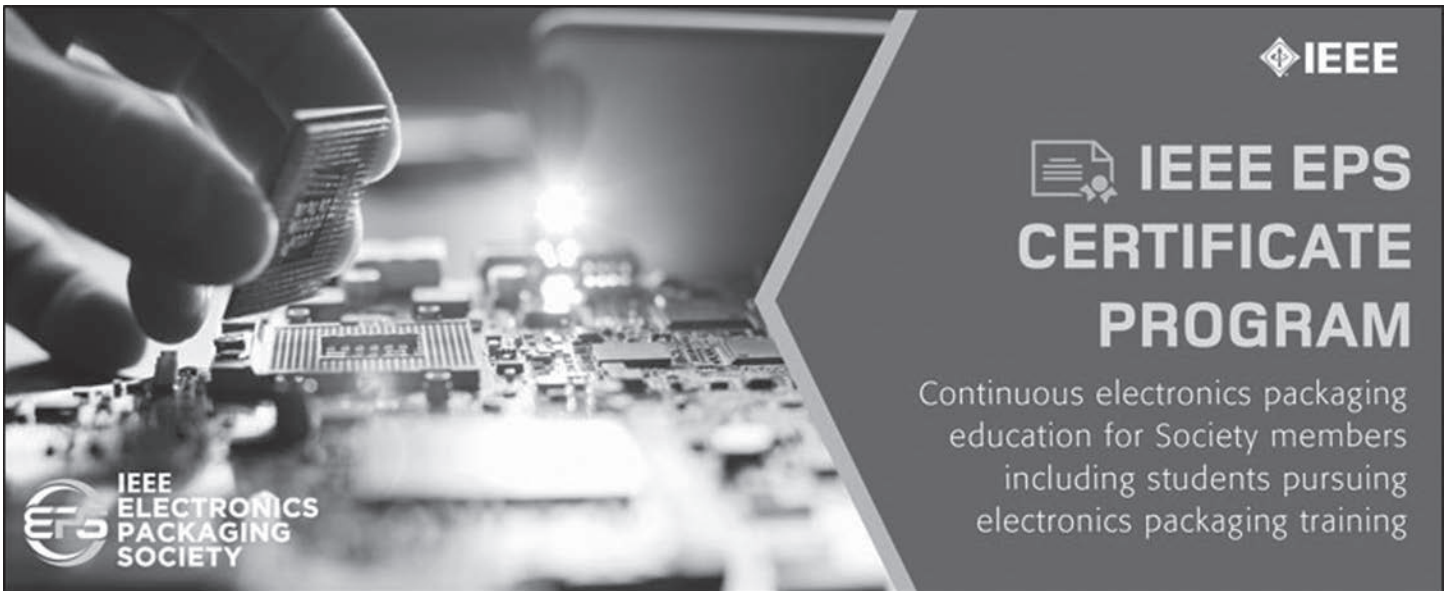
Jaehyun Choi; Dooseok Choi; Jongwoo Lee; Woonbong Hwang; Wonbin Hong
Publication Year: 2020,Page(s):1–1

77/79-GHz Forward-Wave Directional Coupler Component Based on Microstrip and SIW for FMCW Radar Application

Yongrong Shi; Xin Yi; Wenjie Feng; Yongle Wu; Zhengyong Yu; Xingcheng Qian
Publication Year: 2020,Page(s):1879–1888



Comprehensive EPS Certificate Program

The IEEE Electronics Packaging Society is pleased to announce that it has expanded its Certificate Program to include a new *EPS Distinguished Achievement Certificate*. This new level of recognition builds on the initial *EPS Achievement Certificate* aimed at early-career professionals, and provides a pathway for mid-career to late-career professionals to highlight their more advanced level accomplishments.

EPS Achievement Certificate

The EPS Certificate Program was initially established in January 2019 to encourage continuing education and professional development of EPS members. The original offering consisted of an *EPS Level One Achievement Certificate* that can be earned by completing 15 Professional Development Hours (PDHs) of continuing education in the area of electronics packaging. A variety of mechanisms exist to satisfy the continuing education requirement including attending online IEEE EPS Webinars (1 PDH per 1 hour webinar), attending registered Professional Development Courses (PDCs) at one of the EPS Conferences (ECTC, EPTC, and ESTC) (1 PDH per hour of PDC course attendance), authoring papers at EPS sponsored conferences and the IEEE CPMT Transactions that are published in IEEE Xplore (5 PDH per published conference/journal paper), and serving as a reviewer for IEEE CPMT Transactions papers (5 PDH per 3 reviews completed). Once an EPS member has achieved at least 15 PDHs through a combination of the above approaches, he/she can then self-nominate for the Certificate via an online form at https://eps.ieee.org/education/eps-certificate-program.html.

The first level *EPS Achievement Certificate* is aimed at early-career professionals working in the field of electronics packaging. It is especially intended to encourage the career development of young professionals including advanced graduate students. To date, over 25 EPS members have been recognized. Since there was an overwhelming response to the initial program, the EPS


IEEE

EPS CERTIFICATE OF ACHIEVEMENT

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in Recognition of

Having Completed 15 Hours of Professional Development Continuing Education in the Field of Electronics Packaging

Awarded on January 1, 2021

EPS President

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IEEE ELECTRONICS PACKAGING SOCIETY

Vice President Education formed an adhoc Committee from members of the EPS Education Functional Team to further develop the Certificate Program. In particular, the goal was to add a new more advanced certificate that could capture an individual's technical growth, technical and service contributions, and other achievements. This process resulted in the establishment of a new *EPS Distinguished Achievement Certificate* that was recently approved by the EPS Board of Governors.

EPS Distinguished Achievement Certificate

This new level of recognition builds on the *EPS Achievement Certificate* that is earned by achieving 15 PDHs of continuing education, and provides a pathway for mid-career to late-career professionals to highlight their more advanced level continuing education and career accomplishments. The new *EPS Distinguished Achievement Certificate* will be awarded for advanced technical and service

contributions to the industry and EPS. Two different categories of recognition are offered:

- Distinguished Achievement Certificate for Technical Leadership and Expertise
- Distinguished Achievement Certificate for Professional Engagement and Service

For either area of recognition, the nominee's strengths will be evaluated against prescribed criteria described in more detail below. As with the *EPS Achievement Certificate*, people interested in receiving the *EPS Distinguished Achievement Certificate* must self-nominate via an online Form. The nominee should first review the specific certificate requirements in each recognition area, and choose which one he/she wants to apply. The nominee should review the certificate requirements to assess themselves against the criteria and to prepare their supporting paperwork.

Distinguished Achievement Certificate for Technical Leadership and Expertise

There are five high-level focus areas for this new certificate. These areas include: (1) being recognized authority of technical expertise in one's field; (2) being a subject matter expert (SME) at conferences, keynotes, webinars, blogs; (3) demonstrating sustained technical contributions to industry; (4) documenting advanced technical recognitions; and, (5) being endorsed strongly by others. Examples of being a recognized authority of technical expertise include being an advanced member of the technical staff at a company (e.g. Fellow, Senior Technical Staff, Distinguished Engineer, etc.), making technical contributions as a Member or Fellow of professional associations/societies related to electronics packaging (e.g., IEEE, IMAPs, SMTA, ASME, etc.), and being an invited speaker at companies, technical conferences, and EPS Chapter meetings. Methods to demonstrate participation as a SME include abstracts accepted and papers presented at conferences, giving keynote lectures at conferences or professional society meetings, presenting webinars for EPS and other IEEE Societies, and serving on technical panels at conferences and other venues. Example approaches to demonstrate sustained technical contributions to industry include publishing well-cited technical papers at conferences and in journals, book chapters, and patents; serving as an editor of a journal or reference book; and being a leader or participant in industry blogs, focus groups, technical roadmaps, newsletters, and forums. Methods to document technical recognitions include receiving technical awards from a company, institute, professional society, or academic institution; being the acknowledged inventor of a seminal technology or process important to industry; serving as the point person for global high-level task force activity; and being elected to be a Member of an organization such as the US National Academy of Engineering, Royal Academy of Engineering, Chinese Academy of Engineering, IBM Academy of Technology, etc.

Distinguished Achievement Certificate for Professional Engagement and Service

There are four high-level areas of focus for this new certificate. These areas include: (1) demonstrating leadership in the electronics packaging field; (2) illustrating broad impact/influence in the electronics packaging field, (3) providing extensive service and "give back" to the profession and/or industry; and (4) being endorsed strongly by others. Leadership and broad impact activities in electronics packaging can be documented from outstanding accomplishments during industry employment or for notable volunteer contributions to the profession and society. Examples of significant professional service include serving as an officer in a technical society at the international, national, or local chapter level; participating in packaging related technical committees, councils, or affinity groups; contributing to technology roadmaps such as the Heterogeneous Integration Roadmap (HIR); and receiving a professional society or industry award based on service contributions. Documentation of "give-back" to one's technical community can be accomplished via demonstrations of coaching and mentoring of co-workers, young professionals, and students.

More details on the Certificate Program are available on the EPS website at https://eps.ieee.org/education/eps-certificate-program.html. The EPS Certificate Program is sponsored by the IEEE EPS VP Education and is offered only to EPS members. For questions, please contact Jeff Suhling (jsuhling@auburn.edu).

EPS Resource Center

The IEEE EPS Resource Centers contains valuable, technical content from reputable experts to enhance research or industry work, implement trainings, or earn CEU/PDH credits--all of which are universally available on demand.

IEEE EPS Resource Centers benefits include:

- Access to valuable technical community content
- Access to content 24 hours a day, 7 days a week through an easy-to-use global portal
- Available at no cost for EPS members
- Opportunities to earn CEUs and PDHs

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- Heterogeneous Integration Roadmap Driving Force and Enabling Technology for System of the Future
- Overview of the High-Performance Computing Chapter of the Heterogeneous Integration Roadmap
- Thermal Management Challenges and Opportunities for Heterogeneous Packages
- Power Electronics Packaging, Reliability, and Thermal Management

https://resourcecenter.eps.ieee.org/

Upcoming webinars from the EPS Santa Clara Valley (SCV) Chapter. If your Chapter is interested in co-sponsoring, please contact the SCV Chapter Chair—annette@ieee.org.

You can register here: https://ieee-region6.org/scv-eps/

Virtual for 2021	California Time	Speaker Location	Title	Speaker		Speaker Affiliation
Jan 28, 2021	Noon	St. Paul, MN	High performance & reliable aerosol jet printed 3D interconnects for bare die & components	Bryan Germann	bgermann@optomec.com	Optomec
Feb 11, 2021	Noon	San Jose	Design analysis of chiplet interfaces for heterogenous systems	Wendem Beyene, DL	wendem@gmail.com	
Feb 24–26, 2021	Half days for 3 days	Binghamton	HIR 4th Annual Meeting	12 Working Group sessions over 3 days	william.chen@aseus.com	
Mar 18, 2021	Noon	Auburn, AL	Additively-printed multilayer flexible substrates with Z-axis interconnects	Pradeep Lall, DL	lallpra@auburn.edu	Auburn U.
April 15, 2021	Noon	Helsinki, Finland	Sustainable electronics	Mervi Paulasto-Krockel, DL	mervi.paulasto@aalto.fi	Aalto U., Finland
May 13, 2021	Noon	Boston, MA	Packaging for quantum computing	Rabindra Das	rabindra.das@ll.mit.edu	MIT Lincoln Lab
June 10, 2021	8:00 AM	St. Florian, Austria	Low temperature wafer bonding	Jurgen Burggraf	j.burggraf@evgroup.com	EVG
June 17, 2021	8:00 AM	Enschede, Netherlands	Photonics assembly	Brad Snyder, Jeroen Duis	bradley.w.snyder@gmail.com	PHIX

President's Column (*Continued from page 1*)

contributions to our community during their time on the BoG. And a warm welcome to our new and continuing members—Mark Poliks, Patrick McCluskey, Annette Teng, Jin Yan, Xuejun Fan, Steffan Kroehnert, Yoichi Taira, and Yan Liu. I am also delighted to welcome Kitty Pearsall as our new President-Elect.

The coming years are exciting times for our society, with developments in electronics packaging viewed as a critical differentiator for future electronics systems by the whole electronics industry. I look forward to working with the EPS Board of Governors and our volunteers worldwide throughout 2021 to deliver our strategic goals and continue to provide the unique service that IEEE EPS can offer you, our members, and our industry.

Please stay safe, stay well, and hopefully, there will be opportunities to meet in a less-distanced manner soon.

Chris Bailey

Upload Abstracts

66th IEEE HOLM CONFERENCE

Hilton Palacio Del Rio
San Antonio, Texas

24-27th October, 2021

This is to inform you that our website is now open for accepting abstracts for the conference. To submit go to: www.ieee-holm.org or https://www.softconf.com/l/holm21

The program committee will review the abstracts at a meeting on Feb 10, 2021. Please submit your abstract by **Feb 9, 2021**. The website will guide you through the process. If you have last year's ID and password, you can use it. If you are new you will be guided through the registration. If you encounter any problems with your upload, or have a question please email Prof. Robert Jackson at the following: jacksr7@auburn.edu.

Authors will be notified on your abstract status shortly after our committee meeting.

We expect a very good conference this year and our committee looks forward to your participation in our technical program. Looking forward to seeing you in San Antonio.

Best regards,

Xin Zhou
Conference Chair

Robert Jackson
Technical Program Chairman

Symposium on Reliability for Electronics and Photonics Packaging (REPP)—*reliability, failure modes and testing for integration of electronics and photonics (SiPh).*

https://attend.ieee.org/repp/

This new symposium was held virtually, from Silicon Valley on ***November 12-13, 2020*** with sponsorship from IEEE Silicon Valley chapter and EPS and was colead by chairs of Technical committee's of Photonics and Reliability.

This symposium's focus was on quantified reliability, accelerated testing and probabilistic assessments of the useful lifetime of electronic, photonic, MEMS and MOEMS materials, assemblies, packages and systems in electronics and photonics packaging.

Keynote Presentations that were made are listed below:

— Reliability Challenges for the Aerospace Sector and the Use of Commercial Off-The-Shelf Components (COTS), Chris Bailey, University of Greenwich

— Emerging Reliability Challenges: Solutions from Architecture to Layout for Large SoCs and 3DICs, Dr. Norman Chang, ANSYS;

— Reliability Challenges in Advanced Packaging, Dr. Subramanian Iyer, UCLA;

— Reliability Challenges for Electronics and Photonics Packaging for Deep Space, Dr. Reza Ghaffarian, JPL/NASA;

— Highly Reliable Silicon Photonics DWDM modules, Dr. Ranjani Muthiah, Inphi Corp;

— Electronics Quality and Reliability for Critical Applications that Adopt New Technologies and Designs, Dr. Alan Lucero, Intel Corp;

— Evolution of Data Center Optics Packaging Technology and Reliability Challenges, Dr. Omer Khayam, Google Technical Infrastructure;

— Silicon Photonics: State-Of-The-Art, Challenges, and Future Requirements, Dr. Vipul Patel, Cisco;

And in addition this symposium included four sessions of papers.

Many of the keynote sessions and the session papers recordings can be viewed in the Program section of symposium webpage.

All the sessions of the symposium were well attended. Details for the symposium for 2021 will be coming out shortly. One can signup through the mailer of the symposium to get regular updates.

Submitted by :
Gnyan Ramakrishna
General Chair, REPP 2020.

ESTC 2020—A Review

ESTC 2020 was planned in Vestfold, Norway, 15-18 September 2020, organized by University of South-Eastern Norway (USN). It took place at these dates, live on a virtual platform. We are happy and proud to state that the virtual ESTC 2020 was a success: 245 registered attendees, discussions after the presentations quite similar to a regular on-site conference, and also with questions from anonymous people that might not have appeared in a physical conference. "Poster pitch" videos allowed exposure of the poster presentations to the plenary audience. Recordings of sessions were available for two weeks after the conference, giving attendees the opportunity to see the parallel sessions they couldn't catch live.

Highlights of ESTC 2020 include:

- Five keynotes, addressing the future of a broad variety of technologies and market segments: Autonomous shipping; Fan-out Wafer and Panel Level Packaging; Smart Sensors for Agriculture; Quantum Computing; Artificial Intelligence for Ensuring Reliability
- Three plenary Special Sessions, looking at past, present and future of electronics, organizations and society: The history of Silicon Valley; Masculine and feminine roles in organizations; A look into the bright future after Moore's Law

- A Workshop on the Heterogeneous Integration Roadmap (HIR), setting the directions for future development in the field of Electronics System-Integration
- 124 presented papers, extracted from 194 submitted abstracts
  - 92 oral presentations in parallel sessions
  - 32 interactive poster presentations, including 1-minute pitch video in plenary session
  - 24 countries represented, from Europe, Asia, North & South America
  - The 8 countries with highest number of papers: Germany (33), Norway (19), France (9), Belgium (8), Finland (8), Romania (7), United Kingdom (7), Japan (6)
- A virtual exhibition, with virtual booths for direct contact with exhibitors
- Virtual company visits to some of Vestfold's electronics/ microsystem companies, specializing towards different market segments that require high quality and high reliability, such as aerospace and medical applications.

Now, we look forward to EMPC 2021 (Gothenburg, Sweden) and ESTC 2022 (Sibiu, Romania)!

On behalf of the Organizing Committee,
Knut E Aasmundtveit, University of South-Eastern Norway (General Chair)
Kristin Imenes, University of South-Eastern Norway (Executive Chair)
Paul Svasta, University Politehnica of Bucharest, Romania (Technical Programme Chair)

Top Conference Papers Based on 2020 Usage

2020 IEEE 70th Electronic Components and Technology Conference (ECTC)

(June 3 – 30, 2020)

Magnetic Inductor Arrays for Intel® Fully Integrated Voltage Regulator (FIVR) on 10th generation Intel® Core™ SoCs
Malavarayan Sankarasubramanian; Kaladhar Radhakrishnan; Yongki Min; William Lambert; Michael J Hill; Ashay Dani; Ryan Mesch; Leigh Wojewoda; Jose Chavarria; Anne Augustine

InFO_SoW (System-on-Wafer) for High Performance Computing
Shu-Rong Chun; Tin-Hao Kuo; Hao-Yi Tsai; Chung-Shi Liu; Chuei-Tang Wang; Jeng-Shien Hsieh; Tsung-Shu Lin; Terry Ku; Douglas Yu

Ultra High Density SoIC with Sub-micron Bond Pitch
Y. H. Chen; C. A. Yang; C. C. Kuo; M. F. Chen; C. H. Tung; W. C. Chiou; Douglas Yu

Die to Wafer Stacking with Low Temperature Hybrid Bonding
Guilian Gao; Thomas Workman; Cyprian Uzoh; K. M. Bang; Laura Mirkarimi; Jeremy Theil; Dominik Suwito; Rajesh Katkar; Gill Fountain; Gabe Guevara; Bongsub Lee h

Scalable Chiplet Package Using Fan-Out Embedded Bridge
Joe Lin; C. Key Chung; C. F. Lin; Ally Liao; Ying Ju Lu; Jia Shuang Chen; Daniel Ng

2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(July 21 – 23, 2020)

Embedded Microchannel Cooling for High Power-Density GaN-on-Si Power Integrated Circuits
Remco van Erp; Georgios Kampitsis; Luca Nela; Reza Soleimanzadeh Ardebili; Elison Matioli

Topology Optimization of Manifold Microchannel Heat Sinks
Yuqing Zhou; Tsuyoshi Nomura; Ercan M. Dede

Coupled Electro-Thermal Analysis of Permanent Magnet Synchronous Motor for Electric Vehicles
Amitav Tikadar; Nitish Kumar; Yogendra Joshi; Satish Kumar

Additively Manufacturing Nitinol as a Solid-State Phase Change Material
Darin J. Sharar; Adam A. Wilson; Asher Leff; Andrew Smith; K. Can Atli; Alaa Elwany; Raymundo Arroyave; Ibrahim Karaman

3D Wafer-to-Wafer Bonding Thermal Resistance Comparison: Hybrid Cu/dielectric Bonding versus Dielectric via-last Bonding
Herman Oprins; Vladimir Cherman; Tomas Webers; Soon-Wook Kim; Joeri de Vos; Geert Van der Plas; Eric Beyne

2020 8th Electronic System-Integration Technology Conference (ESTC)

(September 15 – 18, 2020)

3D-Opto-MID for Asymmetric Optical Bus Couplers
Lukas Lorenz; Florian Hanesch; Krzysztof Nieweglowski; Yannic Eiche; Jörg Franke; Gerd-Albert Hoffmann; Ludger Overmeyer; Karlheinz Bock

A Frequency-Domain Thermoreflectance Method for Measuring the Thermal Boundary Conductance of a Metal-Polymer System
Susanne Sandell; Jeremie Maire; Emigdio Chávez-Ángel; Clivia M. Sotomayor Torres; Jianying He

An Organic Process Design Kit, from Characterization to Modelling and Simulation
August Arnal; Lluís Terés; Eloi Ramon

Analysis of Package Design of Optic Modules for Automotive Cameras to Realize Reliable Image Sharpness
Stephan Kühn; Amit Pandey; Andreas Zippelius; Klaus Schneider; Hüseyin Erdogan; Gordon Elger

Carbon Nanotubes Based On-Chip Supercapacitors with Improved Areal Energy Density
Chengjun Yu; Xuyuan Chen

Study on Bottom-up Cu Filling Process for Through Silicon Via (TSV) Metallization
Gilho Hwang; Hsiao Hsiang-Yao; David Ho Soon Wee

Upcoming EPS Sponsored and Cosponsored Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the EPS sponsors and supports a number of global and regional conferences, workshops and other techical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances with colleagues. Many produce publications that are available through IEEE Xplore.

Name:	2021 IEEE International Workshop on Integrated Power Packaging (IWIPP)
Location:	Aalborg East, Denmark
Dates:	Apr 28, 2021–Apr 30, 2021
Name:	2021 44th International Spring Seminar on Electronics Technology (ISSE)
Location:	Bautzen, Germany
Abstract Submission Date:	Jan 20, 2021
Dates:	May 5, 2021–May 9, 2021
Name:	2021 32nd Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)
Location:	DC, WA USA
Dates:	May 10, 2021–May 12, 2021
Name:	2021 20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm)
Location:	San Diego, CA USA
Dates:	Jun 1, 2021–Jun 4, 2021
Name:	2021 IEEE 71st Electronic Components and Technology Conference (ECTC)
Location:	San Diego, CA USA
Dates:	Jun 1, 2021–Jun 4, 2021
Name:	2021 Third International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)
Location:	Osaka, Japan
Dates:	Jun 21, 2021–Jun 23, 2021
Name:	2020 International EOS/ESD Symposium on Design and System (IEDS)
Location:	Chengdu, SICHUAN, China
Dates:	Jun 23, 2021–Jun 25, 2021
Name:	2021 IEEE 30th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
Location:	Austin, TX USA
Dates:	Oct 17, 2021–Oct 20, 2021
Name:	2021 IEEE 67th Holm Conference on Electrical Contacts (HLM)
Location:	San Antonio, TX USA
Dates:	Oct 24, 2021–Oct 27, 2021
Name:	2021 IEEE International 3D Systems Integration Conference (3DIC)
Location:	CA, USA
Dates:	Oct 26, 2021–Oct 29, 2021

Heterogeneous Integration and Chiplet Assembly—all Between 2D and 3D

Peter Ramm[1], Paul Franzon[2], Phil Garrou[2,3], Raja Swaminathan[4], Pascal Vivet[5], Mustafa Badaroglu[6]
[1]Fraunhofer EMFT, [2]NCSU, [3]MCNC, [4]AMD, [5]CEA, [6]Qualcomm

Introduction

"Real 3D" integration - 3DIC Integration in its true definition [1] - has a long history. As early as 1985, Richard P. Feynman expressed this vision [2]: "Another direction of improvement of computing power is to make physical machines **three dimensional** instead of all on a surface of a chip. That can be done in stages instead of all at once - you can have several layers and then add many more layers as time goes on" [2].

Successively, several R&D initiatives started on 3DIC throughout the globe. Towards the end of the 1980´s in a consortium with a.o. Siemens and Fraunhofer Munich, 3D CMOS test devices as e.g. 3D SRAMs were realized based on recrystallization of thin Si [3]. Such "sequential processing" or monolithic concepts are reconsidered today as "ultimate 3D" for stacking at transistor level - in the IRDS More Moore roadmap for the 2030´s [4].

Towards the end of the 1990´s Prof. Mitsumasa Koyanagi´s team at the Tohoku University, for the first time in the world, succeeded in fabricating 3DICs using TSV, explicitly 3D stacked image sensor and 3D stacked memory test chips [5] representing *the* pioneering contributions of today´s two key applications in high volume production (see Fig. 1). At about the same time Fraunhofer in Munich focused already on the key application of heterogeneous systems, consisting of components with different materials/technologies and die sizes. Robust die-to-wafer stacking technologies were developed to achieve what is called today **3D heterogeneous integration** [3, 6]. But despite these early technology demonstrators, it needed decades, until finally Samsung started in 2015 a high volume 3DIC product, the stacked DDR4 and later the HBM2 memory (see Fig. 1, bottom left). The other application that has gone into high volume production is CMOS image sensors (see Fig. 1 top middle). Since 2017, Sony is producing a stacked CMOS image sensor (CIS) for smart phone cameras. On the other hand, there have also been drawbacks. Most significantly, 3D memory on logic applications, widely forecasted by many sources, have been postponed several times.

Realization of 3D chips needs specific design methodology. Essential driving forces for 3D integration are performance (speed), power consumption, costs, and form factor. While TSV technologies using advanced IMC bonding or hybrid bonding processes provide very high vertical interconnect densities, the major issue is the high cost of 3DIC manufacturing. Nevertheless, TSV technology shows up as packaging mainstream for high performance 3DICs. But alternative concepts "between 2D and 3D" were in fact very successful for products with no need of such high interconnect performances, i.e. Si interposer technology (see Fig. 1, top right). And moreover, alternative interposer concepts avoiding costly TSV technology are gaining importance, as e.g. Intel´s omni-directional interconnect (see Fig. 1).

In order to pay more attention to such new stacking concepts, the IEEE Technical Committee 3D decided to broaden its objectives correspondingly and include so-called 2D enhanced architectures (see Fig. 2) and also "chiplet" integration (see further down).

The **Heterogeneous Integration Roadmap** [7] has categorized corresponding architectures between 2D and 3D as follows:

2DO (Organic) multi-chip package (MCP) Architecture: Side by side active Silicon die interconnected at very higher densities on the package using organic materials-based approaches. These can be further sub-categorized into *Chip First 2DO* achieved using a redistribution based approach with fan-out architectures (wafer or panel level: fan-out wafer-level packaging (FOWLP) or fan-out panel-level packaging (FOPLP), (examples: Infineon´s embedded

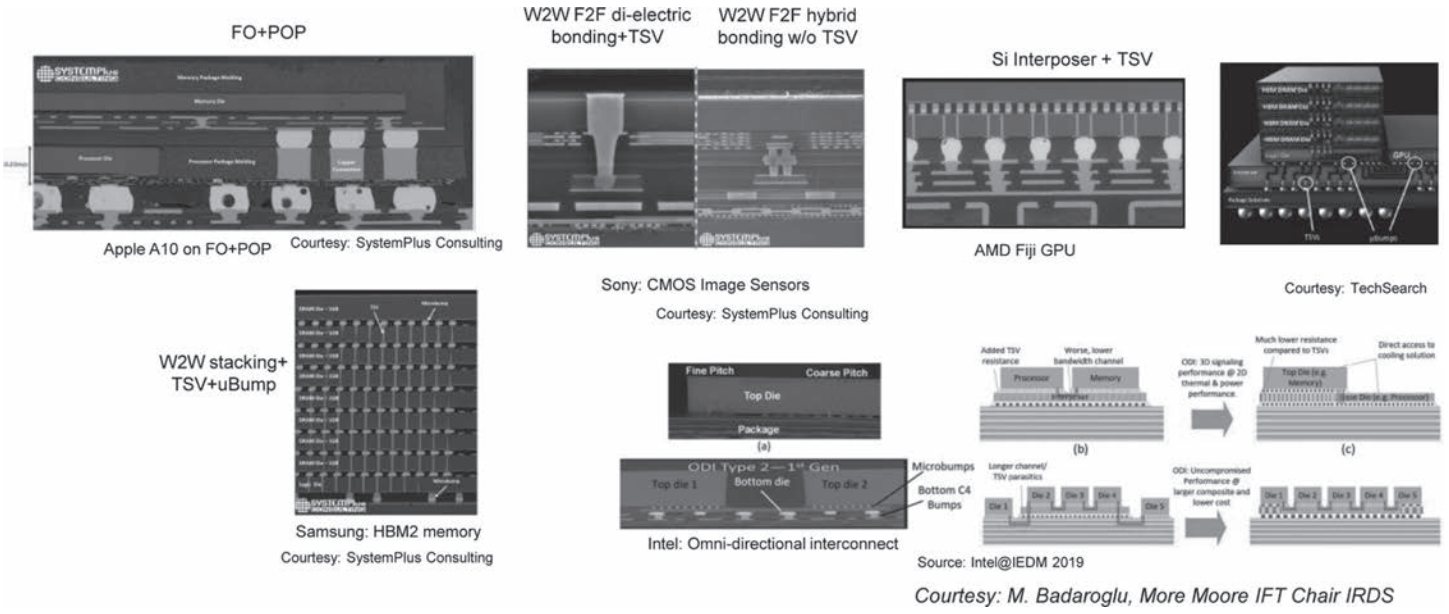

Figure 1: Fine-pitch 3D stacking technologies today ([4]).

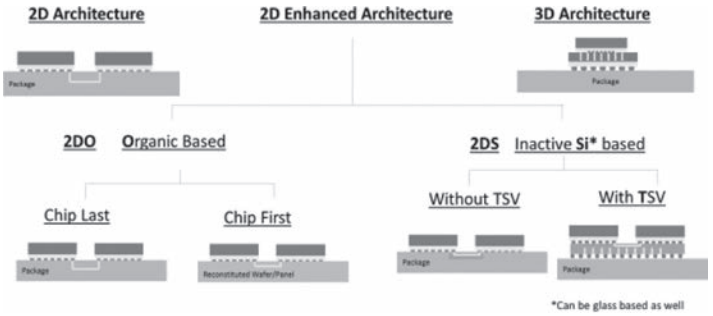

Figure 2: 2D to 3D architectures (source: HIR [7])

Wafer-Level Ball-grid array (eWLB) and ASE`s Fan-out Chip on Substrate (FoCoS)) and *Chip Last 2DO*.

2DS (Inactive Silicon) MCP Architecture: Side by side active Silicon interconnected at extreme higher densities using inactive Silicon integrated into an organic package. These can be further sub-categorized into *Inactive Si with TSV* (example: TSMC´s Chip-on-Wafer-on-Substrate (CoWoS) architecture in Nvidia Tesla) and *Inactive Si without TSV* (Example: Intel Embedded Multi-die Interconnect Bridge (EMIB) based products [8].

Dis-Integration is Underway

We have known for some time that with lateral scaling is slowing down the industry would need to find another way to continue to move forward. One of the options being implemented is to actually "disintegrate" SoCs into their functional parts and then connect these "chiplets" back together on high density interposers.

This was first done by Xilinx on their FPGAs in 2010. Chiplets, as they are now called, are not simply small chips. Chiplets cannot be used by themselves; they're specifically intended to be interconnected together to build complete functionality. Thus, it is better to think of chiplets as a silicon IP (intellectual property) subsystem, designed to integrate with other chiplets through advanced package interconnect (usually micro bumps) and standardized interfaces.

Building complete circuits from pre-verified chiplets is beginning to gain traction as a way of cutting costs and reducing time to market for heterogeneous designs. Chiplets allow us to use the latest node only where needed which in turn results in reduced silicon cost. These silicon savings, in turn, can be allocated for more expensive packaging solutions.

AMD, Intel and TSMC have all introduced or announced chiplet based products and/or technologies. It is also widely accepted that for us to be able to mix and match chiplets produced at different foundries we will need to have standard interfaces and communication protocols. This is presently the most important thing that we can do to stabilize and broaden the chiplet infrastructure. Currently Intel is recommending their AIB (advanced interface bus) interfaces such as AIB and AIB2 while TSMC is offering Lipincon (low voltage in package interconnect) to their advanced customers. It is presently unknown whether these two interfaces can be made compatible.

It is hoped that these functional chiplets will create a library and in the future, we can combine these tested chiplets from multiple foundries, to devise future circuits. DoDs DARPA is in year 4 of their CHIPS program which has been looking at chiplet based solutions for the military.

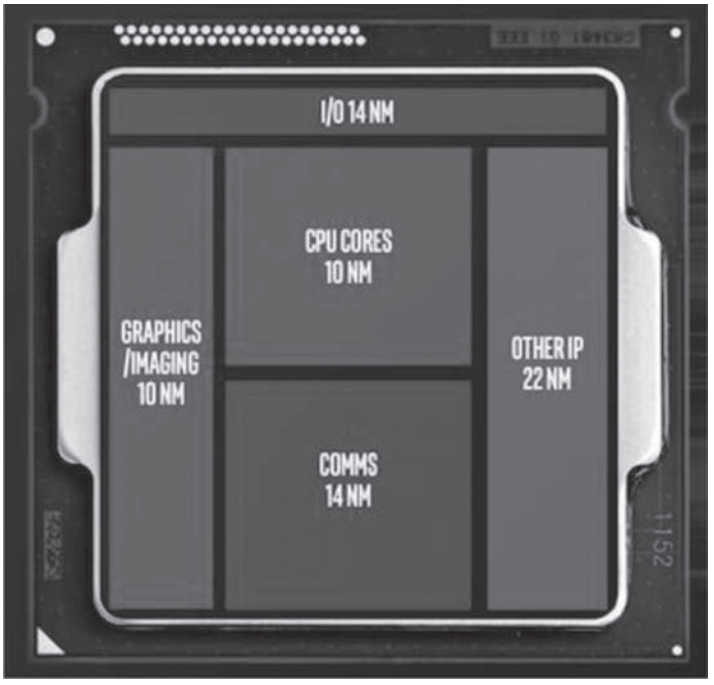

Figure 3: Example of chiplet configuration in a single package

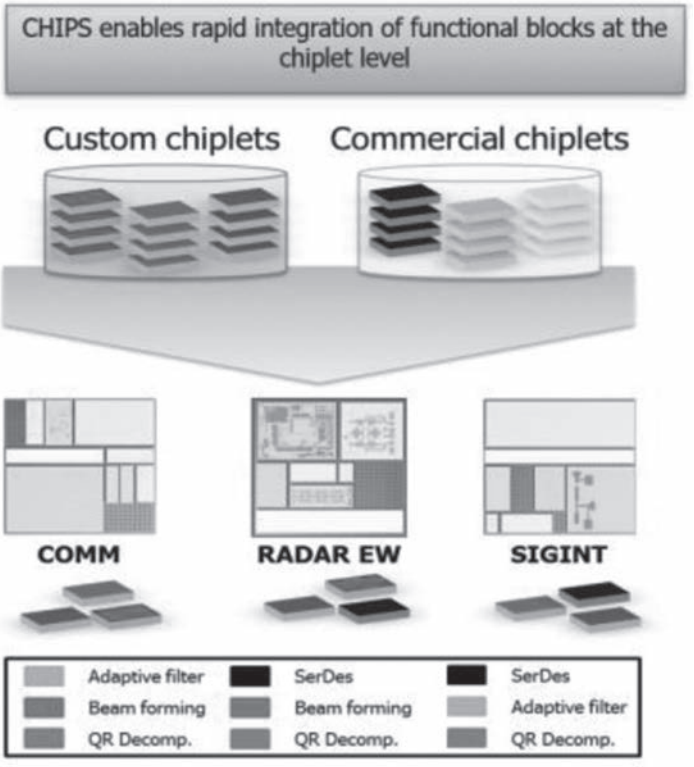

Figure 4: DARPA´s CHIP concept

Chiplet Physical Interfaces

The central idea behind chiplets is to enable new systems to be designed from a set of existing small parts, possibly combined with a small value-add part (or parts) and integrated using advanced interposer technologies. One goal behind chiplet technology is to enable the fast and low-cost design of new systems – systems enabled by unique combinations of chiplets – and thus avoid the high costs of designing a single SOC.

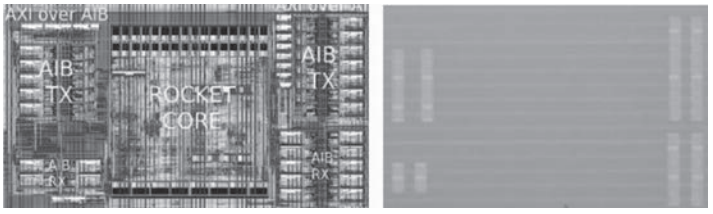

Figure 5: Layout and photo of a RSIC-V chiplet with an AIB interface (source: NSCU)

A key enabling technology is the chiplet to chiplet interface. There are several layers to such an interface including protocol and physical layers. This article will briefly discuss the physical layers. The ideal physical layer interface would achieve the power and area footprint of a long range on-chip SOC driver/receiver pair while enabling a high aggregate bandwidth, being able to drive a wide range of wire lengths (with the attendant range of line losses), and support standardized DFT. Key decisions include voltage swing, serialization, clock management, bus-widths, etc.

In a recent experiment Paul Franzon´s group at NCSU designed a RISC-V chiplet with an AIB interface. The layout and die photo are shown below. The area cost of using a standardized interface is self-evident. However, note this includes area (FIFOs etc.) required to support clock domain crossing.

A number of of chiplet interfaces have been proposed. These proposals and some salient features are summarized in the Table below.

Standard	Source	Bandwidth density/edge	Throughput / lane	Delay	PHY Energy/bit
Advanced Interface Bus (AIB)	Intel [23]	504 Gbps/mm	Up to 2 Gbps	<5 ns	0.85 pJ
Multi-Die I/O (MDIO)	Intel	1600 Gbps/mm	Up to 5.4 Gbps		0.5 pJ
High Bandwidth Memory (HBM3)	JEDEC [26]		4.8 Gbps		0.37 pJ
XSR/USR	Rambus/ OIF		112 Gbps		
Lipincon	TSMC [21]	536 Gbps/mm	2.8 Gbps	<14 ns	0.486 pJ
Bunch of Wires (BoW)	OCP/ODSA [22]	1280 Gbps/mm	Up to 16 Gbps	<5 ns	0.7 pJ
Bandwidth Engine	Mosys [24]		Up to 10.3125 Gbps	<2.4 ns	
Infinity Fabric	AMD [25]		10.6 Gbps	< 9 ns	2 pJ

Chiplet Integration onto Active Interposers

Circuit and system designers need a more affordable, scalable and efficient way of integrating heterogeneous functions, to allow more reuse, at circuit level, while focusing on the right innovations in a sustainable manner. Due to the slowdown of advanced CMOS technologies (7nm and below), with yield issues, design and mask costs, the innovation and differentiation through a single die solution is not viable anymore. Mixing heterogeneous technologies using 2.5D/3D is a clear alternative.

Chiplet partitioning is raising new interests in the research community [9], in large research programs as DARPA CHIPS [19] and in the industry. It is actually an idea with a long history in the 3D technology field [1]. Motivation for chiplet-based partitioning is driven by cost, modularity and heterogeneity. By dividing a single circuit in various chiplets and sub-modules, a large system is achieved with acceptable yield and cost using Know-Good-Die (KGD) sorting [10]. "Chipletization" allows building modular systems from elementary blocks and circuits, more focusing on function than on technology constraints. Finally, proper technology is selected for the right function (advanced CMOS for computing, mature technology for analog and IOs, etc), while 3D integration is used for the overall system assembly.

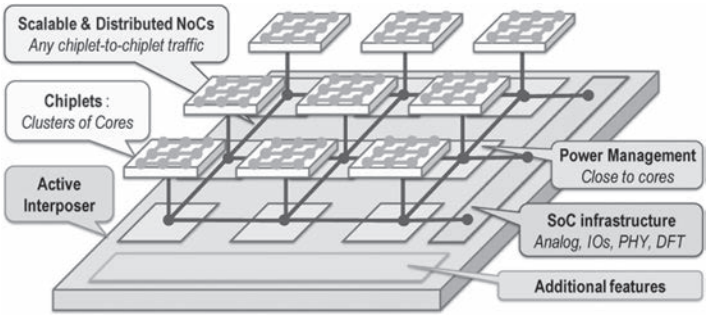

Figure 6: Active Interposer concept and main features

Several technologies have been assessed for chiplets assembly: organic substrates as a low-cost solution adopted by AMD [11], passive interposers as a high-performance solution adopted by TSMC [12] or silicon bridges as an intermediate solution adopted by Intel [13]. These technologies are mature, economical benefits and performances are achieved, but they still raise limitations. Due to wire-only interconnects, inter-chiplet communication are still limited to side-by-side communication reducing the number of connected chiplets; the passive interposers cannot carry less scalable functions such as analog and IOs; co-integration of chiplets with incompatible interfaces is impossible.

Homogeneous Chiplets

To tackle these issues, the concept of active interposer is introduced that enables integration of some active CMOS circuitry on a large-scale interposer (Fig. 6). The active interposer can be seen as a generic bottom die infrastructure which integrates i) flexible and distributed system interconnect topologies between chiplets for scalable communication traffic, ii) energy efficient 3D-plugs for dense inter-layer communication, iii) fully integrated voltage regulators for efficient power supply close to the cores and iv) memory-IO controller and PHY for socket communication. Finally, the active interposer integrates system infrastructure: clock, low speed interfaces, thermal sensors and 3D design-for-test (DFT) to enable KGD strategy.

As an active interposer large prototype [14], the IntAct circuit demonstrator from CEA (Fig. 7) is composed of 6 chiplets (28nm FDSOI) each integrating 4 clusters of 4 cores (16 cores per chiplet), 3D stacked with 20 µm pitch µbumps on an active interposer (65nm CMOS) with 40µm pitch TSV middle (Fig. 8) [15]. In terms of technology partitioning, there are two technology node differences, ensuring enough performances in the bottom layer, while preserving system costs. The active interposer integrates numerous distributed interconnects for long distance low latency communication, 3D-plug interfaces achieving 3 Tbit/s/mm^2 bandwidth density, and fully integrated switched capacitor voltage regulators with up to 82% power efficiency. The circuit implements a total of 96 cores with a scalable cache coherent architecture, delivering a peak 220 GOPS. As a result, users will get more GOPS at the same power budget – or a reduced energy footprint for the same task – and will benefit from an increased

memory-computing ratio along the memory hierarchy. These are main drivers to address big data applications.

Heterogeneous Chiplets

For active interposer, chiplets can be either identical, with similar functions as presented in this first example, or with distinct functions. In another example, the ExaNode CEA prototype integrates 2 bare FPGA dies, 2 chiplets onto an active interposer, all integrated onto a large substrate MCM module, as presented Fig. 9 [16]. This circuit targets ultra-wide range of workloads for next generation scalable and high-performance compute nodes.

For 3D integration, the technologies are still evolving to provide more advanced chiplet integration, with reduced pitches, for improved energy efficiency, die-to-die parallelism, and thermo-mechanical behavior. Hybrid bonding technology initially devoted to Wafer-to-Wafer (for BSI Imagers) are also appearing for Chip-to-Wafer assembly, with reduced pitches (down to 10µm and targeting below) [17].

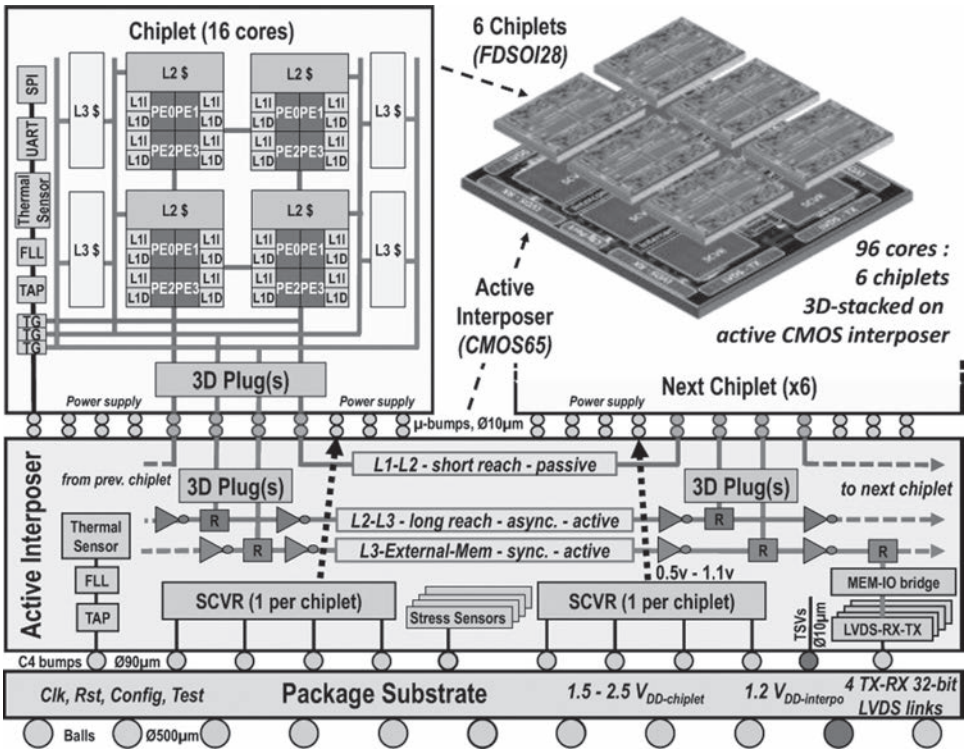

Figure 7: IntAct circuit architecture [14]

The IntAct and ExaNode circuit demonstrators are a first step towards larger scale and heterogeneous chiplet-based systems, showing the benefits of 3D connectivity and the smart features of active interposers.

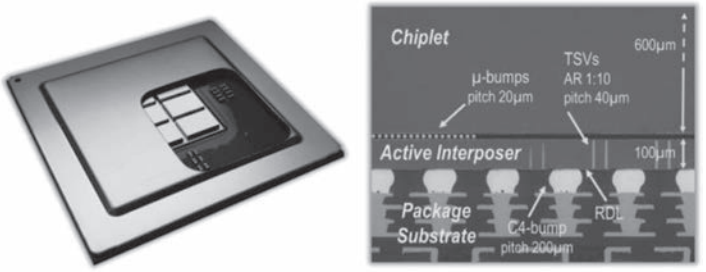

Figure 8: IntAct package and 3D cross-section [15]

Interfacing Chiplets, Die-to-Die Standards, and Testability

As presented in previous circuit demonstrators, the so-called 3D-plug IP solution, integrating both the logical and physical aspects are used for energy efficient parallel die-to-die interfaces. For true chiplet compatibility, it is currently complex to integrate chiplets from different sources, due to missing standards. Strong standardization initiatives are on-going from ODSA group [18] and CHIPS program [19]. As of today, with passive interposers, wire-only connectivity prevents the integration of chiplets using incompatible protocols. On the contrary, active interposer is a solution enabling to bridge incompatible chiplets by ad-hoc logic. This solution has been proposed by zGLUE Inc. for instance as a generic connectivity solution for medium performance devices.

Lastly, testability is also a strong concern for chiplet based design, where testability and Know-Good-Die strategy must be available to yield the overall 2.5D or 3D system. Strong progresses have been achieved recently, since the on-going standardization effort of the IEEE1838 Working Group has led to the approval of the IEEE1838 3D test standard in March 2020 [20].

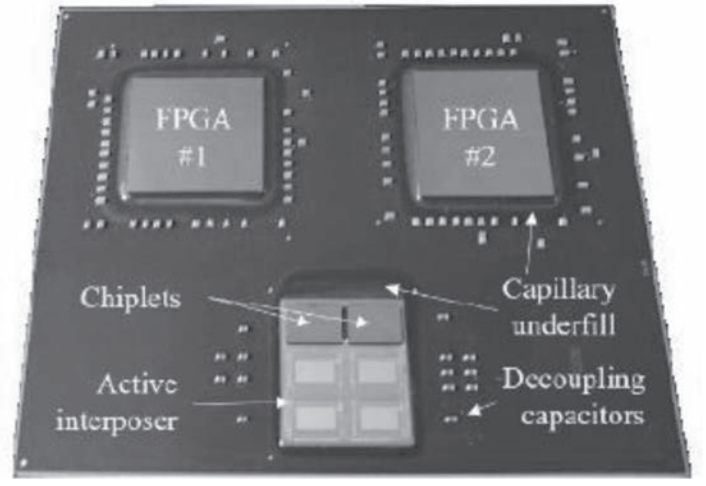

Figure 9: ExaNode heterogeneous Multi-Chip-Module [16]

Architectures between 2D and 3D – best-tailored for the different specific applications of heterogeneous integration

The different applications, as e.g. memory, CMOS image sensor, GPU, RFIC and chiplet based products need best-tailored technology solutions for their specific performance, power consumption, costs, and form factor requirements. Besides 3DIC integration in its strong definition, a variety of architectures between 2D and 3D are potentially well-suitable for cost-effective production. This is especially true for the growing market of heterogeneous 3D sensor/IC systems with the need for robust die-to-wafer stacking of

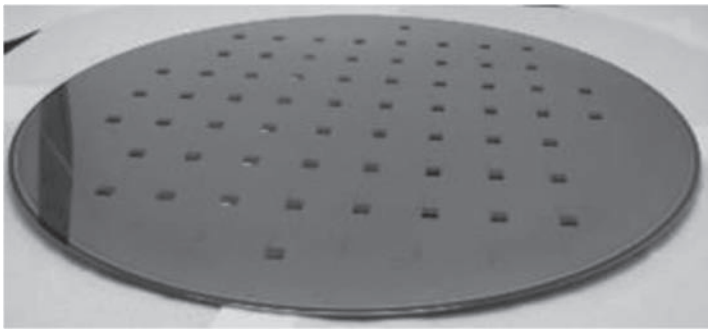

Figure 10: Chip-to-Wafer Hybrid Bonding integration

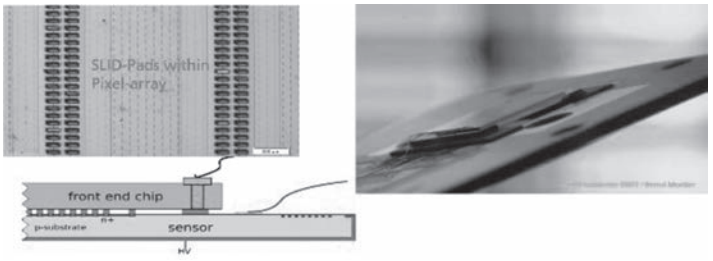

Figure 11: Heterogeneous integration of sensor and readout circuit (Fraunhofer EMFT in co-operation with Max-Planck MPP)

components of *significant* different device technologies, as CMOS, sensors, actuators and MEMS [27, 28] rather than extremely small TSV/pad pitches.

A corresponding example of **heterogeneous 3D sensor integration** is shown in Fig. 11. The photon detector and appropriate read-out IC are 3D integrated by intermetallic compound (IMC) bonding with mechanically stable Cu/Sn Solid-Liquid-InterDiffusion (SLID) interconnects [28].

In order to pay more attention to the described fine-pitch stacking concepts and new architectures "between 2D and 3D", the **IEEE EPS Technical Committee 3D** decided to broaden its objectives from 3DIC and monolithic integration on one side, to non-TSV 3D technologies, chiplet assembly, Si interposer and alternative interposer concepts (including TSV less), on the other side of the fine-pitch interconnect "spectrum". In the last decade we have seen a true success story of 3D and enhanced 2D technologies. Nevertheless, there is still a huge amount of related problems, as e.g. thermal issues, design and test issues, materials optimization, robustness of the processes, thermal-mechanical reliability of the systems and last not least high production costs, which can only be solved by significant development efforts [7, 29].

Visit our website for information on TC 3D/TSV:

https://eps.ieee.org/technology/technical-committees/technical-committee-3d-tsv.html

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Reliability Challenges for Enhanced 2D and 3D Heterogeneous Integration Technologies

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[3]Intel Corp., [4]Inphi Corp.

Introduction

As an active interposer large prototype [1], the IntAct circuit demonstrator from CEA (Fig. 1) is composed of 6 chiplets (28nm FDSOI) each integrating 4 clusters of 4 cores (16 cores per chiplet), 3D stacked with 20 mm pitch µbumps on an active interposer. Fig. 2 is the cross-section of the InFO technology TSMC introduced in 2016.

Combining thinned stacked chips, interposer, package substrate, underfill material, micro-bumps, TSVs, RDL and C4 bumps, as shown in these examples, brings new reliability challenges. In general, well known electrical failure mechanisms such as electromigration and dielectric breakdown remain important but can now also occur in new building blocks such as micro-bumps, TSVs and RDL. But in addition, the risk of thermo-mechanical related failure mechanisms, such as delamination and cracking, clearly increases, especially when the technology uses chips with, mechanically fragile, ultra-low-k (ULK) BEOL layers.

In this paper, we will review the major reliability failure modes and failure mechanisms associated with the 3D and FanOut packaging technologies.

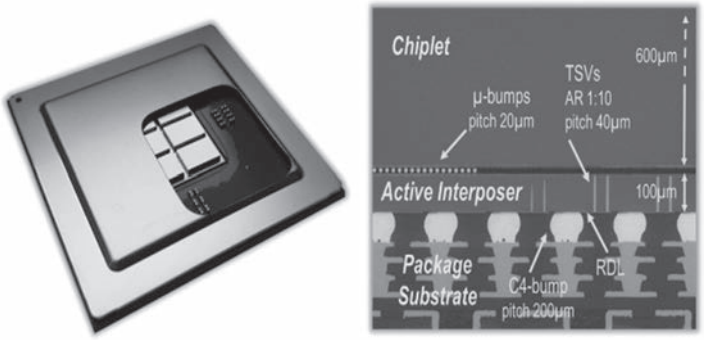
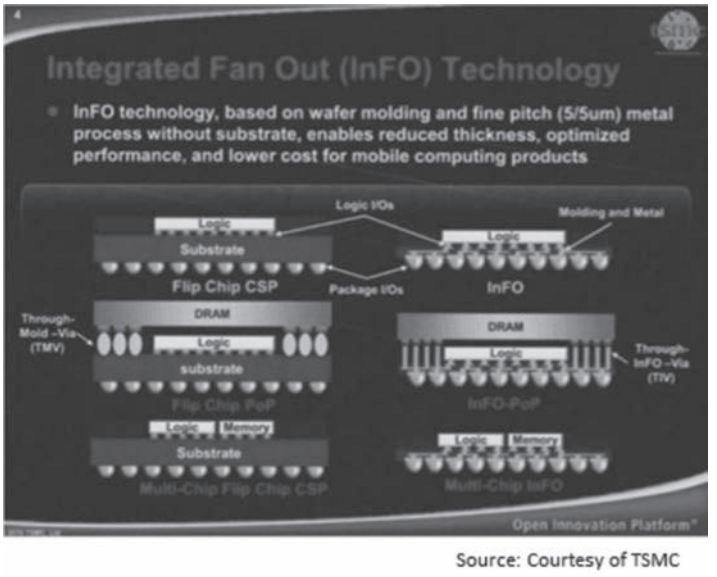


Figure 1: IntAct package and 3D cross-section [2].



Source: Courtesy of TSMC

Figure 2: TSMC Integrated Fan Out (InFO) Technology [3].

Impact of Mechanical Stress on Active Devices

Stresses generated by 2D- and 3D technology can result in delamination and fracture, as discussed later in the paper. But stress also affects mobility and bandgap, and thus the electrical characteristics of active devices. In general, one can distinguish between global stress and local stress. Global stress acts on the full chip and is mostly a result of CTE mismatch between stacked chips and interposer and package materials. It is affected by thinning, bonding, backside processing etc. Fig. 3 demonstrates the impact of different packaging options on the I_{ON} current of FETS, which were in this case used as stress sensors [4]. The packaging process resulted in a global decrease of I_{ON}.

TSVs, micro-bumps and Cu pillars can also introduce local stress. The impact of TSV-generated in-plane stress on planar and finfets was studied in detail in many publications [11], leading to the introduction of the well-known keep-out-zone (KOZ) for active devices. In general, this Impact decreases with decreasing gate length and also the TSV induced stress decreases for TSVs with smaller diameter. But also out-plane stress can affect devices that are located close to the stress source. For example, the combination of underfill shrinkage and a micro-bump, locally induces high out-of-plane stresses in the Si. This is clearly visible in Fig. 3, bottom, where the FET stress sensors are located under a micro-bump. Not only FETs, but also III-V devices such as for example HBTs, the transistor performance were shown to be very stress sensitive [5].

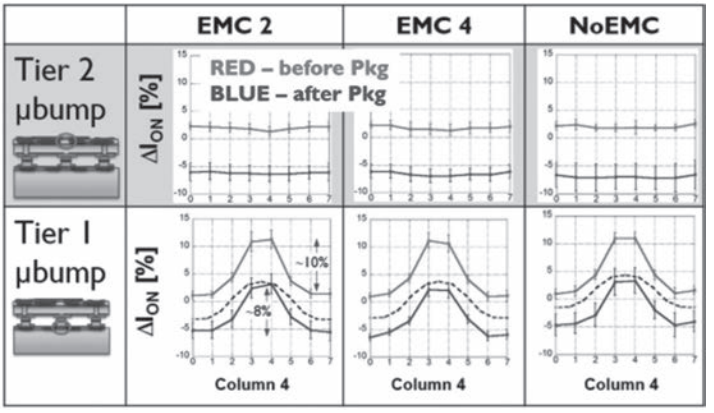


Figure 3: Impact of local stress induced by packaging and micro-bump presence on the Ion current in FETs. [5].

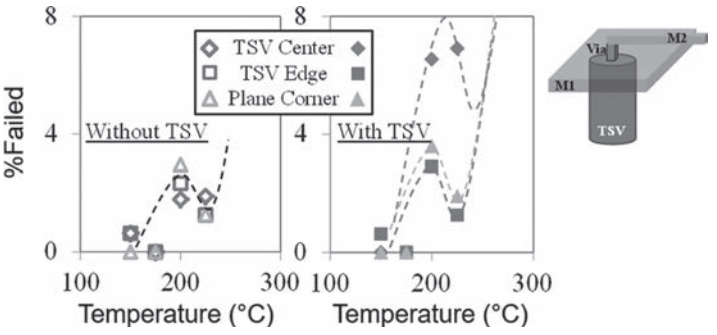


Figure 4: Impact of TSV-presence on stress migration in the BEOL.

TSV

Besides the thermo-mechanical stresses induced by a TSV and its impact on device performance described above, the introduction of TSVs leads to different reliability concerns. First, there is bulge-out of Cu at the top of the TSV due to the thermal budget required for BEOL processing, a phenomenon generally referred to as Cu pumping. To drive out this bulge-out, a high thermal anneal is required prior to Cu CMP [6]. A continuous concern is the high statistical variation in Cu pumping due to micro-structural variations [7]. Once optimized the impact of the phenomenon on BEOL reliability, where all aspects have been studied by various authors [8-10]. As an example, figure 4 shows the impact of TSV-presence on stress migration in the BEOL close to the TSV. Due to higher stress gradients, a higher amount of failures is seen under a via that is placed on top of a TSV. As via-redundancy is a well-know fix to the problem of stress migration, this issue can be solved by design.

Another issue with TSVs is liner integrity. Although TSV-liners are much ticker than oxides used in FEOL and low-k dielectrics used in BEOL, the high aspect ratio of TSVs and the low temperatures of dielectric deposition required for certain applications challenges the reliability of this liner. The main issue with the liner integrity is not the intrinsic breakdown of the liner, but the potential drift of Cu due to a weak barrier coverage. Decoupling the two mechanisms by applying different voltage polarities during reliability testing is crucial [11].

Micro-Solder Balls

Depending on the UBM/solder materials used, intermetallic compounds (IMCs) are formed at the interface between UBM and solder. The IMC layer grows over time (accelerated by temperature) which results in a change of resistance of the bump, as shown in Figure 5 for a Cu-UBM/Ni/Sn system where two IMCs are formed [12]. The resistance change and temperature impact highly depend on the materials used. IMC growth can result in complete consumption of the UBM, causing an open failure. Depening on the material choice, Kirkendall voids can form at the interface between UBM and IMC, weakening the mechanical robustness of the bump and increasing the risk of fracture upon impact. High density micro bumps will increase the rsik of solder bridging during bonding.

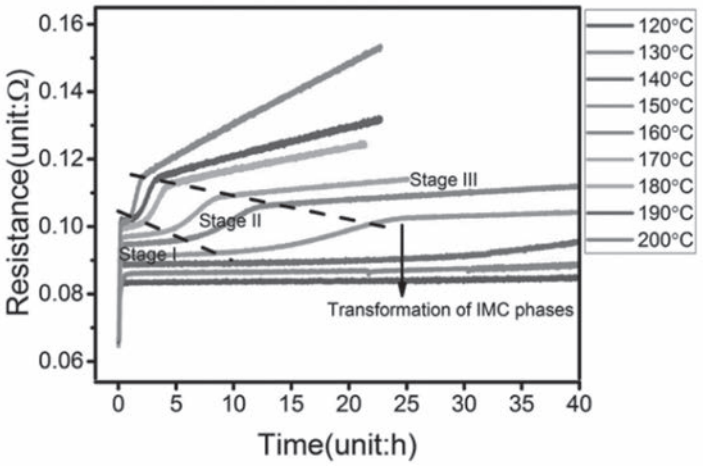


Figure 5: In-situ measured IMC induced resistance change of Cu/Ni/Sn test samples [12].

Table 1. TSV and Micro-Balls Induced Failure Modes.

AREA	DESCRIPTION	EXPECTED RELIABILITY FAILURE MODE	FAILURE STIMULI for the FAILURE MECHANISM (description of the driving factor to the failure
FEOL	Change of electrical characteristics of all devices	Devices/system out of specs	Global mechanical stress -induced in silicon by 3D processing. This stress is mainly caused by CTE mismatch
FEOL	Change of local device electrical characteristics	Device/system out of specs	Local mechanical stress induced in silicon near 3D processing components (TSVs, micro-solder bumps, Cu pads and pillars).
Interconnect	Micro bump IMC growth	Increase in interconnect resistance over time	IMC growth over time (enhanced by temperature)
Interconnect	Micro bump delamination	Electrical open	IMC growth over time (enhanced by temperature) resulting in UBM consumption.
Interconnect	Micro bump crack in Cu-UBM/Sn based solders	Electrical open	Micro bumps fracture during mechanical impact due to a weak interface caused by Kirkendall void formation.
Stacking	Increased chip temperature.	Temperature accelerated failures	Increased thermal resistance due to a thick BEOL stack or due to many stacked chips with a thinner BEOL stack but many bonding interfaces
Interconnect	Solder bridging	Electrical short, or XCT or CSAM detection	Ultra-fine micro bump pitch and high density increases the risk of solder bridging during bonding.
Interconnect	Cu pumping	Damaged BEOL	Cu bulge-out due to thermo-mechanical stresses induced by TSV-anneal during BEOL processing
Interconnect	Liner integrity	High leakage/ copper diffusion	Weak barrier coverage in TSV liners can cause Cu to become mobile in liners and adjacent Si

Thermal Resistance

3D technology highly affects the thermal management of the chips. In face-to-face bonding, there will be an increased thermal resistance due to a thick BEOL stack, which thermal properties will determine the overall behaviour. On the other hand, when stacking many chips with a thinner BEOL (ex. HBT), the many bonding interfaces will determine the thermal resistance of the integration. [13].

Alan's Paragraph

AREA	DESCRIPTION	EXPECTED RELIABILITY FAILURE MODE	FAILURE STIMULI for the FAILURE MECHANISM (description of the driving factor to the failure
EMIB	Microbump crack	Electrical open during Temp. cycle	Microbumps fail due to difference in package and die and underfill CTE and residual process stressing
EMIB	Microbump crack	Electrical open during bake or preconditioning or early thermal cycling	Bump solder consumption resulting in brittle intermetallic that cracks with high normal and shear loading. – see Xylinx paper Ramalingham
EMIB	Underfill cracking at die corner and edges	Open circuit or delamination	High shear force at the corners and edges of the companion dice (distance to neutral point effect) resulting from package displacement relative to the dice during preconditioning and thermal cycling.
EMIG SUM			EMIB packages trend to have large die to package ratios that results in high shear loading during thermal cycling events. Microbumps in tension by crack due to high brittle intermetallic content or bump consumption depending upon design, geometry and processing.

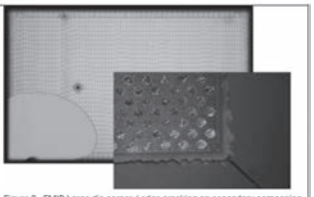
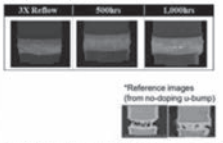


Figure 2. EMIB Large die corner / edge cracking on secondary companion die. CSAM shows the extent of damage and shear from the corner while the inset figure shows underfill cracking at the die corner and edges. A.E.Lucero, Chip Package Interaction-CPI tutorial, IEEE Int'l Reliability Physics Symposium, Orange CA, 2015

MICROBUMP CONSUMPTION CRACK

Microbump on COWAS showing copper consumption and IMC formation after SMT and baking in the doped bump and undoped bump cases.



Suresh Ramalingam; 3D-IC Advances in the Industry, IEEE Elect. Components Tech. Conf.; Orlando FL 2014

ELK	ELK Cracking under bump	Electrical open or CSAM crack signature	Mechanical loading in tension and mixed modes that results from package and underfill contraction and expansion in thermal cycling
ELK	ELK Delamination at the die corners and edges	Electrical open, short or CSAM crack signature	Mechanical loading in concentrated near edges and corners from shear and mixed modes that result from package and underfill contraction and expansion in thermal cycling
ELK SUMM			Low-k dielectric is intrinsically weaker in strength in the temperatures used in thermal cycling which results in risk when the die is flip-chip assembled to a package. The package, composite layered stack tends to change shape during thermal events due to CTE differences and when coupled to a stiff, non-compliant die the differential displacements result in high normal and mixed mode loading of the low-k die layers.

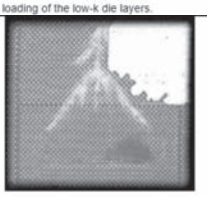


Figure 5. Large area underfill related die delamination on a large die silicon and package observed during development after 28 cycles of TC 'B' testing, c. 2000

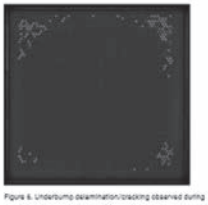
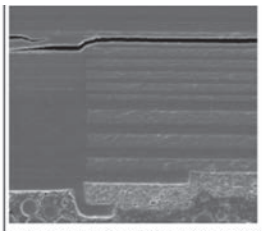
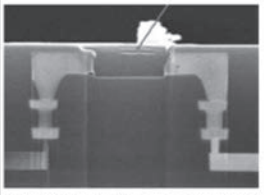


Figure 6. Underbump delamination/cracking observed during development, observed after 200 cyc. of TC 'B' testing, c. 2001

A.E. Lucero, G.Xu, D.Hultink, Low-k - Package Integration Challenges and Options for Reliability Qualification, IEEE-Int'l Reliability Physics Symposium, Monterey, CA, 2012.

			 K.Chanda, V.Mahadev; A Fabless Company's Perspective on Large Die Chip Package Interaction (CPI) Challenges, IEEE, Int'l Physics Symposium, Orange, CA.; 2015  Lei Mercado, Analysis of flip chip packaging challenges on Cu/low K interconnects, IEEE trans. Device and materials reliability, V3, N4, 2003 OTHERS: Pei-Haw Tsao, Bill Kiang, Kenneth Wu, Abel Chang and Tsorng-Dih Yuan; Low-K Flip Chip Board Level Reliability on 65nm Technology; IEEE Elect. Components Tech. Conf.; Las Vegas, NV 2007
RDL	Re-distribution layer cracking	Electrical open after preconditioning or thermal cycling	Mechanical loading from normal, tension and mixed modes resulting loading near bumps and RDL edges that cracks during package expansion and contraction.
RDL SUMM			The redistribution layer is often thicker and of a different metal composition that the underlying die layers which results in an internal residual stress. The stress may be amplified when assembled into a package where additional CTE differences result in high differential displacement related stress at all parts of the RDL.

Fan Out Package Failure Modes

Major failure modes for the Fanout packages are summarized in table x. Figure x shows a typical RDL failure near the die edge. [x]

Table x. Major Failure Modes for Fan Out Packages.

AREA	DESCRIPTION	EXPECTED RELIABILITY FAILURE MODE	FAILURE STIMULI for the FAILURE MECHANISM (description of the driving factor to the failure
RDL	RDL Cracking	Electrical open during Temp. cycling and drop tests on board	Large die induced high local stress due to CTE mismatch between die, RDL and board
RDL	RDL Delamination and Lifted	Electrical open during drop test on board	Localized high stress and poor adhesion between RDL and dielectric polymer
RDL	RDL and microvia Electromigration	Electrical open during high temperature and current	Localized current crowding and scaling of RDL and microvia size
RDL	RDL Crrosion	Electrical short during biased HAST test	Reduced RDL spacing and UF stress breaking UBM sealing
Under Bump ILD	ILD Damage under Cu pillars	Electrical open during flip chip and during Temp cycling test	RDL first process incuded planarization issue Bonding force during TCNCP process
Micro-bump	Cracking	Electrical open during temp cycling	Global/local CTE mismatch induced stress in micro-bumps
Micro-bump	Voiding	Electrical open during elcromigration test	Temperature and high current density particarly the current crowding at RDL/Bump intersection
Overall Package	Warpage	Chip first RDL Lithograph Board level SMT Issue	Large size panel Material properties Process flow and parameters Die size and thickness

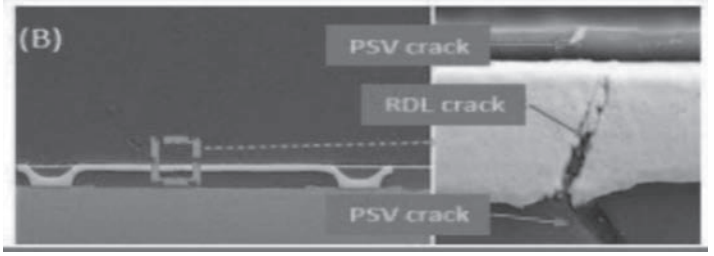


Figure x: Typical RDL Failure Mode for Fan Out Package.

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Additive Assembly Technologies for Advanced Semiconductor Packaging

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***Abstract*—As the benefits of conventional transistor scaling declines, innovative semiconductor packaging architectures, over and above the flip-chip style, need to be developed to increase the bandwidth and reduce the latency of data transfer while delivering reliable products. These novel architectures, including but not limited to, Si-interposers, high-density laminates, bridges, 3D packages, embedded and fan-out packages require advanced Bond & Assembly technologies that are additive in nature to enable Heterogeneous Integration (HI). By leveraging the strength of silicon on the device side, these packages can be deployed in electronic applications, including AI hardware, such as, sensing & IoT, automotive & power, MEMS, NEMS, flexible, stretchable and wearable electronics. The focus of this article from the IEEE EPS Technical Committee on Emerging Technologies is to summarize state-of-the-art additive Bond and Assembly (BA) techniques from the literature, such as, additive manufacturing and 3D printing, along with their specific material requirements and the thermal/mechanical/reliability challenges and limitations.**

***Index Terms*—3D packaging, additive manufacturing, flexible electronics, heterogeneous integration, integrated heat sinks, thermo-mechanical reliability.**

I. Introduction

With The Advancements In Emerging Applications For Iot, Mems, Rf, Flexible Electronics, High-Performance Computing (Hpc), Artificial Intelligence (Ai) Computing, And 5G Applications, There Is An Increasing Need For Improving The Bandwidth And Reducing The Latency Of Data Transfer In Electronic Devices [1]–[5]. Electronic Packaging Plays An Important Role Here As It Allows For Heterogeneous Integration Of Novel Architectures, Above And Beyond Flip-Chip Style, Including But Not Limited To, Si-Interposers, High-Density Laminates, Bridges, 3D Packages, Embedded, And Fan-Out Structures [6], [7]. For Such Innovative Packaging Architectures To Be Mechanically, Thermally, And Electrically Reliable, Significant Improvements In Our Traditional Bond & Assembly (Ba) Processes Are Required.

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Additive manufacturing (AM)-based BA processes refers to a class of technologies that can print dielectric material and conductive material selectively within a volume, with these volumes being uniquely defined for each print. These processes are evolving as a promising candidate for next-gen electronic packaging architectures due to its multiple advantages [8]–[13]. Firstly, they serves as an energy and resource efficient alternative of the conventional BA processes. Secondly, it can combine multiple materials in a single build that can produce volumetric designs that are especially interesting for 3D electronic packages, enabling the creation of intricate and conformal electronics that are structurally united into a manufactured part with integrated cooling. This attribute minimizes cable interconnects and redundant electronics packaging, resulting of a reduction of mass and assembly complexity in the final electronic component [14]–[18]. Finally, with AM—complexity is free—this opens doors for unconventional shapes and structures that reduce prototyping and development cycle times, while reducing material waste [19]–[21]. Reduced costs and time to part could come from replacing traditional multi-stack PCB manufacturing, which currently can take one the order of multiple weeks for manufacturing and shipping which significantly impedes time-to-part and ease of design iteration. Many of the AM technologies could be applied towards advancing the System-in-Package (SiP) technology by creating complex geometries with encapsulation packaging. Regarding the elimination of currently necessary manufacturing steps, an optimized AM-based BA technology could allow for the concurrent fabrication of a multi-stack PCB, embedded components, printed or placed passives, placed dies, printed interconnects, printed encapsulation, high aspect ratio vias, printed antennas, and other necessary heterogeneous integration-based SiP components as shown in **Figure 1**.

II. AM-based BA Processes for Electronic Packages

A. Inkjet-Printed 3D Interconnects for Millimeter-Wave System-On-Package Solutions

One of the well-suited application areas for AM-based electronics packaging is electromagnetics due to the cost, form factor and electrical performance involved in these technologies. High frequency millimeter-wave (mm-wave) wireless technologies are essential for efficient bandwidth data transmission in next-gen communication systems [22]–[24]. For such applications, system-on-package (SoP) packaging is popular, where an integrated circuit (IC) die can be directly bonded to peripheral components, such as other ICs, antennas, and various other passive components [25], [26]. For such bonding, 3D first-level interconnects are required, that are historically realized using wire-bonding and flip-chip techniques [27]. Despite being inexpensive, they suffer from poor mechanical reliability, high parasitic inductance, and coefficient of thermal expansion (CTE) mismatch [28], [29]. Due to these challenges, the development of 3D interconnects using additive manufacturing has been studied in literature.

One such approach is to use piezoelectric inkjet printing, a rapid, fully additive electronic fabrication technology with the benefits of zero waste, reduced cost, and increased design flexibility. As a first-of-its-kind proof of concept, coplanar waveguide (CPW) transmission lines with a fan-out structure are fabricated and measured to interconnect a silicon die with a packaging substrate using conductive silver nanoparticle and dielectric polymer

inks as shown in **Figure 2** [30]. The packaging substrate chosen here is a 1 mm thick glass slide in order to facilitate handling throughout the fabrication process, however this technology could be applied to other packaging substrates, such as metallic, flexible organic, and ceramic.

The insertion and return loss from these low-cost, robust CPW transmission lines are measured and found to be appropriate for their applications in conventional mm-wave systems.

B. Packaging for Power Semiconductors Based on the 3D Printing Technology Selective Laser Melting (SLM)

Printing onto silicon and other substrates is desirable to make both electrical connections and cooling structures. In contrast to inkjet sprays, Selective Laser Melting (SLM) can build-up thick, and high-aspect ratio metallic films [31]. These processes use a focused high-power laser directed with a galvo to melt metal powder into a solid piece [32].

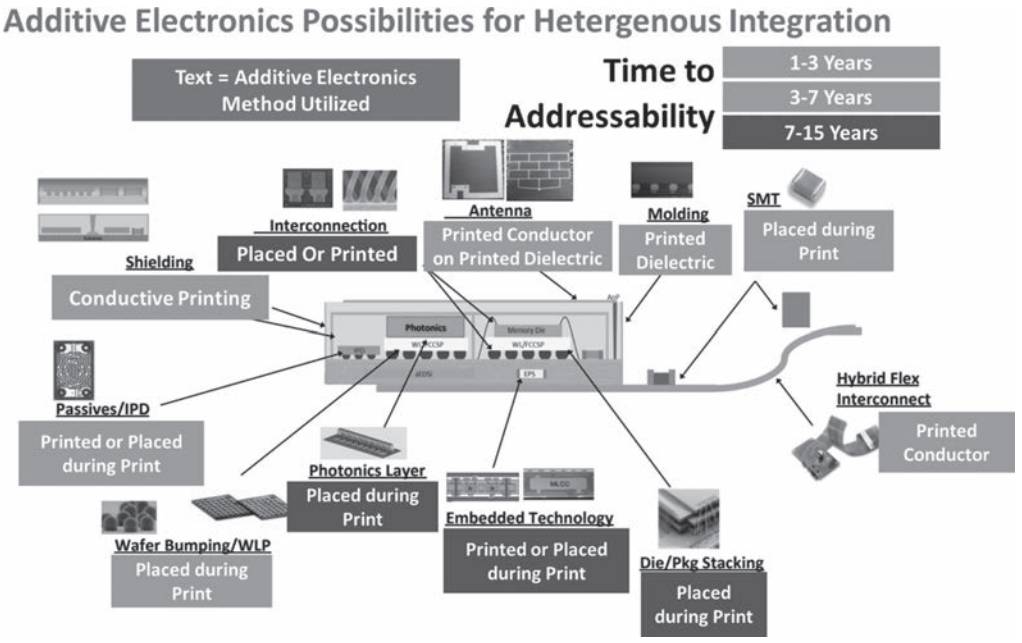

Figure 1. Possible uses for additive electronics (AE) within SiP applications for heterogeneous integration with estimated time horizons for development.

Classic BA processes for power electronics include assembly of a chip soldered / sintered onto a direct-copper bonded substrate where the topside of the chip is contacted via bond wires. Here, the solder layer and the bond wire contacts are the two most sensitive elements. A new packaging technique based on AM-based SLM method using aluminum powder is proposed in literature that tries to replace solder or sinter layers, respectively bond wires – and hence reduce the thermo-mechanical stress. Conrad *et al* have developed a process to print the electrical bonds on the top of these power devices [33]–[35]. Their process requires sputtering an extra thick layer of aluminum (at least 15 μm), beyond what is typical, to bond. They also proposed a structured geometry to strengthen the robustness of the printed slender structures (**Figure 3a**).

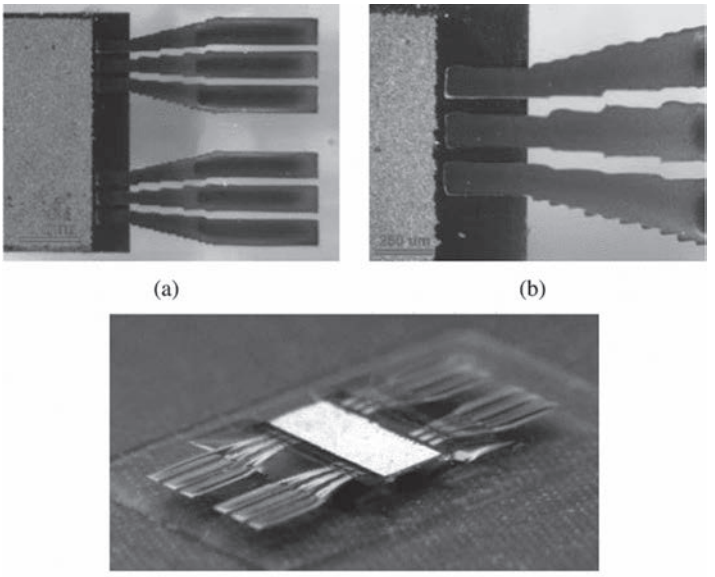

Figure 2. (a-b) Micrographs and (c) perspective image of the inkjet-printed CPW interconnect samples [30].

To overcome the need for a thick metallization and allow direct printing onto silicon, Azizi et al have developed a process that uses an SLM printed interlayer alloy to bond to the silicon [36]–[39]. In this technique, a Sn3Ag4Ti interlayer alloy is first deposited onto the semiconductor substrate by selective laser melting in a specific pattern (**Figure 3b**). During this process, the titanium elements will chemically bond to the semiconductor substrate in a short timescale (sub-100 μs). The low melting point of the alloy minimizes the thermal stresses during the high heating and cooling rates of selective laser melting. This process was able to print 400 μm diameter fins of 8 mm height (1:20 aspect ratio) on top a flip-chip package (**Figure 3b**). This same printing process has also been demonstrated with graphite, which also has desirable thermal properties [40].

The prior SLM print processes used powder with diameters of around 20-40 μm, which sets the minimum feature size to be of that order. More recently for Roy et al demonstrated that metals can be printed via selective laser sintering of 1-5 μm [41], [42]. The process deposits a thin layers of nanoparticle inks of about

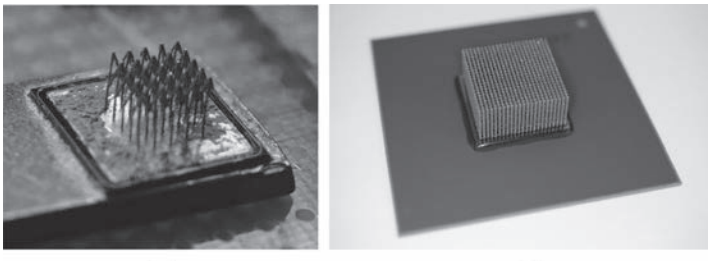

Figure 3. (a) Conrad *et al*'s first realized prototype showing electrical functionality [33]. (b) Azizi *et al*'s demonstration of printing aluminum directly onto silicon without a sputtered metallization using a printed SnAgTi interlayer.

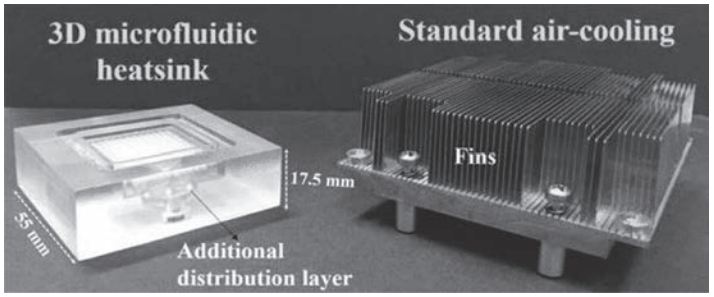

Figure 4. Benchmarking study: size comparison of the standard air-cooling solution and the package-size impingement cooling solution [53].

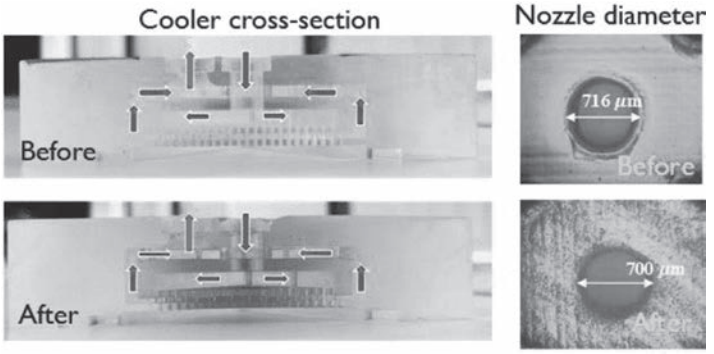

Figure 5. Cross section analysis after long term measurement with DI water for the 3D printed plastic cooler [53].

1.5 μm wet film thickness which dries to a 500 nm dry film. This dried film is then laser sintered with a beam expanded laser that has its exposure image selectively controlled with a digital micromirror array. A continuous wave or nanosecond laser can be used. The substrate in these experiments were aluminum and glass and they demonstrated the ability to build structures as tall as 7 μm with thickness of 50 μm.

For certain applications, printing non-metals, like thermoelectrics, would be beneficial for subcooling optics, like detectors that need cold stable temperatures. Zhang *et al* demonstrated the printing of Bi_2Te_3 thermoelectric material [43], [44]. The demonstrated properties were similar to bulk Bi_2Te_3.

C. Demonstration of Package Level 3D-printed Direct Jet Impingement Cooling Applied to High Power, Large Die Applications

With the increasing demand on the functionality and higher computation performance for high performance chips, the die size is continuously increasing. For example, the die size has increased from 12 mm^2 in 1971 to 688 mm^2 in 2019 for Intel microprocessors, and from 270 mm^2 in 1998 to 696 mm^2 in 2019 for IBM microprocessors [45]. Moreover, the chip power also increases with the increase of performance, especially for the emerging applications, such as machine learning or AI, HPC and networking applications such as 5G [46]. This creates a concern due to the temperature gradient and hence the non-uniform cooling over the chip surface. The regular cooling solutions such as interlayer cooling [47] and intra-die cooling [48] have been proposed and demonstrated, showing high cooling performance. These solutions are however not compatible with the fine pitch requirements for high bandwidth communication between different tiers of a 3D system. Microscale jet impingement cooling on the bare die is an efficient cooling technique where the liquid coolant is directly ejected on the chip backside. However, these methods require the different individual parts to be fabricated separately and then assembled together via photolithographic techniques [49], [50].

AM-based 3D printing technique called Stereolithography (SLA) is regarded as a promising technique for on-demand electronics manufacturing [51], [52] and for the fabrication of complex geometries in various materials, which can provide more design flexibility for the complex internal geometry of microfluidic coolers. As an example, Wei et al. have demonstrated, for the first time, a liquid jet impingement cooling concept with a scalable nozzle array that can be applied to the large die size applications, for a die sizes above 500 mm^2, and for high power applications (> 250W) [53], [54]. The objective is to provide a proof-of-concept that this cooling solution, that was previously demonstrated on the small die size of the test chip, can be scaled-up to relevant chip sizes and power dissipation values. This work presents the design, fabrication, and experimental characterization of the 3D printed large-die cooler as one single piece and the assessment of the cooler performance over a 1000 hrs long period of operation as shown in **Figure 4** and **5** below.

The heatsink achieves a chip temperature increase of 17.5°C at a chip power of 285 W for a coolant flow rate of 3.25 LPM, demonstrating that 3D printing enables the design for low-cost, high efficiency direct on-chip microfluidic heatsink with complex internal 3D manifold liquid delivery channels. Long term thermal tests of 1000 hrs show no reliability issues and a constant thermal performance with no degradation of the cooler material. The benchmarking study shows that the 3D printed microfluidic heatsink improves cooling performance by a factor of 5 combined with a large reduction in cooler size and weight, compared to a standard air-cooled heat sink.

III. Challenges

Although the AM-based packaging processes have many attractive features, they are not without limitations. These disadvantages vary from one AM approach to another, but we would like to highlight some of them that are universal in nature [55], [56].

One such challenge is issues seen with reproducing functionality – in most cases, no two parts function in the same manner due to inconsistency in printing / post-processing parameters and varying material properties. Secondly, there is a lack of standards / data / tools available for design-stage assessment of the process modeling, performance and reliability of the packaging architectures built using additive processes. Specifically, the integration of ECAD and relevant MCAD tools to support electrical design, and modeling of key physical behavior such as electrical, thermal and mechanical. Such analysis tool integration will ensure that designs can be assessed at the early design stage in terms of their performance and stress reliability [57]. Current substrates being built from AM processes have a tensile strength of 70 MPa that can survive heat deflection temperatures up to ~ 190°C with a dielectric strength of ~10 kV/mm. Understanding the behavior of printed materials as they are deposited and cured will ensure that quality of the fabricated parts meet industry requirements. In addition, the current AM-based processes used to build parts are relatively slow with speeds not more than 15 mm/hr (leading to low manufacturing throughputs) and have poor resolution (minimum line and

space width ~ 40 μm & ~ 100 μm respectively) and electrical conductivity (trace conductivity on the order of 12×10^{-8} Ω.m) compared to traditional electronic packaging technologies they aim to replace / compliment in the future.

IV. Conclusions

In summary, several AM-based processes such as 3D printing have been disrupting the design and manufacturing of functional electronic products. It promises to deliver unlimited differentiated products and unprecedented part performance through precise internal geometries and economical customized parts. Some of the established additive manufacturing techniques, such as inkjet printing, selective laser melting (SLM), polyjet printing (PJP) and stereolithography (SLA), have already been adopted for prototype manufacturing in 3D electronic packaging. Despite being available for many years now, these processes have been primarily used for rapid prototyping and manufacturing of low volume parts as seen in the research works highlighted in this article. As the advancements in processes and materials continue, and the software tools become available—these additive assembly technologies will be adopted on a wider scale by the electronics packaging industry for advanced applications in IoT, MEMS, RF, HPC, AI and 5G space. It is likely that a hybrid approach may result over time, combining the best of both worlds , incorporating in aspects of additive-based BA processes in concert with traditional SiP manufacturing methods.. Finally, as discussed towards the end, challenges need to be overcome related to the need for suitable materials (particularly functional materials), improved throughput, integrated heat sinks, reliability, and required dimensions and tolerances.

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