



IEEE ELECTRONICS PACKAGING SOCIETY

Newsletter



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Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN



Kitty Pearsall
Boss Precision, Inc.
Austin, TX

At year end the EPS President's gavel passed to me from Chris Bailey to continue the governance of the Electronic Packaging Society. I am really looking forward to this exciting challenge and I will continue to reinforce all the established initiatives/goals of the EPS functional teams (Technology, Education, Conferences, Membership, Chapters, and Finance) and will supplement these as needed.

I want to personally thank Chris for his contribution to the Society and acknowledge that his leadership has driven two remarkably successful years of achievements despite the continuing Covid crisis. Yes, EPS continued its activities, but all of us learned that adaptation of how we do things had to occur to stay relevant in the new, mostly virtual, environment.

Covid restrictions impacted EPS Conferences in 2021 and will continue to do so. Almost 70% of the twenty-six planned conferences were virtual; 15% of conferences were in person. The remaining conferences were hybrid events. While the virtual conferences enabled EPS to continue its presence in the technical community the amount of time, commitment and dedicated effort was extensive and quite tedious.

Since EPS is the leading international forum for scientists and engineers engaged in the research, design, and development of revolutionary advances in microsystems packaging and manufacturing, it is imperative that two critical goals of the EPS Technology Communities be strengthened: first, positioning EPS as a preferred information source of disruptive packaging technology and, second, optimizing the value of outreach by Technical Communities to conferences, societies, local chapters, standard activities, in and beyond EPS. Only by doing this can we increase and grow our society's benefits to its internal and external community.

Looking back, I want to note a few, high-level achievements from 2021. Overall EPS membership has tracked the IEEE society membership exhibiting slight growth. However, Region 10 membership alone has shown a strong, YoY growth from 616 in 2018 to 688 members in 2021. The student chapters' YoY membership has increased from 167 in 2018 to 221 in 2021. The number of student chapters grew from 7 in 2018 to 22 in 2021. This significant

increase in the number of student chapters as well as increase in members is attributed to the introduction of the Student Chapter Continuation Program (SCCP) and Student Chapter Promotion Program (SCPP) introduced in 2020 and 2021.

Peer-reviewed technical articles were submitted monthly to the EPS eNews and biannually to the EPS Newsletter from the EPS Technical Communities in 2021 and this will continue in 2022.

The EPS Resource Center went live in 2021. It is the IEEE Electronics Packaging Society's online library of webinars, lectures, presentations and more. In the EPS Resource Center, there are videos from the world's leading electronics packaging experts at your fingertips. This can be extremely beneficial in maintaining and enhancing one's technical expertise. Be sure to check it out!

Looking forward I want to focus on EPS partnering with both internal IEEE Societies as well as external societies and organizations in India, Japan, Europe, and the Americas. While EPS is off to a good start with the Young Professionals and the women engineers I hope to drive a more diverse and inclusive set of membership initiatives. So be on the lookout! Perhaps, you have a few ideas that you would like to share with the Board of Governors (BoG).

Lastly, I want to express my gratitude for the strong support provided to the EPS Board of Governors from all Directors, VPs, volunteers, appointees, and members at large. I look forward to working with each and every one of you.

Please join me in congratulating our new and continuing Officers and BOG Directors:

- Dave McCann, VP Technology

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NEWSLETTER SUBMISSION DEADLINES

15 June 2022 for Summer issue 2022

1 December 2022 for Winter issue 2022

Submit all material to d.manning@ieee.org

EPS Officers

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Jr. Past Pres.: Chris Bailey, C.Bailey@greenwich.ac.uk

Members At Large

2022 Term End: Regions 1-6, 7, 9—Rozalia Beica, Xuejun Fan, Subramanian S. Iyer, Region 8—Tanja Braun, Karlheinz Bock, Region 10—Gu-Sung Kim
2023 Term End: Regions 1-6, 7, 9—Mark Poliks, Annette Teng, Patrick McCluskey, Jin Yang, Region 8—Steffen Kroehnert, Region 10—Yoichi Taira, Young Professional—Yan Liu
2024 Term End: Regions 1-6, 7, 9—Benson Chan, Pradeep Lall, Wolfgang Sauter, Region 10—Kishio Yokouchi, Chuan Seng Tan, Chin-Pin (CP) Hung

Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:

Ravi Mahajan

Co-Editor Special Topics:

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Co-Editor, Electrical Performance:

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Co-Editor, Components: Characterization and Modeling:

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Emerging Technology:

Benson Chan

Nanotechnology:

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Power & Energy:

Patrick McCluskey

RF & Thz Technologies:

Manos Tentzeris

Photonics—Communication, Sensing, Lighting:

Gnyaneshwar Ramakrishna

3D/TSV:

Peter Ramm

Reliability:

Richard Rao

Test:

Pooya Tadayon

Program Directors

Chapter Programs: Toni Mattila, toni.mattila@investinfinland.fi

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Nominations: Chris Bailey, C.Bailey@greenwich.ac.uk

Distinguished Lecturers

VP Education: Jeff Suhling, jsuhling@auburn.edu

Lecturers: Ramachandra Achar, Ph.D., Mudasir Ahmad, Kemal Aygün, Ph.D., Muhammad Bakir, Ph.D., W. Dale Becker, Ph.D., Wendem Beyene, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., William T. Chen, Ph.D., Xuejun Fan, Ph.D., Philip Garrou, Ph.D., Madhu Iyengar, Ph.D., Subu Iyer, Ph.D., Beth Keser, Ph.D., Pradeep Lall, Ph.D., John H. Lau, Ph.D., Ravi Mahajan, Ph.D., James E. Morris, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Eric D. Perfecto, Mark Poliks, Ph.D., Jose Schutt-Aine, Ph.D., Nihal Sinnadurai, Ephraim Suhir, Ph.D., Chuan Seng Tan, Ph.D., Rao Tummala, Ph.D., E. Jan Vardaman, Paul Wesling, C.P. Wong, Ph.D., Jie Xue, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

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Douglas C. H. Yu Receives the 2022 IEEE Rao R. Tummala Electronics Packaging Award



Douglas C. H. Yu
Taiwan Semiconductor Manufacturing Company, Vice President
Hsinchu, Taiwan

“For contributions to the development of advanced packaging technologies and their implementation in high-volume manufacturing.”

Douglas C.H. Yu’s leadership in developing advanced packaging technologies has paved the way for new technology standards and semiconductor trends that have supported the continued scaling of microelectronics and are enhancing high-performance computing, wireless, and artificial intelligence applications. Among Yu’s many accomplishments, at Taiwan Semiconductor Manufacturing Corporation he led the introduction of the copper/low-k dielectric interconnects, which provided a significant improvement in on-chip wiring performance. He also led the development of the innovative TSMC 3DFabric system integration technology platform, which includes chip-on-wafer-on-substrate (CoWoS), integrated fan-out (InFO) wafer-level-package, and system-on-integrated chip (SoIC) technologies. This holistic solution for advanced packaging is critical to continued improvement in performance, power, and form factor of heterogeneous integrated microelectronic systems for above-stated wide applications.

An IEEE Fellow and a Distinguished Fellow of TSMC Academy, Yu is vice president of Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

2021—Chin C. Lee

“For contributions to new silver alloys, new bonding methods, flip-chip interconnect, and education for electronics packaging.”

2020—Mitsumasa Koyanagi and Peter Ramm

“For pioneering contributions leading to the commercialization of 3D wafer and die level stacking packaging”

2019—Ephraim Suhir

“For seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems.”

2018—William Chen

“For contributions to electronic packaging from research and development through industrialization, and for his leadership in strategic roadmapping.”

2017—Paul Ho and King-Ning Tu

“For contributions to the materials science of packaging and its impact on reliability, specifically in the science of electromigration.”

2016—Michael Pecht

“For visionary leadership in the development of physics-of-failure-based and prognosticsbased approaches to electronic packaging reliability.”

2015—Nasser Bozorg-Grayeli

“For contributions to the advancement of microelectronic packaging technology, manufacturing, and semiconductor ecosystems.”

2014—Avram Bar-Cohen

“For contributions to thermal design, modeling, and analysis, and for original research on heat transfer and liquid-phase cooling.”

2013—John Lau

“For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging.”

2012—Mauro J Walker

“For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations.”

2011—Rao R. Tummala

“For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging.”

2010—Herbert Reichl

“For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging.”

2009—George G. Harman

“For achievements in wire bonding technologies.”

2008—Karl Puttlitz Sr. and Paul A. Totta

“For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages.”

2007—Dimitry Grabbe

“For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards.”

2006—C. P. Wong

“For contributions in advanced polymeric materials science and processes for highly reliable electronic packages.”

2005—Yutaka Tsukada

“For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process.”

2004—John W. Balde

“For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing.”

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit <http://www.ieee.org/awards>

New Appointments for 2022

The Electronics Packaging Society Board of Governors appointed its Officers and Program Directors for the two-year term of 1 January 2022 through 31 December 2023. The following individuals were appointed:



President

KITTY PEARSALL (AM’84-M’01-SM’02) received the BS degree in Metallurgical Engineering (1971) from the UT El Paso. Kitty received the MS and Ph.D. degree in Mechanical Engineering and Materials from the UT Austin in 1979 and 1983 respectively. Kitty worked for IBM from 1972 to 2013. In 2005 Kitty was appointed an IBM Distinguished Engineer and was elected to the IBM Academy of

Technology. Kitty was a process consultant and subject matter expert working on strategic initiatives impacting component qualification and end quality of procured commodities. She engaged with worldwide teams implementing cross-brand, cross commodity processes/products that delivered high quality/high reliability end product.

Kitty received 4 IBM Outstanding Technical Achievement Awards; holds 9 US patents; 2 patents pending; and 8 published disclosures. She has numerous internal publications as well as 22 external publications in her field. Kitty is a licensed Professional Engineer (Texas since 1993). Kitty was the recipient of the UT Austin—Cockrell Engineering Distinguished Engineering Graduate Award in 2007 followed by induction into the UT Mechanical Engineering Dept. Academy of Distinguished Alumni in 2008. Kitty was awarded the Women in Technology Fran E. Allan Mentoring Award (2006) in recognition of her people development both in and outside of IBM. Currently Kitty is President of Boss Precision Inc. and works as an Independent consultant. This has included a one year engagement with Shainin Corporation.

Kitty is an active member in IEEE and CPMT. She is a member of TMS, American Society of Metals, and WIE. Kitty has more than 22 years’ experience with ECTC serving as a member of the ECTC Manufacturing Technology Committee (1993-2013) and as the Professional Development Course Chair since 2006. During Kitty’s 10 years on the CPMT Board of Governors she has served in many roles: Member at Large, Strategic Awards Director, VP of Education and currently Director of Chapter Programs. In each role Kitty made key contributions.

Kitty introduced the Regional Contribution Awards. She established the baseline for the CPMT Distinguished Lecturer’s (DLs)

Program. The history of the DLs presentations to Universities, Research Centers, Conferences and CPMT Chapters was charted to determine if the program was meeting its founding principal; i.e., primarily supporting the CPMT chapters. Review of the data noted that this was not the case. Therefore Kitty focused on increasing Chapter usage which did improve over time. DL Budget tracking of planned versus actuals was initiated. Lastly, Kitty documented the roles and responsibilities of the VP Education and passed these on to the new VP. As Director of Chapter Programs Kitty is focusing on worldwide Chapter Communication as well as ensuring Chapters know their benefits and how to access them. First deliverable was a Worldwide Chapter Communication Survey highlighting best practices amongst them.



Vice President,
Technology

DAVID MCCANN (M’89) David McCann is Vice President of Package Engineering at Rockley Photonics. Rockley develops and produces integrated silicon photonics products, including products for biomarker sensors and datacom applications. Previously David was at GlobalFoundries for seven years, as Vice President of Post Fab, which included development and operations for bump, probe, assembly, and test. Prior to GlobalFoundries, David was at Amkor Technology for 11 years leading flip chip technology development and the flip chip business unit, and at Biotronik for 9 years developing and manufacturing implanted medical products. He has degrees from the University of Illinois and Santa Clara University and his technical background is materials science.

David is presently the VP of Technology for the IEEE Electronics Packaging Society (EPS) and previously was a member of the ECTC Executive Committee for 10 years.



Vice President,
Conferences

SAM KARIKALAN (M: 1995, SM: 2003) has 32 years of experience in the Semiconductor and Electronic Systems Industry. He is currently a Senior Manager of Package Engineering R&D at Broadcom Inc., responsible for Electrical, Thermal and Mechanical design analysis and optimization of IC Packages, Advanced Packaging Technology Path-finding, and co-design of IPs and Systems. Prior to Broadcom, Sam held technical or managerial positions

at STATS ChipPAC, Primarion and Advanced Micro Devices, working on IC Package Design for Signal/Power Integrity and Electromagnetic Compatibility (EMC). Before entering the

semiconductor industry in 1998, Sam was a scientist at SAMEER-Centre for Electromagnetics in India, for over a decade, working on EMI/EMC Research & System Design and Radar technology. His current interests include Heterogeneous Integration Technologies, Design for Performance & Reliability, and Design for Test & Manufacturing.

Sam has 23 issued US patents to his credit, on Interconnect design, 2.5D/3D Packaging and EMI/EMC. He also has authored/co-authored 14 Conference/Journal papers on IC Packaging, Signal Integrity and EMI/EMC and delivered few hundred hours of training lectures on Signal/Power Integrity and EMI/EMC at locations all across the globe, including two PDCs at the IEEE Electronic Components and Technology Conference (ECTC). Sam holds a B.E. degree in Electronics & Communications Engineering from Bharathiar University, Coimbatore, India.

Sam has been a member of the IEEE for over 20 years. He has been very active in local chapters and sections in Singapore, Phoenix and Orange County (California), in various leadership roles, including the founding chairperson of the CPMT Orange County chapter. Sam has received several awards for his contributions to the IEEE, including the 2014 IEEE CPMT Regional Contributions Award - Regions 1-6, 7, 9 (US, Canada, Latin America) and the 2012 Outstanding Leadership Award from the Orange County Section. Sam has been serving on the Technical Program Committee and the Executive Committee of the IEEE ECTC since 2006. Sam was the General Chair of the 2018 IEEE 68th ECTC.



Vice President,
Publications

RAVI MAHAJAN is an Intel Fellow and the Co-director of pathfinding and assembly and packaging technologies for 7-nanometer (7nm) silicon and beyond in the Technology and Manufacturing Group at Intel Corporation. He is responsible for planning and carrying out multi-chip package pathfinding programs for the latest Intel process technologies. Ravi also represents Intel in academia through research advisory boards, conference leadership and participation in various student initiatives.

Ravi has led efforts to define and set strategic direction for package architecture, technologies and assembly processes at Intel since joining the company's Assembly and Test Technology Development organization in 2000, spanning 90 nm, 65 nm, 45 nm, 32 nm, 22 nm and 7 nm silicon. Earlier in his Intel career, he spent five years as group manager for thermal mechanical tools and analysis. In that role, Mahajan oversaw a Thermal-Mechanical Lab chartered with delivering detailed thermal and mechanical characterization of Intel's packaging solutions for current and future processors.

A prolific inventor and recognized expert in microelectronics packaging technologies, Mahajan holds more than 30 patents, including the original patent for a silicon bridge that became the foundation for Intel's Embedded Multi-Die Interconnect Bridge technology. His early insights also led to high-performance, cost-effective cooling solutions for high-end microprocessors and the proliferation of photo-mechanics techniques used for thermo-mechanical stress model validation. Ravi has written several book chapters and more than 30 papers on topics related to his area of expertise.

Ravi joined Intel in 1992 after earning a bachelor's degree from Bombay University, a master's degree from the University of Houston, and a Ph.D. from Lehigh University, all in mechanical engineering. His contributions during his Intel career have earned him numerous industry honors, most recently the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI award from SEMITHERM and the 2016 Allan Kraus Thermal Management Medal from the American Society of Mechanical Engineers. He has also been nominated as an IEEE EPS Distinguished Lecturer. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently Co-Editor for Special Topics of IEEE T-CPMT. Additionally he has been long associated with ASME's InterPACK conference and was Conference Co-Chair of the 2017 Conference. Ravi is a Fellow of two leading societies, ASME and IEEE. He was named an Intel Fellow in 2017.



Vice President,
Education

JEFFREY C. SUHLING received a B.S. degree in Applied Mathematics and Physics, and M.S. and Ph.D. degrees in Engineering Mechanics from the University of Wisconsin, Madison, WI. He joined faculty of the Department of Mechanical Engineering at Auburn University in 1985, where he currently holds the rank of Quina Distinguished Professor. Dr. Suhling co-established the NSF Center for Advanced Vehicle and Extreme Environment Electronics (CAVE3) in 1998,

and served as Center Director from 2002–2008. CAVE3 is a government and industry sponsored research center involving over 20 member companies, 15 faculty, and 35 graduate students that specializes in reliability of electronic packaging in harsh environments. In 2008, he was appointed Department Chair of the Department of Mechanical Engineering, which is the largest program at the University with over 1000 undergraduate students and 150 graduate students. He was selected "Outstanding Mechanical Engineering Faculty Member" by the undergraduate students during 1990, received the College of Engineering Birdsong Superior Teaching Award in 1994, and received the College of Engineering Senior Research Award in 2001. He has advised 75 graduate students at Auburn University, including 27 Ph.D. students and 48 M.S. students.

Dr. Suhling has been an active researcher in electronic packaging for over 25 years. His general areas of interest are in the mechanics and reliability of packaging. Specializations include silicon sensors for packaging stress and temperature measurements, stress effects in silicon devices, test chips, mechanical characterization of packaging materials including solders and polymers, solder joint reliability and aging effects, and finite element modeling. He has authored or co-authored over 375 technical publications, including 6 books and book chapters, 55 journal articles, and 325 conference proceedings papers. Six of his conference papers have been selected as the Best of Conference. These include Best Session Paper Awards at the 2005 and 2010 ECTC Conferences, as well as Best Paper Awards at the 1998 and 2002 IMAPS Annual Conferences, 2008 SMTA International, and 2013 InterPACK Conference. In addition, he and his co-authors have received Best Poster awards at the InterPACK 2007, InterPACK 2009, and InterPACK 2013 conferences.

Dr. Suhling is a member of IEEE/EPs, ASME, IMAPS, and SMTA. In IEEE, he has served on the ECTC Applied Reliability program committee for the past 10 years. He was appointed to the ECTC Professional Development Course (PDC) program committee in 2006, and has served as Assistant Chair. He has also been active in the IEEE/EPs ITherm Conference series, serving on the program committee for over 10 years. In ASME, Dr. Suhling served as Chair of the Electrical and Electronic Packaging Division (EPPD) during 2002–2003, and was on the EPPD Executive Committee from 1998–2003. Dr. Suhling was the Technical Program Chair of the InterPACK '07 Conference, and General Chair of the InterPACK '09 Conference. He was elected a Fellow of ASME in 2009, and was recognized with the ASME-EPPD Mechanics Award for outstanding contributions to electronic packaging research. Jeff has served as a member of the EPs Board of Governors since 2014 and as Program Director- Membership Programs from 2016–2018.



Vice President,
Finance

and packaging, flip chip on board and chip scale packages, to multi-chip packaging, MEMS, optoelectronic packaging, and high performance portable packaging. He has led teams at Bell Labs, AMI Semiconductors, and Motorola (now Freescale). Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he currently leads fine pitch Cu pillar interconnect and TSV packaging technology development.

Pat is active in industry-consortia and industry-university partnerships, including mentoring SRC custom projects and PhD students.

Pat has five patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He is a member of the Electronic Components and Packaging Technology Conference technical program committee, where he has held multiple positions, including General Chair of the 2006 ECTC, and continues to serve as Financial Chair. He has served at both the local and Society level of EPs holding positions including Member-at-Large of the Board of Governors, Administrative Vice President, and Vice President of Technology.



Vice President,
Membership

ALAN HUFFMAN (M: 2005, SM: 2007)

is currently the Director of Engineering for Micross Advanced Interconnect Technology in Research Triangle Park, NC. He received the B.S degree in physics from The University of North Carolina at Chapel Hill in 1994. From 1994 to 2005 he was a Member of the Technical Staff at MCNC Research & Development Institute working on development and implementation of

wafer level packaging technologies, reliability and failure mode analysis of flip chip devices, and optoelectronic and MEMS packaging. In 2005, he joined RTI International and was a Senior Research Engineer and Program Manager for WLP technology with RTI's Electronics and Applied Physics Division. His technical interests include wafer level packaging and flip chip process technology and fine pitch bump interconnect, 2.5D and 3D integration technology, characterization and process development for electronic materials used in WLP. He has authored or co-authored numerous papers and presentations on a number of advanced packaging topics, particularly on high density interconnect technologies and characterization of polymer material processes.

Alan is an IEEE Senior Member whose activities include, member of ECTC Interconnects technical sub-committee from 2005–2013, Chaired multiple ECTC technical sessions during this period, member of ECTC Executive Committee 2011–present, 2016–17—Jr. Past General Chair, 2015–16—General Chair, 2014–15—Vice General Chair, 2013–14—Program Chair, 2012–13—Asst. Program Chair, 2011–12—Web Administrator. Alan was appointed to the EPs Board of Governors in 2016 and has been a contributing member of the Board through various ad-hocs including Branding Change, Membership and Conference Functional Teams.

PATRICK THOMPSON (M'87, SM'92) earned his BS, MS and PhD degrees in Chemical Engineering at the University of Missouri-Rolla. He has more than 25 years of experience in advanced packaging research, development and transfer to manufacturing, contributing to technologies ranging from flip chip fabrication



Program Director,
Chapter Programs

TONI MATTILA (M'08) is a research scientist and docent at Aalto University in Helsinki, Finland where he leads a research team that focuses on the reliability of electronic devices. He received his Ph.D. degree in electrical engineering in 2005 and an M.Sc. degree in materials science and engineering in 1999 from the Helsinki University of Technology (HUT). Since 1996, he has been working with electronics production technologies and reliability of electronic devices both in industrial and academic settings. Before joining HUT in 1999 he worked in Tellabs and Nokia.

Toni's research has focused on electronics production technologies, soldering in electronics, failure mechanisms of electronic assemblies, MEMS technologies, and the development of improved methods for reliability assessment and lifetime prediction. Within the framework of his research Toni has been working in close cooperation with international electronics industry, research institutions and universities. His research has so far resulted in over fifty publications in scientific and technical journals and conferences. In addition, Toni has authored seven book chapters, held several professional tutorials during conferences and been a frequent speaker at conferences, seminars and technology fairs. He is also a frequent reviewer in several scientific journals, including CPMT Transactions.

Since 2008, Toni has been Chairman of the CPMT Finland Chapter. During this time he has, together with other board members, developed and revitalized local activities. More than 100 people attend seminars and events organized by the CPMT Finland chapter annually. He has also established firm connections between the CPMT chapters in Scandinavia. Toni is currently an elected member of the Board of Governors of the CPMT.

Toni also works actively in the IEEE Finland Section, where he has been a member of the executive committee since 2008, and served in various positions. Other IEEE activities include, for example, a membership of technical committees for all three Electronics System Integration Technology Conferences (ESTC). In the past he has also acted in several other positions of trust. For example, he has been the chairman of a housing association for ten years.



Program Director,
Award Programs

PATRICK MCCLUSKEY (M: 1985, SM: 2015) (B.S.('84) Lafayette College; M.S.('86) and Ph.D. ('91), Materials Science and Engineering, Lehigh University) is a Professor of Mechanical Engineering at the University of Maryland, College Park and the Mechanical Engineering Department's Division Leader for Electronic Products and Systems. He has over 25 years of research experience in the areas of thermal management, reliability, and packaging of

electronic systems for use in extreme temperature environments and power applications. Dr. McCluskey has published three books and over 125 peer-reviewed technical articles with over 2000 citations, including over 40 articles in IEEE journals and major EPS conferences, such as ECTC and iTHERM. He has also served as technical program or general chair of IEEE conferences on high temperature electronics and integrated power electronic packaging, as well as being the organizer of the President's panel session on Power Module Integration at ECTC 2016, and panel sessions at iTHERM and ITEC. Dr. McCluskey has provided a short course on integrated thermal packaging of power electronics at ECTC and iTHERM since 2013, along with short courses at IWIPP and 3D-PEIM. He is an associate editor of the IEEE Transactions on Components, Packaging, and Manufacturing Technology, and of Microelectronics Reliability. He is a senior member of IEEE and the chair of the EPS Technical Committee on Energy and Power Electronics. He has also served as IEEE EPS representative to the Future Car Workshop. He is a fellow of IMAPS and a member of ASME and TMS/AIME.



Program Director,
Student Programs

MARK POLIKS (M: 2004) is Empire Innovation Professor of Engineering, Professor of Systems Science and Industrial Engineering, Professor of Materials Science and Engineering and Director of the Center for Advanced Microelectronics Manufacturing (CAMM) at the State University of New York at Binghamton. In 2006 he established the first research center (CAMM), to explore the application of roll-to-roll processing methods to

flexible electronics and displays, with equipment funding from the United States Display Consortium (USDC) and the Army Research Lab. His research is in the areas of industry relevant topics that include: high performance electronics packaging, flexible hybrid electronics, medical and industrial sensors, materials, processing, aerosol jet printing, roll-to-roll manufacturing, in-line quality control and reliability.

He has received more than \$20M in research funding from Federal, New York State and corporate sources and more than \$30M in equipment funding from federal and state sources. He is the recipient of the SUNY Chancellor's Award for Excellence in Research. He leads the New York State Node of the DoD NextFlex Manufacturing USA and was named a 2017 NextFlex Fellow. He has authored more than one-hundred technical papers and holds forty-six US patents. Previously he held senior technical management positions at IBM Microelectronics and Endicott Interconnect. Poliks is a member of technical councils for the FlexTech Alliance, NBMC and NextFlex, and on the NextFlex Governing Council. He is an active member of the IEEE Electronics Packaging Society Electronic Component and Technology Conference and served and the 69th ECTC General Chair. Poliks received dual undergraduate degrees, with honors, in chemistry and mathematics from the University of Massachusetts and a Ph.D. from the University of Connecticut in materials science and engineering. He was a McDonnell-Douglas post-doctoral fellow working on solid-state magnetic resonance at Washington University, St. Louis before starting his career at IBM.



Program Director,
Industry Programs

WILLIAM T. CHEN (M'92, SM'03, F'06) received his engineering education at University of London (B.Sc), Brown University (M.Sc) and Cornell University (PhD). He joined IBM Corporation at Endicott New York in 1963.

At IBM he worked in a broad range of IBM microelectronic packaging products. He received IBM Division President Award for his leadership and innovation in Predictive Modelling on IBM products. He was elected to the IBM Academy of Technology for his contributions to IBM Products and Packaging Technologies. He retired from IBM in 1997. He joined the Institute of Materials Research and Engineering (IMRE) in Singapore, to initiate research in micro-electronic packaging materials and processes. He was appointed to the position Director of the Institute (IMRE) steering the growth in people, funding and research facilities and research direction for IMRE to become the leading materials science and engineering research center in the ASEAN region. In 2001 he joined ASE Group, where he holds the position of ASE Fellow and Senior Technical Advisor. In this assignment he has responsibilities for guidance to technology strategic directions for ASE Group.

He is Senior Past President of the IEEE/CPMT Society. He is the Co-Chair of the ITRS Assembly and Packaging Roadmap Technical Working Group. He is chair of the Semicon West Packaging Committee. He has been elected to a member of the iNEMI Board. He is a member of the Technology Committee of GSA.

He has been elected to Fellow of IEEE and Fellow of ASME. He has served as an Associate Editor of ASME Journal of Electronic Packaging, and IEEE/CPMT Transactions.

ANNETTE TENG (SM: 2001) is the Chief Technology Officer at Promex Industries, a manufacturer of electronic and medical components in Silicon Valley, since 2014. She has spent most of her career in electronic component packaging and manufacturing in both corporate and academic environments. Born in Borneo



Program Director,
Regions 1-6 & 7
Programs

Science and Technology and helped launch their electronics packaging programs from 1997 to 2000. She has published at ECTC and Meptec in the area of dicing, die attach films and package delamination. She has been active in IEEE-EPS Chapter activities in Silicon Valley since 2000 and is currently the Chair of the IEEE-EPS Santa Clara Chapter.



Program Director,
Region 8 Programs

destructive tools and advanced polymer analysis. Recent research is focused on wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. In 2013, she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins.

Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun holds also several patents in the field of advanced packaging. In 2014, she received the Fraunhofer IZM research award.

(Malaysia), she left at 16 to attend Sweet Briar College in Virginia. After Graduating from University of Virginia with a Ph.D. in Materials Science, she moved to Silicon Valley and started her career in the IC world at Signetics. She has worked in components packaging and assembly at Philips Semiconductor, Linear Technology Corp. and Corwil Technology. Prior to joining Promex, she was Package Assembly Manager at Silanna in Australia for 3 years. She also worked at Hong Kong University of

Tanja Braun is an active member of IEEE. She is member of the IEEE EPS Technical Chapter “Materials & Processing” and the Award Committee as well as the IEEE EPS Women in Engineering (WIE) delegate. Currently she is also ECTC subcommittee chair of “Materials & Processing”.



Program Director,
Region 10 Programs

electronics and EV battery systems, reliability of solar photovoltaic modules and fracture mechanics. To date he has published more than 250 technical papers, 4 book chapters, 7 keynote presentations, 11 invited presentations, 3 panel discussions, and co-edited 4 conference proceedings and two special issues of technical journals.

Dr Tay was the inaugural General Chair of the 1st and 2nd Electronics Packaging Technology Conference (EPTC) in 1997 and 1998. Since then, he has been in the organising committee of EPTC. In 2006 he was appointed the inaugural Chairman of the EPTC Board, charged with steering the development of EPTC, and is currently again serving as its Chairman. He has been in the Executive Committee of the Singapore Joint Reliability/CPMT/ED Chapter since 2000 and was its Chairman from 2010-2011. He has been involved in the international advisory boards and program committees of more than 108 electronics packaging conferences worldwide including DTIP, ECTC, EMAP, EPTC, EuroSimE, HDP, ICEPT, IEMT, IMPACT, InterPack, IOTHERM and THERMINIC.

Dr. Tay was an Associate Editor of the ASME Journal of Electronics Packaging, an editorial board member of several journals including Microelectronics Journal and Finite Elements in Analysis and Design, and a guest editor of a special issue on Microelectronics Reliability.

He has contributed significantly as a member of the IEEE EPS Education Committee from 1998 to 2007 where he helped to evaluate projects on web-based educational modules.

ANDREW TAY (M'91) is currently a Senior Research Fellow at the Singapore University of Technology and Design. Prior to this he was a Professor in the Department of Mechanical Engineering, National University of Singapore (NUS). He obtained his B.E. (Hons I and University Medal) and PhD in Mechanical Engineering from the University of New South Wales, Australia. His research interests include thermo-mechanical failures, thermal management of

Newly Elected Members of the Electronics Packaging Society Board of Governors

In 2021, EPS members elected new Members-at-Large to the EPS Board of Governors for the three-year term of 1 January 2022 through 31 December 2024:

REGIONS 1-6, 7 & 9



PRADEEP LALL (StM: 1990, M:1993, SM: 2008, F: 2012) is the MacFarlane Endowed Distinguished Professor with the Department of Mechanical Engineering and Director of the NSF-CAVE3 Electronics Research Center at Auburn University. He holds Joint Courtesy Appointments in the Department of Electrical and Computer Engineering and the Department

of Finance. He is a member of the technical-council, academic co-lead of the asset-monitoring TWG of NextFlex Manufacturing Institute. He is the author and co-author of 2-books, 14 book chapters, and over 700 journal and conference papers in the field of electronics reliability, safety, energy efficiency, and survivability. Dr. Lall is a fellow of the ASME, fellow of the IEEE, a Fellow of NextFlex Manufacturing Institute, and a Fellow of the Alabama Academy of Science. He is recipient of the Auburn Research and Economic Development Advisory Board Award for Advancement of Research and Scholarship Achievement, IEEE Sustained Outstanding Technical Contributions Award, National Science Foundation's Alex Schwarzkopf Prize for Technology Innovation, Alabama Academy of Science's Wright A. Gardner Award, IEEE Exceptional Technical Achievement Award, ASME-EPPD Applied Mechanics Award, SMTA's Member of Technical Distinction Award, Auburn University's Creative Research and Scholarship Award, SEC Faculty Achievement Award, Samuel Ginn College of Engineering Senior Faculty Research Award, Three-Motorola Outstanding Innovation Awards, Five-Motorola Engineering Awards, and over Thirty Best-Paper Awards at national and international conferences. Dr. Lall has served in several distinguished roles at national and international level including serving as member of National Academies Committee on Electronic Vehicle Controls, Member of the IEEE Reliability Society AdCom, IEEE Reliability Society Representative on the IEEE-USA Government Relations Council for R&D Policy, Chair of Congress Steering Committee for the ASME Congress, Member of the technical committee of the European Simulation Conference EuroSIME, and Associate Editor for the IEEE Transactions on Components and Packaging Technologies. He received the M.S. and Ph.D. degrees in Mechanical Engineering from the University of Maryland and the M.B.A. from the Kellogg School of Management at Northwestern University.

STATEMENT OF INTEREST

If elected to the EPS Board-of-Governors, I am interested in enhancing the presence of IEEE-EPS publications and conferences in new emerging areas including—harsh-environment electronics, automotive electronics, prognostics health management, electric vehicles, smart-grid and renewable energy. I will aim to

develop a magazine publication focused on the role of packaging in the above-mentioned areas and positioning the newly conceived IEEE publications advantageously in terms of visibility and reach. My past experience in leadership roles within the IEEE and additionally as Director of a successful Research Center at Auburn University will help in working with key personnel in IEEE for developing a path forward in the new emerging areas.



DR. WOLFGANG SAUTER (M: 2016) is a Distinguished Engineer at Marvell.

He received his Ph.D. in Mechanical Engineering from The University of Vermont in 2000, and his M.S. in Mechanical Engineering from The Technical University of Munich in 1997.

From 2000 until 2015, he worked in packaging development at IBM, leading several development projects on new technology introduction, flip chip development, component reliability improvements, and CPI (Chip Package Interaction). With the acquisition of IBM's Microelectronics Division by GLOBALFOUNDRIES, Wolfgang moved to a customer facing role in the ASIC organization, where he was the primary contact for all advanced packaging product discussions, and owns roadmap definition for future technology nodes.

Since joining Marvell in 2019, Wolfgang is responsible for all Marvell ASIC product packaging solutions, and drives the packaging technology roadmap for ASIC and across Marvell.

Wolfgang holds over 130 patents and has authored or co-authored numerous papers and presentations on a number of advanced packaging topics.

STATEMENT OF INTEREST

My particular interest in joining the EPS BOG is to further the sharing of technology advancements and innovation across the industry. Being a member of the ECTC community for the last 18 years has provided me with the opportunity to meet and learn from many of our industry's greatest experts, and I would like to ensure this opportunity continues for young and coming engineers. It is of great importance to me personally that platforms for sharing information and forming cross-industry connections (such as ECTC and the other EPS conferences) remain affordable and accessible to the next generation of engineers. I would therefore like to contribute particularly in the area of EPS conferences, and their technical leadership, as well as financial viability and success.



BENSON CHAN (M: 6/2020, SM: 11/2020) received his B.S. in Mechanical Engineering in 1981 and M.S. in Engineering Science in 1987 from Rensselaer Polytechnic Institute. Mr. Chan has solid background in Electronic Packaging, with strong emphasis in High Speed Applications and Electrical Connector design. Mr.

Chan had a diverse career with IBM for 22 years in the areas of Process Engineer, Design Engineer and Development Engineer. At IBM he was an Advisory Engineer in the Connector Development group responsible for developing custom connectors used in I, P and Z series mainframes for IBM. He

was also the lead mechanical engineer for the development of the first 10Gbps x 12 optical transceiver in IBM. In the last 4 years at IBM, he was a taskforce lead managing members around the world responsible for correcting problems with LGA connectors for Z series systems as well as the 10K RPM hard drives for IBM.

After IBM, he was with Endicott Interconnect Technologies for 12 years as a Chief Scientist. At EIT, he was the principle investigator for the DARPA Terabus III program, responsible for the design and build of a flexible optical waveguide capable of 25Gbps per channel with 48 channels interconnecting 2 hybrid optical modules. For a large DoD project, he provided all packaging options to dense pack the maximum number of processing elements into a given space, he also provided thermal solutions to support a 72 KW cabinet.

Mr. Chan is currently the Associate Director for the Integrated Electronics Engineering Center at Binghamton University, this center is a NY State Center for Advanced Technology and has a mission to work with companies to understand their use of electronics to improve their business by understanding the design, reliability and failures of their products. He has also been instrumental in increasing the exposure of the GE/BU Electronics Packaging Symposium, this is a yearly symposium dedicated to the electronics industry, since starting at Binghamton, this symposium has grown 3 x in attendance and 40 x in exhibitors. It is now seen as the largest east coast event focused on the trends of electronics ranging from power packaging to wearable flexible electronics for medical uses.

Mr. Chan holds 54 Patents in the fields of electronic packaging and advanced Connectors. He has 18 published papers in the fields of electronic packaging and connectors (ECTC, iMAPS, Photonics Journal, Fleck Research).

Mr. Chan is a director for iMAPS and the president of the Empire Chapter of iMAPS. He is the chair of the Emerging Technologies Committee for ECTC and a member of IEEE EPS. He is on the TWG for the Heterogeneous Integration Roadmap for Single/Multichip, MEMS and Mobile.

Mr. Chan received the 2019 iMAPS Outstanding Educator award at the 2019 National iMAPS meeting in Boston.

STATEMENT OF INTEREST

Focus on new and emerging technologies to have knowledge of where it can be applied. I am the current chair of the ECTC Emerging Technology Committee as well as the track chair for the iMAPS Advanced Process and Materials track for iMAPS for the last 4 years, this gives me good insight of what is coming and seeing where this technology can be applied. This helps with interactions in my current role as the Associate director for IIEC during discussion with our member companies. Keeping up with what is coming is also the reason for being part of the Heterogeneous Integrations Roadmap, great way to make contacts as well as understand the challenges of each TWG and where the industry is headed. Knowing this the IIEC can tailor our research to easing the challenges of our member companies.

REGION 10

KISHIO YOKOUCHI (M: 2002, SM: 2016,) is head of Japan Jisso-Interconnect Solutions Laboratory, and Visiting Professor



of Kanto Gakuin University. He has been leading on development of high-end electronics interconnect and thermal management technology field on over 30 years.

He joined FUJITSU Laboratories Ltd. in 1979, where he has been engaged in R&D on High-Density Packaging Integration technologies for supercomputers, based on material science, such as copper co-fired multilayer LTCCs (1990), thin film 2.5D module substrates (1995), and phase change direct liquid cooling technologies. In 2000, he directed R&D of optical monolithic integrated devices at FUJITSU Laboratories of America. From 2005, he was VP of Device & Materials Laboratories, FUJITSU Laboratories Japan. In 2007-17, he joined FUJITSU Interconnect Technologies Ltd. as a VP.

Dr. Yokouchi received his engineering education at Yokohama National University (B.Sc, M.Sc), and the Osaka University (PhD) In society activities, he contributed on IEEE EPS as a BoG member 9 years, Japan chapter chair, and DL. He also contributed technical committee chair of the "High Density Substrates & Boards". He is co-founder of ECTC EPS Seminar, stated as CPMT Plenary Seminar on 2004. He also contributed other societies, President of IMAPS Japan on 2006-12, Vice President of JIEP on 2014-17. He received awards of IMAPS the Sidney J. Stein International Award (2015), and IEEE EPS Regional Contributions Award (2020). He is the author or co-author of 55 technical presentations or publications, also published 3 technical books, 72 U.S. and 100 Japanese patents.

STATEMENT OF INTEREST

EPS has to increase the number of members. In particular, it is important to disseminate the value and attractiveness of EPS in order to acquire next generation young members. Fortunately, in Region-10 area, there are leading packaging-related organizations, such as JIEP (around 2,000 members). I will try to achieve goals by taking advantage of my strong relationships with these organizations.



CHUAN SENG TAN (StM: 2001, M: 2006, SM: 2019) is a Professor of Electronic Engineering at the School of Electrical and Electronic Engineering at Nanyang Technological University, Singapore. He received his PhD from MIT in 2006. Currently, he is working on process technology of three-dimensional integrated circuits (3D IC), as well as engineered substrate (Si/Ge/Sn) for group-IV photonics. He has numerous publications (journal and conference) and IPs on 3D technology and engineered substrates. Nine of his inventions have since been licensed to a spin-off company. He co-edited/co-authored five books on 3D packaging technology.

He is a senior member of IEEE and a recipient of the Exceptional Technical Achievement Award from the IEEE Electronics Packaging Society (EPS) in 2019. Beginning June 2019, he is a Distinguished Lecturer with IEEE-EPS. He is a Fellow of the International Microelectronics Assembly and Packaging Society

(IMAPS) since 2019 and a recipient of the William D. Ashman - John A. Wagnon Technical Achievement Award in 2020.

He was the Chair of the Interconnections Sub-Committee for ECTC'2021. He was the General Chair of the 2020 IEEE Electronics Packaging Technology Conference (Virtual). In addition, he is an Associate Editor for the IEEE Transactions on Components, Packaging and Manufacturing Technology and was recognized with the Best Associate Editor Award in 2021.

STATEMENT OF INTEREST

I have been a member of the IEEE for 21 years and EPS for 10 years. I have had the honour to serve as a member of the Interconnection Sub-committee of ECTC since 2013 and was the Chair in 2021. In 2020, I was the General Chair for the Electronics Packaging Technology Conference (EPTC). My experience with these two roles were under exceptional situation due to disruptions brought by COVID-19. We managed to overcome all challenges and delivered the intended outcomes thanks to strong commitment by the respective teams. In addition, I also served as an associate editor of IEEE Transactions on Components, Packaging and Manufacturing Technology since 2018 and recognized with the Best AE Award in 2021. I have been working on 3D packaging since 2001 and the research contributions have been recognised with the 2019 Exceptional Technical Achievement Award (EPS) and the 2020 William D. Ashman - John A. Wagnon Technical Achievement Award (IMAPS). I am passionate about promoting education and training in the broader area of electronic packaging for immediate and future needs in the industry. I have been a Distinguished Lecturer with EPS since 2019 and my lectures are done online now. As important as it is, advanced packaging is not taught in most institutions of higher learning, unlike courses in micro-fabrication and processes. One of my goals is to work with stakeholders to create awareness and make courses and training in advanced packaging more accessible to the community, especially university students.



CHIH-PIN HUNG (M: 2017, SM 2021)

is a member of IEEE and EPS. He received his Ph.D. degree from the Department of Electrical and Electronic Engineering, University of Paisley (now, University of the West of Scotland), United Kingdom.

Professions

Dr. C.P. Hung currently holds the position of Vice President, Corporate R&D, at ASE Group. Based in Kaohsiung, Taiwan, he leads teams responsible for next-generation product development to be rolled out to various ASE manufacturing sites. Products developed featuring integrated design technologies, as well as a broad range of advanced chip, package, and system integration solutions.

During his about 22 years of ASE tenure, Dr. Hung has experienced a variety of management roles at ASE, including VP of Corporate Design, VP of Central Engineering & Business Development, and VP of Logistic Services Integration.

Society Services

Since 2019, IEEE EPS (Electronics Packaging Society), Board of Governor

Dr. Hung has been the Chair of PKG & TEST Committee, SEMICON Taiwan since 2013. He is currently the Co-Chair of IMPACT since 2013 (EPS sponsored annual conference to be held in October in Taipei, Taiwan).

Dr. Hung was the Co-Chair of the Transducers (one of the three largest MEMS Conferences) in 2017.

He was also a member of ECTC Component & RF Committee during 2013-2015. Dr. Hung was peer reviewer for IEEE Trans. Advanced Packaging published by CPMT (now EPS).

Academic Experiences

Dr. Hung is Visiting Associate Professor in the College of Engineering, National Cheng Kung University. He was also Visiting Assistant Professor of ASE Group Cooperative Advanced Packaging Courses at National Sun-Yat-Sen University, National University of Kaohsiung, National Kaohsiung First University of Science and Technology, National Kaohsiung University of Applied Science.

Publications

Dr. Hung holds 167 patents encompassing IC packaging structure, process, substrate and characterization technology. He has also published over 62 conference and journal papers on the subjects including Design Optimization, Hi-Speed SI / PI, RF, Hi-Frequency Analog, Thermal and Stress for Lead-frame, BGA, Flip-Chip, SiP Module, Fan-Out & 2.5D / 3D IC Packages. These presentations and publications appeared in ECTC, IMAPS, Inter-Pack, IMAPS-VLSI, SEMICON_West, SEMICON_Taiwan, SEMICON_Europe, ICEP, ConFab, EPTC, ICSJ, IMPACT, Transducers, IEEE MEMS, and IEEE Transactions Journals.

Awards

Received "Industry Contribution Award" from the President of Taiwan in SEMICON_TW Gala Dinner, on 2018, 2019 and 2020 respectively

2005 Oct, Dr. Hung received Outstanding Youth Creative Award of 13th Industrial Technology Development Award from the Ministry of Economic, Taiwan.

STATEMENT OF INTEREST

- 1) Joint the EPS's Technology Committee and Conference Committee
- 2) Promote and enable speakers / attendee / publications to EPS related events ECTC, HIR, ICEP, EPTC, ESTC, etc.

Congratulations to New EPS Senior Members

The members listed below were elevated to the grade of Senior Member between June and November 2021.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: <https://www.ieee.org/membership/senior/>

Gary Chen, Central Indiana Section

Mun Kit Chong, Malaysia Section

Chih-Pin Hung, Tainan Section

Rajesh Sur, Winston-Salem Section

Wan-Ming Chen, Taipei Section

Thomas Gneiting, Germany Section

Fengyi Guo, Zhejiang Subsection

Masaki Hashizume, Shikoku Section

Yoichi Hiruta, Tokyo Section

Yasuhiro Murase, Kansai Section

Shuye Zhang, Harbin Section

Asmah Mat Taib, Malaysia Section

Sungwook Moon, Seoul Section

Attila Bonyar, Hungary Section

Andrew Berry, United Kingdom and Ireland Section

Seungbae Park, Binghamton Section

Anu Ramamurthy, Buenaventura Section

Osamu Suzuki, Shin-Etsu Section

Congratulations to the 2022 Newly Elevated IEEE Fellows

Listed below are new IEEE Fellows who are members of the EPS. See a list of all EPS members who are IEEE Fellows in the IEEE Fellows Directory.

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;

- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

***Kemal Aygun** for contributions to high-bandwidth and high-speed packaging and socket technologies.*

***Chuan Seng Tan** for contributions to wafer bonding technology for 3D packaging and integration.*

MEMBERSHIP NEWS

EPS Student Chapter Promotion Programs

To promote the formation and continuation of EPS student chapters, EPS has recently initiated a couple of promotion programs. The Student Chapter Promotion Program (SCPP) is aimed at the formation of new student chapters while the Student Chapter Continuation Program (SCCP) is aimed at helping existing student chapters to remain viable.

Student Chapter Promotion Program (SCPP)

Under the SCPP, six students from any university which has an IEEE student branch who are willing to serve as executive committee (excom) members in a new student branch chapter (SBC) will be given complimentary IEEE+EPS student memberships.

Additionally, faculty members who are willing to serve as Advisors to new SBCs will also be given complimentary IEEE+EPS eMemberships where available, otherwise regular memberships will be provided. The Advisor's duties include advising the excom on student chapter activities, endorsing financial statements where necessary, ensuring that annual election/appointment of new student excom members are held before end December, and that required reports are submitted by the student excom in a timely manner every year.

Student Chapter Continuation Program (SCCP)

Another program, the Student Chapter Continuation Program (SCCP) has also been initiated to facilitate the continuation of existing EPS student chapters. Similar complimentary IEEE+EPS

memberships will be given to six students in a university with an *existing* EPS SBC who are willing to serve as executive committee (excom) members in the student chapter, and to a faculty who agrees to serve as the Advisor to the student chapter.

To qualify for subsidy under the SCCP, the excom and Advisor must ensure that their SBC remains viable for the year. This includes the organization of at least two technical activities per calendar year, formation of new excom for the following year, and timely submission of required activity and financial reports for the year.

An evaluation on the performance of subsidized student excom members and Advisors will be conducted in December each year based on reports submitted. Non-performing students and Advisors

will not be subsidized for another year. While Advisors may be subsidized every year, student excom members may normally be subsidized for up to 2 years, in order to encourage a healthy succession of student leaders in the chapter. However, if the Advisor can report some extenuating circumstances, the subsidy for an excom student can be extended for up to 4 years, subject to the approval of the Student Program Director.

Annual Subsidy for Student Chapters

To support the organisation of technical activities by SBCs, existing SBCs may apply for subsidies of up to US\$1000 per annum from EPS. For new SBCs in their first year, the subsidy can be up to US\$1500.

PUBLICATIONS NEWS

Electronics Packaging Society Section Within IEEE Access

The Electronics Packaging Section within *IEEE Access* will draw on the expert technical community to continue IEEE's commitment to publishing the most highly-cited content. The Journal peer-review process targets a publication period of 6 weeks for most accepted papers. This journal is fully open and compliant with funder mandates, including Plan S.

This is an exciting opportunity for your research to benefit from the high visibility of *IEEE Access*. Your work will also be exposed to 5 million unique monthly users of the IEEE *Xplore*® Digital Library.

Scope

The IEEE Electronics Packaging Society section in *IEEE Access* covers the scientific, engineering, and production aspects of materials, components, modules, hybrids and micro-electronic systems for all electronic applications, which includes technology, selection, modeling/simulation, characterization, assembly, interconnection, packaging, handling, thermal management, reliability, testing/control of the above as applied in design and manufacturing. Examples include optoelectronics and bioelectronic systems packaging, and adaptation for operation in severe/harsh environments. Emphasis is on research, analysis, development, application and manufacturing technology that advance state-of-the-art within this scope.

Get Published in the New Electronics Packaging Society Section of IEEE Access

Go to: <https://mc.manuscriptcentral.com/ieee-access>

Select the Electronics Packaging Society (EPS) Section from the pull-down menu of "Manuscript type" in the first page of the submission process.

Author Information and Instructions

EPS is committed to supporting authors and researchers with IEEE Author Tools including the IEEE Publication Recommender, IEEE Graphics Analyzer, LaTeX Analyzer and more. Discover the tools available at the IEEE Author Center—<https://ieeeauthorcenter.ieee.org/ieee-author-tools/>.

The EPS is regarded as a trusted and unbiased source of technical information for dialog and collaboration to advance technology within the computing community. EPS is led by researchers and technology professionals who are at the center of respected electronics packaging communities where readers and authors already come together.

The articles in this journal are peer reviewed in accordance with the requirements set forth in the IEEE Publication Services and Products Board Operations. Each published article is reviewed by a minimum of two independent reviewers using a single-blind peer review process, where the identities of the reviewers are not known to the authors, but the reviewers know the identities of the authors. Articles will be screened for plagiarism before acceptance.

Article Processing Charge (APC): US\$1,750

IEEE Members receive a 5% discount.

IEEE Society Members receive a 15% discount.

These discounts cannot be combined.

Topical Editors

Ravi Mahajan, Intel Corporation, USA

Dale Becker, IBM Inc., USA

Muhannad Bakir, Georgia Institute of Technology, USA

Koneru Ramakrishna, Cirrus Logic, Inc., USA

Kuo-Ning Chiang, National Tsing Hua University, Taiwan

Most Popular Articles according to Xplore® Usage Statistics

CPU Overclocking: A Performance Assessment of Air, Cold Plates, and Two-Phase Immersion Cooling

Bharath Ramakrishnan; Husam Alissa; Ioannis Manousakis; Robert Lankston; Ricardo Bianchini; Washington Kim; Rich Baca; Pulkit A. Misra; Inigo Goiri; Majid Jalili; Ashish Raniwala; Brijesh Warriar; Mark Monroe; Christian Belady; Mark Shaw; Marcus Fontoura

Publication Year: 2021, Page(s): 1703–1715

A Review of 5G Front-End Systems Package Integration

Atom O. Watanabe; Muhammad Ali; Sk Yeahia Been Sayeed; Rao R. Tummala; Markondeya Raj Pulugurtha

Publication Year: 2021, Page(s): 118–133

Fully Integrated Wireless Elastic Wearable Systems for Health Monitoring Applications

Mohammad H. Behfar; Donato Di Vito; Arttu Korhonen; Dung Nguyen; Belal Mostafa Amin; Timo Kurkela; Markus Tuomikoski; Matti Mäntysalo

Publication Year: 2021, Page(s): 1022–1027

The ICECool Fundamentals Effort on Evaporative Cooling of Microelectronics

Avram Bar-Cohen; Mehdi Asheghi; Timothy J. Chainer; Suresh V. Garimella; Kenneth Goodson; Catherine Gorle; Raphael Mandel; Joseph J. Maurer; Michael Ohadi; James W. Palko; Pritish R. Parida; Yoav Peles; Joel L. Plawsky; Mark D. Schultz; Justin A. Weibel; Yogendra Joshi

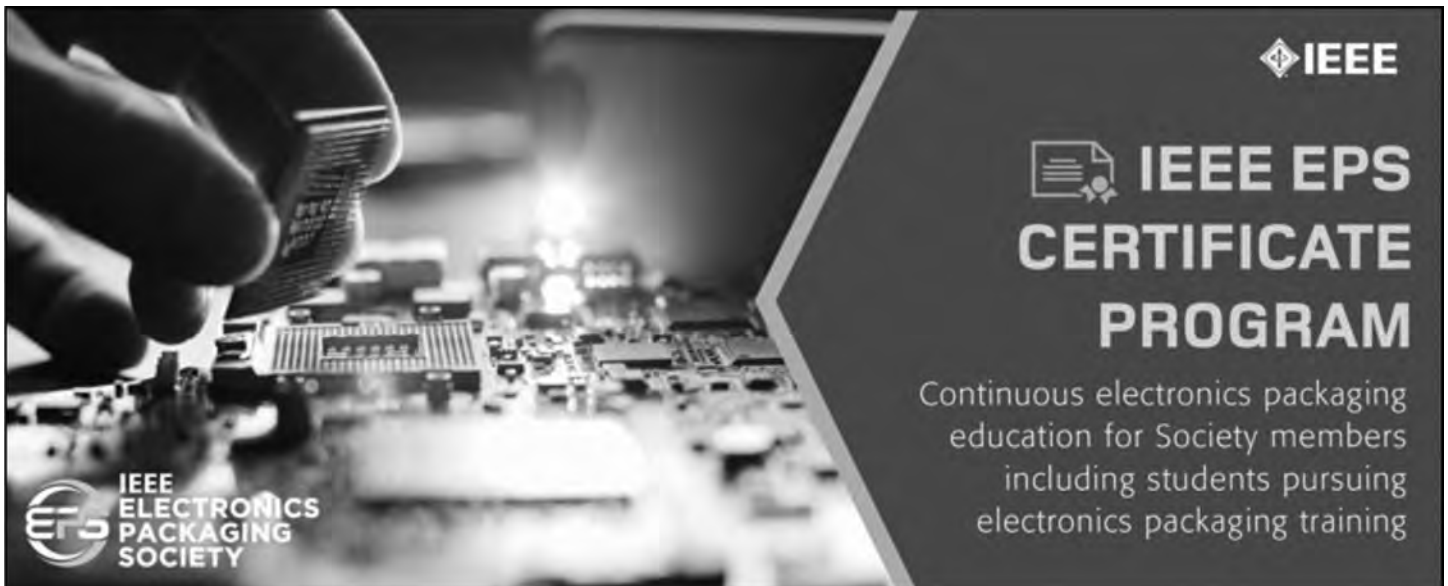
Publication Year: 2021, Page(s): 1546–1564

A Review of Recent Developments in Pumped Two-Phase Cooling Technologies for Electronic Devices

Cong Hiep Hoang; Srikanth Rangarajan; Yaman Manaserh; Mohammad Tradat; Ghazal Mohsenian; Leila Choobineh; Alfonso Ortega; Scott Schiffres; Bahgat Sammakia

Publication Year: 2021, Page(s): 1565–1582

EDUCATION/CAREER NEWS



EPS Certificate Program Expanded

The IEEE Electronics Packaging Society is pleased to announce that it has expanded its Certificate Program to include a new *EPS Distinguished Achievement Certificate*. This new level of recognition builds on the initial *EPS Achievement Certificate* aimed at early-career professionals, and provides a pathway for mid-career to late-career professionals to highlight their more advanced level accomplishments.

Criteria for all Certificates: Must be an IEEE Electronics Packaging Society Member.

The three Certificates you may apply for are below.

EPS Achievement Certificate

The first level *EPS Achievement Certificate* is aimed at early-career professionals working in the field of electronics packaging. It is especially intended to encourage the career development of young professionals including advanced graduate students.

Criteria: Current EPS Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of the following:

- 1) IEEE EPS Webinar (1 PDH)—must complete **PDH evaluation**
- <https://innovationatwork.ieee.org/eps/>



2) Professional Development Courses—must complete survey and CEU credit form. Previous ECTC PDCs from the last 10 years can be used towards this if the CEU application was completed at the time of the course. PDCs from ESTC and EPTC 2018 and forward can be used.

- o Electronic Components and Technology Conference (USA) = 4 PDHs
- o Electronic Systems-Integration Technology Conference (Europe) = 3 PDHs
- o Electronic Packaging Technology Conference (Asia) = 4 PDHs

3) Author of IEEE T-CPMT and/or EPS conference paper(s) (5 PDHs)—paper must be published in IEEE Xplore within the last 5 years.

4) Reviewer for IEEE T-CPMT (3 Reviews = 5 PDH) within the last 5 years.

Once you have completed any combination of the above and received 15 PDHs, please complete the certificate form to request your Electronics Packaging Society Certificate of Achievement.

EPS Distinguished Achievement Certificate for Technical Leadership and Expertise

Criteria: Must be a current EPS member

There are five high-level focus areas for this new certificate. These areas include:

1) Being a recognized authority of technical expertise in one's field

Examples of being a recognized authority of technical expertise include being an advanced member of the technical staff at a company (e.g. Fellow, Senior Technical Staff, Distinguished Engineer, etc.), making technical contributions as a Member or Fellow of professional associations/societies related to electronics packaging (e.g., IEEE, IMAPs, SMTA, ASME, etc.), and being an invited speaker at companies, technical conferences, and EPS Chapter meetings.

2) Being a subject matter expert (SME) at conferences, keynotes, webinars, blogs

Methods to demonstrate participation as a SME include abstracts accepted and papers presented at conferences, giving keynote lec-

tures at conferences or professional society meetings, presenting webinars for EPS and other IEEE Societies, and serving on technical panels at conferences and other venues.

3) Demonstrating sustained technical contributions to industry

Example approaches to demonstrate sustained technical contributions to industry include publishing well-cited technical papers at conferences and in journals, book chapters, and patents; serving as an editor of a journal or reference book; and being a leader or participant in industry blogs, focus groups, technical roadmaps, newsletters, and forums.

4) Documenting advanced technical recognitions

Methods to document technical recognitions include receiving technical awards from a company, institute, professional society, or academic institution; being the acknowledged inventor of a seminal technology or process important to industry; serving as the point person for global high-level task force activity; and being elected to be a Member of an organization such as the US National Academy of Engineering, Royal Academy of Engineering, Chinese Academy of Engineering, IBM Academy of Technology, etc.

5) Being endorsed strongly by others.

Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31

EPS Distinguished Achievement Certificate for Professional Engagement and Service

Criteria: Must be a current EPS member

There are four high-level areas of focus for this new certificate. These areas include:

1) Demonstrating leadership in the electronics packaging field

Leadership and broad impact activities in electronics packaging can be documented from outstanding accomplishments during industry employment or for notable volunteer contributions to the profession and society.

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Examples of significant professional service include serving as an officer in a technical society at the international, national, or local chapter level; participating in packaging related technical



committees, councils, or affinity groups; contributing to technology roadmaps such as the Heterogeneous Integration Roadmap (HIR); and receiving a professional society or industry award based on service contributions.

3) providing extensive service and “give back” to the profession and/or industry; and

Documentation of “give-back” to one’s technical community can be accomplished via demonstrations of coaching and mentoring of co-workers, young professionals, and students.

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More details on the Certificate Program are available on the EPS website at <https://eps.ieee.org/education/eps-certificate-program.html>. The EPS Certificate Program is sponsored by the IEEE EPS VP Education and is offered only to EPS members. For questions, please contact Jeff Suhling (jsuhling@auburn.edu).

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- Overview of the Integrated Photonics Chapter of the Heterogeneous Integration Roadmap
- Overview of the Modeling & Simulation Chapter of the Heterogeneous Integration Roadmap

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President's Column (Continued from page 1)

- Sam Karikalan, VP Conferences
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- Annette Teng, Director of Regions 1-7 & 9
- Tanja Braun, Director of Region 8
- Andrew Tay, Director of Region 10

I want to add a warm welcome to our new and continuing members at Large:

- Regions 1-7 and 9—Xuejun Fan, Subu Iyer, Rozalia Beica, Patrick McCluskey, Mark Poliks, Annette Teng, Jin Yang, Benson Chan, Pradeep Lall and Wolfgang Sauter

- Region 8—Karlheinz Bock, Tanja Braun, and Steffan Kroehnert
- Region 10—Gu-Sung Kim, Yoichi Taira, Chih-Pin Hung, Chuan Seng Tan, and Kishio Yokouchi.
- Yan Liu—Young Professionals
- Marta Rencz—Women in engineering representative.
- Ricky Lee—Fellows Evaluation Chair

Special thanks to the 2021 retiring members for all their hard work, dedication, and contributions to the EPS BoG and the EPS community:

- Eric Perfecto (Awards Director), continuing as Chair of Partnering with IEEE Societies
- Orii Yasumitsu (Region 10 Director), continuing as Chair of Partnering with outside organizations
- Phil Garrou and C. Robert Kao (Members at Large).

CONFERENCE NEWS



ESTC 2022

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The Electronics System-Integration Technology Conference (ESTC) is the premier international event in the field of electronics packaging and system integration. The conference is organized every two years in Europe and is supported by IEEE-EPS in association with IMAPS-Europe. The 9th ESTC will be taking place in Sibiu, Romania. Placed in the middle of Romania, surrounded by the high Carpathian Mountains and Cibin river, Sibiu is a citadel of the European electronics industry and represents a place where culture, landscape, gastronomy and profession merge in a friendly pleasant environment.

The ESTC 2022 seeks original, noncommercial papers describing research and innovations in all areas of electronics packaging and system integration. Authors are invited to submit an abstract describing recent work. Abstracts must detail the objectives of the work presented and demonstrate new results.

Proposed Topics:

- Advanced packaging
- Materials for interconnects and packaging
- Optoelectronic systems packaging
- Assembly and manufacturing technologies
- Design tools and modeling
- Power electronics system packaging
- Advanced technologies for emerging systems
- Reliability and quality of electronic devices and systems
- Flexible, printed and hybrid electronics
- RF, mm-wave and THz systems packaging
- Global education for electronics

The technical program will include oral talks, poster presentations, an exhibition, special sessions and invited keynote talks given by renowned speakers.

Proceedings

Accepted contributions will be published in the conference proceedings, and archived in IEEE Xplore (provided they comply with specifications). ESTC papers can be searched through IEEE, Google scholar and other search engines.

Sponsors and exhibitors welcome!

The ESTC 2022 offers attractive packages for sponsors and exhibitors! Please contact local committee for further details.

Important dates:

Conference:	13 – 16 September 2022
Abstract submission opens:	1 December 2021
Abstract submission deadline:	15 February 2022
Abstract acceptance notification:	31 March 2022
Paper submission deadline:	15 June 2022

Please check the Conference website for details on hotel bookings and travel arrangements.

Venue

Ramada Hotel
Sibiu, Romania

Contact

Local Conference Committee
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Top Conference Papers Based on Usage

2021 IEEE 71st Electronic Components and Technology Conference (ECTC)

(June 1–July 4, 2021)

Wafer Level System Integration of the Fifth Generation CoWoS®-S with High Performance Si Interposer at 2500 mm²

P. K. Huang; C. Y. Lu; W. H. Wei; Christine Chiu; K. C. Ting; Clark Hu; C.H. Tsai; S. Y. Hou; W. C. Chiou; C. T. Wang; Douglas Yu

Die Embedding Challenges for EMIB Advanced Packaging Technology

Gang Duan; Yosuke Kanaoka; Robin McRee; Bai Nie; Rahul Manepalli

SoIS- An Ultra Large Size Integrated Substrate Technology Platform for HPC Applications

Jiun Yi Wu; Chien-Hsun Chen; Chien-Hsun Lee; Chung-Shi Liu; Douglas C. H. Yu

Heterogeneous Integration of a Compact Universal Photonic Engine for Silicon Photonics Applications in HPC

H. Hsia; C.H. Tsai; K.C. Ting; F.W. Kuo; C.C. Lin; C.T. Wang; S.Y. Hou; W.C. Chiou; Douglas C.H. Yu

Info_oS (Integrated Fan-Out on Substrate) Technology for Advanced Chiplet Integration

Y. P. Chiang; S. P. Tai; W.C. Wu; John Yeh; C. T. Wang; Douglas C. H. Yu

2021 20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(June 1–4, 2021)

The effectiveness of heat extraction by the drain metal contact of β -Ga2O3 MOSFETs

Samuel H. Kim; Daniel Shoemaker; Bikramjit Chatterjee; Kelson D. Chabak; Andrew J. Green; Kyle J. Liddy; Gregg H. Jessen; Samuel Graham; Sukwon Choi

Hybrid Electric Aircraft Thermal Management: Now, New Visions and Future Concepts and Formulation

Terry J. Hendricks; Calin Tarau; Rodger W. Dyson

Preliminary study on the boiling heat transfer performance of R-123 refrigerant with nano-porous aluminum oxide membrane

Ji Yong Kim; In Cheol

Package-Level Integration of Liquid Cooling Technology with Microchannel IHS for High Power Cooling

Je-Young Chang; Devdatta Kulkarni; Ravi Mahajan; Michael Jorgensen; Nick Neal; Rich Dischler; Aravind Dasu; Sandeep Ahuja; Rajiv Mongia

Segmented Thermal Management with Flash Cooling for Heterogeneous Wafer-Scale Systems

Ujjash Shah; Subramanian S. Iyer; Timothy S. Fisher

2020 8th Electronic System-Integration Technology Conference (ESTC)

(September 15–18, 2020)

Manufacturing of high frequency substrates as software programmable metasurfaces on PCBs with integrated controller nodes

D. Manassis; M. Seckel; L. Fu; O. Tsilipakos; A. Pitilakis; A. Tasolamprou; K. Kossifos; G. Varnava; C. Liaskos; M. Kafesaki; C. M. Soukoulis; S. Tretyakov; J. Georgiou; A. Ostmann; R. Aschenbrenner; M. Schneider-Ramelow; K-D. Lang

Reliability Testing of FCCSP Packages for Automotive Applications

Karsten Meier; Laura Wambera; Bjoern Boehme; Christian Goetze; Simone Capeccchi; Jens Paul; Marcel Wieland; Karlheinz Bock

Thermal evaluation of metalized ceramic substrates for use in next-generation power modules toward international standardization

Naoki Wakasugi; Chuantong Chen; Kiyoshi Hirao; Shijo Nagao; Katsuaki Suganuma

Cu pillar based Advanced Packaging, for large area & fine pitch heterogeneous devices

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Interconnections of Low-Temperature Solder and Metallizations

YiWun Wang; C. Robert Kao

2020 IEEE 22nd Electronics Packaging Technology Conference (EPTC)

(December 2–4, 2020)

Wafer Level Back to Back Hybrid Bonding for Multiple Wafer Stacking

H. Y. Li; M. Kawano; L. Ji; H. M. Ji; C. S. Lim

Wafer Level Fine-Pitch Hybrid Bonding: Challenges and Remedies

Vivek Chidambaram; Yew Wing Leong; Qin Ren

Lidless and lidded Flip Chip Packages for Advanced Applications

Gamal Refai-Ahmed; Huayan Wang; Suresh Ramalingam; Nagadeven Karunakaran; Ke Pan; SB Park; Alegesen Soundarajan; Sreedharan Kelappen Kanaran; C. Key Chung; Yu Lung Huang

Impact of Process Variations on the Capacitance and Electrical Resistance down to 1.44 μm Hybrid Bonding Interconnects

B. Ayoub; S. Lhostis; S. Moreau; E. Leon Perez; J. Jourdon; P. Lamontagne; E. Deloffre; S. Mermoz; C. de Buttet; V. Balan; C. Euvard; Y. Exbrayat; H. Frémont

An Automatic Chip-Package Co-Design Flow for Multi-core Neuromorphic Computing SiPs

Jingjing Lan; Vishnu P. Nambiar; Rheeshaalaen Sabapathy; Rahul Dutta; Chai Tai Chong; Mihai Dragos Rotaru; Kuang Kuo Lin; Surya Bhattacharya; Kevin Tshun Chuan Chai; Anh Tuan Do

Upcoming Conferences

Dear Members and Patrons of the IEEE Electronics Packaging Society,

With the health and safety of our members and participants being our first priority, please know that our thoughts are with those affected by the COVID-19 outbreak.

We continue to closely monitor the developments related to this pandemic and work diligently with the IEEE and our conference organizing committees worldwide on our preparedness and to make swift decisions, as needed.

The following is the current status of EPS sponsored conferences scheduled so far for 2022, which are all scheduled as in person events as this time.

Conferences sponsored/co-sponsored by the EPS:	
DTMES	Feb 7–9, 2022 Addis Ababa, Ethiopia
SPI	May 22–25, 2022 Siegen, Germany
ITHERM	May 31–June 3, 2022 San Diego, CA
ECTC	May 31–June 3, 2022 San Diego, CA
IWPP	Aug 24–26, 2022 Aalborg, Denmark
EPEPS	Oct 9–12, 2022 San Jose, CA, USA
HOLM	Oct 23–26, 2022 Tampa, FL, USA
ISSE	May 11–15, 2022 Vienna, Austria
ASMC	May 2–5, 2022 Saratoga Springs, NY
EOS/ESD	Sept 18–20, 2022 Reno, NC
EuroSimE	April 25–27, 2022 St. Julian, Malta
IEMT	Oct 19–20, 2022 Kuala Lumpur, Malaysia
ESTC	Sept 13–16, 2022 Sibiu, Romania

3D Integration Technologies for Various Quantum Computing Devices

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INTRODUCTION

With the slowdown of transistor node scaling in the past decade, advanced three-dimensional (3D) integration technologies have been developed as an alternative approach for the continuity of Moore's law, specifically in reducing form factor, cost, power and increasing performance. By extending the conventional two-dimensional layouts, assembly, and interconnections into the third dimension, 3D integration has progressively become the primary building block of advanced electronic devices. Depending on the interconnect hierarchy, 3D integration technologies can be classified into three categories: 3D System-in-Package (SiP, package or system level), 3D System-on-Chip (SoC, device level) and 3D monolithic integration (transistor level) [1].

On the other hand, quantum computing based on quantum mechanisms (i.e., superposition and entanglement) has been intensively investigated in the past two decades, in view of the superior potential in handling certain problems that are intractable for most advanced classical supercomputers. To realize quantum computing, various platforms with distinct physical implementations of quantum bit (qubit) are being developed simultaneously, including trapped ion, superconducting circuit, silicon spin, photon, topological qubits, etc. To date, the number of qubits that are fully connected is ~ 10 in most quantum computing devices. However, in the fault-tolerant quantum computing scheme, it is estimated that millions of physical qubits are required to build sufficient logical qubits (~ 1000) to run the useful quantum algorithms and demonstrate the quantum supremacy [2]. This yields significant challenges in scaling up the current devices to that broad blueprint. One of the possible solutions is to leverage the well-established CMOS fabrication process in semiconductor industry which builds billions of transistors in a fingernail-size chip. At the same time, 3D integration technologies can also be adopted to boost the scalability of qubits by extending to the third dimension either in a hybrid or monolithic manner. Similar to the classical electronics, the 3D integration in quantum devices can be also classified according to its hierarchy.

In the first part of this review, we summarize and classify the state-of-the-art 3D integration technologies that were employed in various quantum computing devices (trapped ion qubit, superconducting circuit qubit, silicon spin qubit, and photon qubit in silicon photonics), which are currently

the most popular candidates due to their favorable manufacturability by leveraging the advanced semiconductor fabrication process. Subsequently in the remaining of this review, the advanced packaging and integration roadmap for ion trap in our group is presented, from substrate material evaluation to the through silicon via (TSV) integration, and finally to the cointegration of TSV, multilayer metallization and silicon photonics into ion trap.

TWO-LEVEL SYSTEM IMPLEMENTATION, GATE OPERATION, AND SCALABILITY BOTTLENECKS FOR DIFFERENT QUBITS

Trapped Ions Qubit

Trapped ions are dynamically confined and isolated from the environment by the RF electric field generated by the electrodes in an ion trap. Lasers with specific wavelengths are focused onto the ions for cooling, manipulation, and detection. The internal electronic states of the valence electron are encoded as qubit. We use optical qubit to illustrate the basic quantum operations. The rotation between states $|0\rangle$ and $|1\rangle$ can be simply performed by focusing a laser beam that resonant at the transition frequency. The shared motional mode in a string of ions can be used as a quantum bus to transfer information. Along with certain single qubit gate rotations, the entangled two qubit gate can thus be performed [3]. Currently, the most-widely used ion trap is surface electrode ion trap, where lithography-defined coplanar electrodes are used in place of the mechanically assembled rod electrodes [4]. Due to the compatibility with microfabrication techniques, surface ion trap with hundreds of electrodes has been demonstrated. However, to realize the actual large-scale ion trapping implementation, numerous challenges remain to be overcome. From the integration point of view, two respective challenges are overcrowding interconnection and on-chip integration of conventionally bulk components (e.g., voltage sources, mirrors, etc.).

With the development of ion trap geometry, certain electrodes located at the geometry center are inevitably surrounded by the peripheral electrodes, which cannot be accessed by bonding wires. Meanwhile, since wire bonds are laterally situated at the edges of a chip in a finite area, the increase of electrodes number will result in the interconnections overcrowding. To mitigate these issues, one needs to explore the third dimension of interconnections. Multilayer metallization (MM) and TSV were independently adopted in place of wire bonding to introduce additional degree of freedom for signal routing [5, 6]. However, both solutions feature some limitations (e.g., thick dielectric layer formation for MM, large diameter and pitch of TSV). Therefore, a combination of TSV and MM is foreseen in future ion trapping devices.

With the increasing number of trapped ions, the optical input and output interface for control and measurement of

individual ions from free-space optics is significantly compressed. Therefore, the integration of optical components becomes essential. At the beginning, bulk optics (e.g., fibers) were mounted into the traps in relatively brute-force approaches. Following that, for light collection, localized components like micromirrors and lenses were integrated and fabricated within ion trap to improve the coupling efficiency [7]. In addition, traps directly fabricated onto high-reflectivity or transparent substrates were also demonstrated [8]. However, these integrations were still limited by the customized fabrication process. Until year 2016, a waveguide and grating coupler integrated ion trap was demonstrated, where a SiN layer as core layer for photonics components is introduced underneath surface electrode and CMOS-compatible fabrication process is used [9]. Besides, it is necessary to highlight that the conventionally bulk passive and active electronic components (e.g., capacitors and digital-to-analog converters) were also on-chip integrated [10, 11].

Superconducting Circuit Qubit

At sufficiently low temperature ($kT \ll \hbar\omega$), the potential of a resonant circuit consists of a capacitor and inductor becomes quantized with a constant energy difference ($\hbar\omega$, harmonic oscillator). By introducing a Josephson Junction into the circuit, the energy difference turns into anharmonic, enabling specific state addressing and thus the encoding of qubit. We use the most popular transmon qubit as an example to demonstrate the quantum operations for superconducting qubit. The single qubit gate is predominately driven by coupling a microwave signal (5-10 GHz) via a coplanar waveguide line. For two qubit gate, two neighboring transmon qubits are normally coupled through a capacitor in between (capacitive coupling). In addition, the qubit transition frequency can be dynamically tuned by incorporating a dc superconducting quantum interference

device (dc SQUID), which is essential for both single and two qubit gates implementation [12]. For superconducting circuit readout, dispersive readout is typically used by coupling the qubit to a transmission line resonator [13]. In summary, all components that are required to define, manipulate and readout superconducting qubits are macroscopic circuits, which can be patterned on the superconducting films with lithography-based techniques. This makes it inherently compatible with advanced CMOS process and thus promising for large-scale realization. However, some challenges are remained.

As differed from large array of classical bits in memory that can be parallel addressed using Word or Bit lines, every single superconducting qubit requires independent circuits designed for control, readout, and qubit-qubit coupling, resulting in huge footprint and interconnection overhead. Meanwhile, most of the circuit layouts are still in a 2D scheme, where interconnections for various signals can only access the qubits via chip perimeters. In the Sycamore processor demonstrated by Google in 2019, a rectangular array of 54 qubits took a surface area of $\sim 10 \times 10 \text{ mm}^2$ [14]. Therefore, to scale up the 2D scheme and maintain the qubit addressability, 3D integration technologies are essential.

Similar to the integration roadmap for ion trap qubit, superconducting multilayers were first introduced. However, the obtained coherence time is generally shorter as compared to the qubits with single layer structure. This is limited by the interlayer coupling as well as the disturbance from natural defects in the interlayer amorphous materials. To mitigate this challenge, a 3D integrated superconducting qubit scheme was proposed in 2017 [15]. This scheme consists of three bonded chips that are individually fabricated. The top chip is the qubit chip which contains qubit circuits, and the bottom chip is for readout and interconnection. To bridge these two chips, an interposer chip that incorporates superconducting TSV is bump-bonded in between. With this

TABLE I
COMPARISON OF VARIOUS QUANTUM COMPUTING DEVICES

Qubit type	Temperature and vacuum	Control signal	Feature size	Pitch between qubits	Challenges to scale up	Commercialization
Ion Trap	Ambient and ultra-high vacuum [^]	Lasers, RF and DC voltage	$\sim 5 \mu\text{m}$ (gap width between electrodes)	$\sim 10 \mu\text{m}$	a. flexible interconnection b. electrode and photonics fabrication c. off-chip light alignment with ions	IonQ, Honeywell
Superconducting circuit	$\sim 10\text{mK}$ and high vacuum [*]	Microwave current, DC current, RF control [#]	$\sim 50 \text{ nm}$ (Josephson Junction)	$\sim 1 \text{ mm}$	a. complex circuit layout b. cryo-electronics c. noise shielding and filtering d. entangle with neighboring qubits only	IBM, Google
Silicon spin	1K and high vacuum [*]	DC magnetic field, AC magnetic field, DC voltages, RF control [#]	$\sim 50 \text{ nm}$ (gate electrode)	10-100 nm	a. multiple quantum dots placement and alignment b. complex electrodes layout c. cryo-electronics d. noise shielding and filtering	Intel
Photons	Ambient and atmosphere	Lasers, DC voltage, RF control [#]	200 nm (waveguide)	$\sim 200 \mu\text{m}$	a. high efficiency single photon source and detector b. the integration and alignment with waveguide circuit	PsiQuantum, Xanadu

[^]Cryogenic apparatus in ion trapping test also benefits for anomalous heating reduction; ^{*} The high vacuum (down to 0.1 mbar) is required by the dilution refrigerator; [#]RF control is required for the pulsed operations within qubit lifetime. Table used with permission from [24].

scheme, the capability for complex interconnection routing is maintained in the bottom chip, while the qubit performance in the top chip will not be degraded.

Silicon Spin Qubit

Silicon spin qubits are encoded on the spin of electrons, that either bound to the embedded dopants or quantum dots (MOS and SiGe material systems are commonly used to define quantum dots). We use the simplest spin qubit defined by single electron as an example to demonstrate the quantum operations for silicon spin qubit. An in-plane large static magnetic field is required to create the Zeeman splitting. The single qubit gate is achieved using electron spin resonance (ESR) technique, in which an AC current is sent into a transmission line close to the qubit and thus generate a localized AC magnetic field resonant with spin transition frequency. The two qubit gate is implemented via the exchange interaction. For the qubit readout, a process known as spin-to-charge conversion is used, where the qubit electron is coupled to a single electron transistor (SET), and under specific conditions spin-up electron will tunnel to the electron reservoir and produce a detectable current pulse. We note that all these basic operations are controlled and enabled by appropriate voltages tuning on the corresponding gate electrodes located on top of qubits [16].

In terms of the compatibility with CMOS process, a silicon spin qubit geometry derived from the field effect transistor (compact two gate FET) was developed in 2016, where two top gates were respectively used to control two quantum dots that defined in the silicon channel (one qubit dot and one sensing dot in series). This work started from the standard CMOS process in transistor fabrication and adapted it to achieve the quantum functionality [17]. Similar to the superconducting circuit qubits, even in a huge array of millions of qubits, the independent control from multiple gate electrodes is anticipated to be indispensable for every single silicon spin qubit, posing significant challenges to the qubit architecture itself as well as the quantum-classical interface. To mitigate the first challenge, a 3D architecture was proposed in the qubit level, where the sensing dot was repositioned to the layer underneath the qubit dot and a tunnel barrier was introduced in between to transmit electron [18]. In terms of the interface overcrowding, a conceptual 3D integration architecture was also proposed for future quantum computer processor where the bottom layer and top layer of a silicon-on-insulator wafer were respectively used to accommodate qubits array and classical transistors for control [19].

Photon Qubit in Silicon Photonics

Photons are appealing to be used as qubits since they are almost free of decoherence. With that, the stringent environmental conditions (e.g., millikelvin temperature and ultra-high vacuum) as required by other qubit candidates can be eliminated, enabling photon qubits with high scalability. Besides, with the development of silicon photonics, photons can be routed by waveguides on a microfabricated chip,

making the scale-up even more feasible. Though the single qubit rotation can be straightforwardly performed using waveplates and beam splitters, the two-qubit gate (i.e., Controlled NOT gate) implementation for photons become significantly more complex due to the large resource overhead required by the linear optics. Different from the abovementioned qubit candidates that have demonstrated single and two qubit gates but lack scalability, photon in waveguide circuits is naturally scalable thanks to the silicon photonics advancement. However, the challenge is to make it quantum, or more particularly, to achieve the entangled logic gate efficiently, which requires further theoretical and experimental innovations. Currently, one of the key requirements is to develop high efficiency single photon sources and single photon detectors, which are integratable to the sophisticated photonics circuit [20].

In 2016, a pick-and-place technique was developed for the integration of quantum dots single-photon source into ion trap. This technique allows for the precise alignment and high coupling efficiency between quantum dots and waveguide circuits [21]. Similarly, in 2015, a micrometer-scale flip chip method was demonstrated to transfer ten superconducting nanowire single photon detectors (SNSPDs) onto the same photonic circuits [22]. Based on separate fabrication and individual pre-selection of SNSPDs and photonic circuits, a 100% device yield was achieved. In addition to those single photon sources and detectors that integrated into the photonic circuits in an out-of-plane approach, novel 3D waveguide circuits can be built using the femtosecond laser direct-write technique by focusing the laser beams at different depth in the substrate [23].

We use Table I to compare and summarize the scalability requirements and bottlenecks of the abovementioned four qubit candidates. The current solutions using 3D integration technologies are classified based on the integration

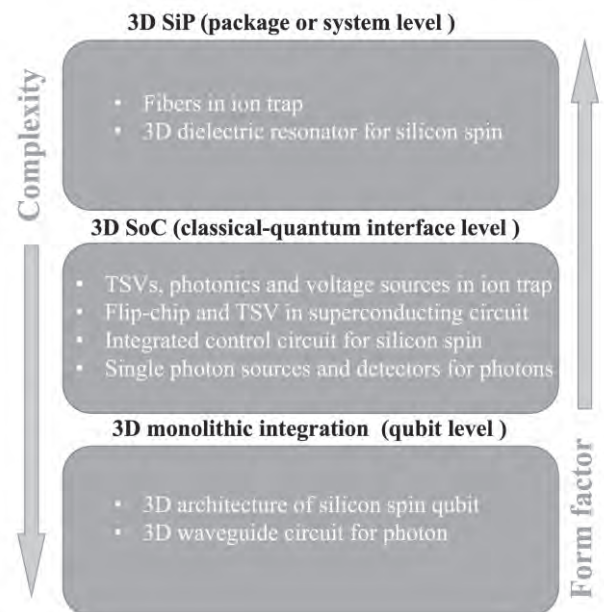


Fig. 1. The hierarchy of 3D integration technologies used in various quantum computing devices. Panel used with permission from [24].

hierarchy, as shown in Fig. 1. A more detailed description is given in [24].

3D HETEROGENEOUS INTEGRATION ROADMAP FOR ION TRAP

Substrate Material Evaluation

In our group, the integration roadmap of surface electrode ion trap starts from the material selection for the ion trap substrate (Fig. 2 (a-c)). The key requirements are low RF loss and high manufacturability. Silicon is always in the shortlist due to the CMOS compatible fabrication process. However, to mitigate the lossy issue of silicon, two possible solutions are proposed: the use of high resistivity silicon ($>750 \Omega \cdot \text{m}$) and the incorporation of grounding plane. Meanwhile, due to the development of glass fabrication technology in commercial foundries, glass has become a popular substrate especially for high frequency devices. Therefore, ion trap on glass substrate is also investigated. The electrical performances of traps on different substrates are compared in terms of leakage current, parasitic capacitance, on-chip RF loss and post-packaging resonance [25]. Ion trap on glass substrate demonstrates smaller capacitance ($<1 \text{ pF}$) and lower RF loss (insertion loss of $<0.05 \text{ dB}$ at RF frequency of 50 MHz), as compared to the silicon counterparts. The ion trapping test on the glass trap is performed and up to four $^{88}\text{Sr}^+$ ions are successfully confined [26]. For single ion, the averaged lifetime is ~ 30 minutes.

TSV Integration

To simultaneously leverage the established fabrication technique of silicon and superior insulation property of glass,

we further demonstrate a novel ion trap design with heterogeneous integration of silicon and glass, acting respectively as ion trap and interposer substrate [6, 27]. The vertical connection between the silicon ion trap and the glass interposer is achieved by TSV (Fig. 2 (d, e)). We highlight all the fabrications of various traps are performed with the standard CMOS back end of line process on 12-inch wafer fabrication platform. Due to the integration of TSV, the original wire bonding pads on trap surface are eliminated. Consequently, the form factor of TSV integrated ion trap is reduced by more than 80%, minimizing the parasitic capacitance from $\sim 30 \text{ pF}$ to $\sim 3 \text{ pF}$. Meanwhile, excellent ultra-high vacuum (10^{-11} mbar) compatibility of the packaged ensemble (trap, interposer and micro-bumps) is observed. In ion trapping test, the obtained heating rate (17 quanta/ms for an axial frequency of 300 kHz) and lifetime (~ 30 minutes) of TSV trap are comparable with traps of similar dimensions, indicating no additional decoherence source is introduced by the TSV integration.

Multi-module Integration

To move forward, the integration of other functional modules (silicon photonics and multilayer metallization) into TSV trap is proposed and the fabrication is ongoing. In silicon photonics module (Fig. 2(f)), waveguide and grating coupler are on-chip introduced in place of bulk optics to achieve localized light routing and emission [28]. Two different grating coupler designs which are correspondingly used for wavelengths of $1,092 \text{ nm}$ ($^{88}\text{Sr}^+$ ion, repumping) and 422 nm (cooling and readout) are included. Based on the FDTD simulation result, the beam size of the light emitted from

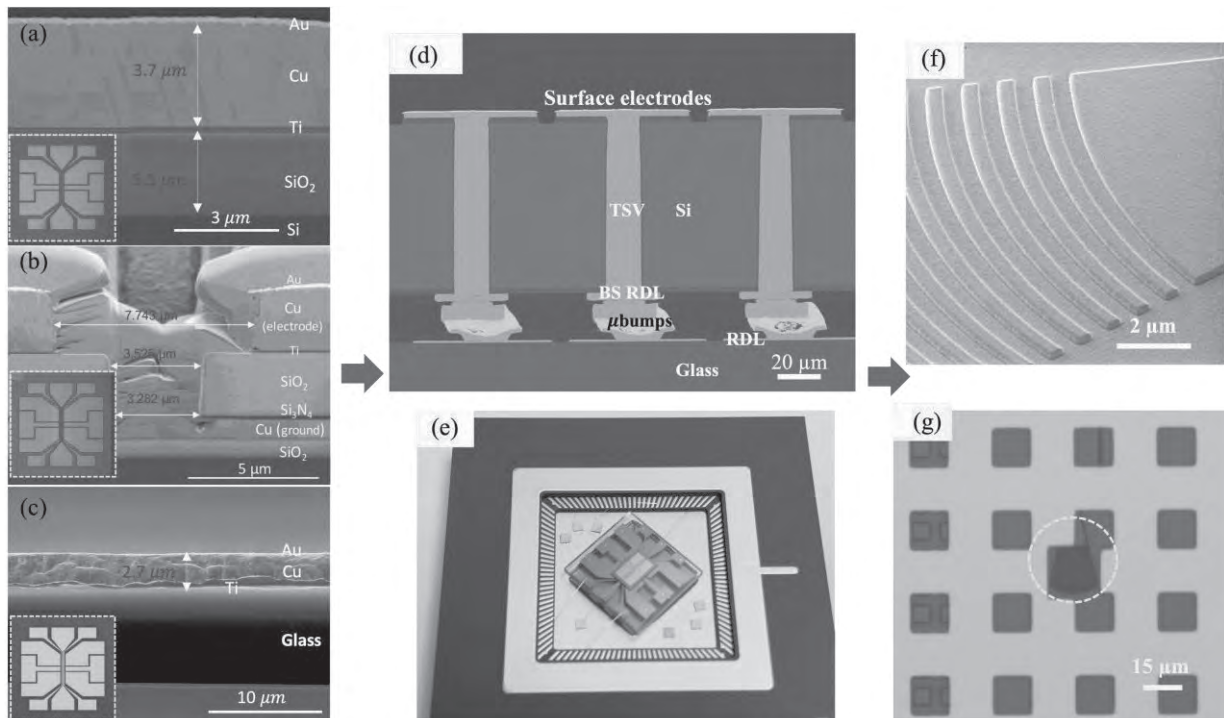


Fig. 2. (a-c) Cross-sectional SEM images of trap on HR silicon, trap on silicon with grounding plane and trap on glass. The insets are top-view optical images of corresponding traps. (d) Cross-sectional SEM image of TSV integrated ion trap chip on a glass interposer. (e) Assembled TSV trap in a CPGA. (f) Grating coupler designed for light of 1092 nm wavelength, which is located underneath grounding plane and surface electrode. (g) Grounding plane with specific windows on top of output grating coupler allowing light transmission. Panels used with respective permission from [25] for (a-c), [6] for (d), [27] for (e).

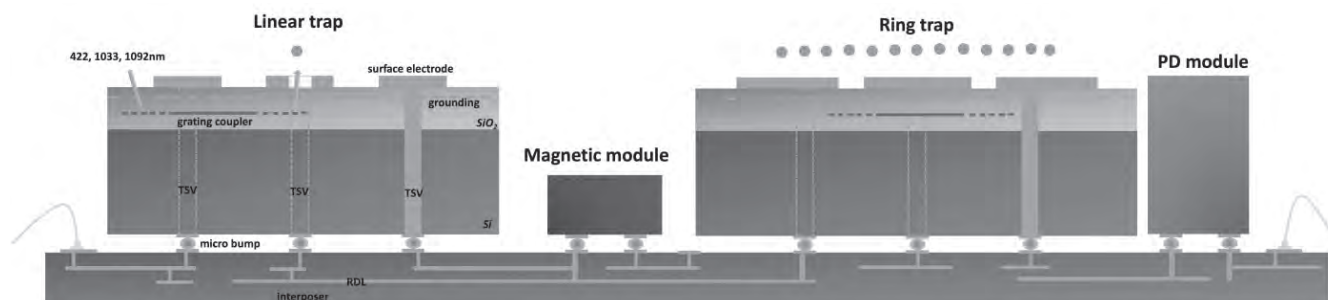


Fig. 3. Large-scale ion trap based quantum computing platform where multi-module integrated ion traps and other functional modules are co-located onto the same interposer in a reconfigurable approach.

output grating coupler is $\sim 10 \times 15 \mu\text{m}^2$ at the nominated ion trapping height, which is compatible with inter-ion distance. In multilayer metallization module, as a first step, a grounding plane is incorporated into TSV trap to shield the silicon substrate from RF signal, in which specific windows are patterned onto the plane to accommodate TSV and allow the transmission of lights (Fig. 2 (g)) [29]. The power loss of TSV trap is further reduced due to the incorporation of grounding plane, maintaining the temperature increase of new trap $< 1 \text{ K}$ (from finite element modelling). This paves the way for the normal operation of temperature-sensitive silicon photonics. The preliminary electrical testing results on the wafer frontside (before wafer thinning and backside processing) show that the capacitance and insertion loss of new trap are further reduced as compared to the TSV trap.

Based on the multi-module integrated ion trap, a large-scale ion trapping platform is proposed, as illustrated in Fig. 3. Different functional modules are co-located on the interposer and interconnected by the RDL in a reconfigurable approach. Linear trap is used for logic operation, whereas ring trap can be used as quantum ‘memory’ due to the superior capability to storage large number of ions.

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Maximizing Benefits of Adaptive Test Techniques by Integration of ML and Test Infrastructure Improvements

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Abstract:

Testing Si devices in high volume manufacturing (HVM) is getting more challenging and expensive, owing to the increasing complexity of the devices under test. Semiconductor companies are adding more capabilities on a package, transistor density is going up, end user applications are more varied than ever before.

Adaptive test techniques have been used in industry for many years now. Applications of machine learning (ML) techniques have also been demonstrated and widely used in test today. This has opened opportunities to really push the envelope in terms of improving outgoing quality and while at the same time reducing production test costs. To take advantage of what ML has to offer, a key is to make sure our test infrastructure such as test hardware, software has a tight integration with ML techniques, so we can take advantage of both, test infrastructure optimizations and progress in ML techniques to deliver the best result for the business. When designing our ML algorithms, we must think not only of its accuracy, efficiency etc., but also pay attention to systems where it will run and optimize them to be best in class. Similarly, when designing our test hardware and software for manufacturing, we must look at the entire stack: automation systems that handle manufacturing routes, to testers, handlers, to operating systems that run on testers and make sure they are optimized to consume the output of ML algorithms and can move the units accordingly, to give the best throughput. Finally, the test engineers must also think about what test data they generate, what format is it in, how is it stored and is it optimized for absorption by ML applications so that they can take advantage of the data without human interaction.

This article will discuss how test world is ideally suited to apply ML techniques, what possibilities exist for improving our test techniques and test manufacturing (MFG) flows and therefore opportunities for future development.

1. Introduction:

Today, machine learning (ML) and artificial intelligence (AI) are the buzz words, we see many applications of these in almost

every field, from faster and more optimized web search engines, to predicting users' shopping preferences, movie preferences to predicting outcomes of elections to medical field for diagnosis etc. and many more. In many of these applications, human behaviors and choices that are inherently unpredictable (example: what movie do I want to watch next) do impact the outcomes. Field of Si testing on the other hand, varies significantly. The Si devices that we see in our everyday lives, like the ones in our laptops, start with a design. It is then fabricated using a specific fabrication technology (or node) and after that, it goes through stress steps to weed out early life failures. After these 3 steps, the Si device characteristics, for the most part, are set – it doesn't have mind of its own to start acting differently for the same input stimuli (Figure 1). This makes application of ML to predict the behavior of these parts during TEST the most apt use of ML and AI, provided we have the right data (input features) and have the right infrastructure in test environment to take advantage of power of ML.

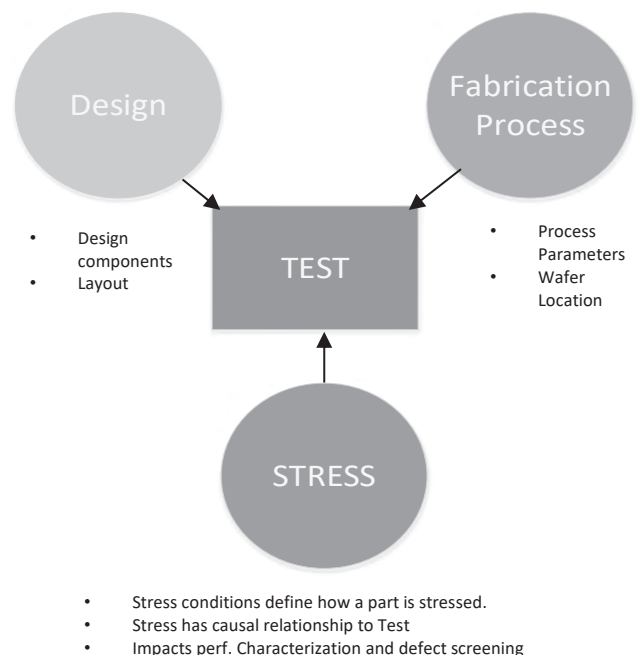


Figure 1: Factors that impact TEST.

In HVM, test engineers have access to data from every step of test manufacturing process, like wafer sort, class test, system test etc. These large volumes of data sets can be used to solve improvement challenges along many different vectors such as yield, quality, performance, or test time improvements using ML techniques that are ubiquitously available (eg: xgboost, random forest etc.) in various ML packages today. These techniques can be used to show, using data analysis offline, what we can gain in any of the vectors listed above. For example, we can do an offline analysis of input features we have to show what test plans are not needed for specific units, or which types of units are most likely to fail in our manufacturing flows. Whether we can take advantage of these techniques to improve our manufacturing, really comes down to the test infrastructure in place and do we have ML integrated within our manufacturing flows at every level, from lot movement to test selection for device under test (DUT) while it is socketed on a test equipment.

It is therefore important that to deliver the most cost-effective test solution, we should be paying close attention to generating the right type of data, the format of how it is stored and investing in making manufacturing systems that can take advantage of immense value ML solutions can provide.

2. Architecting test manufacturing to leverage adaptive test techniques

Use of adaptive test techniques in test manufacturing is quite prevalent in industry and has been documented extensively in conference and journal papers. What we will discuss here is how to architect the manufacturing flows to leverage the best out of ML towards delivering the most cost effective and quality conscious output to our businesses.

A typical manufacturing flow for backend test consists of many steps as shown below in Figure 2.

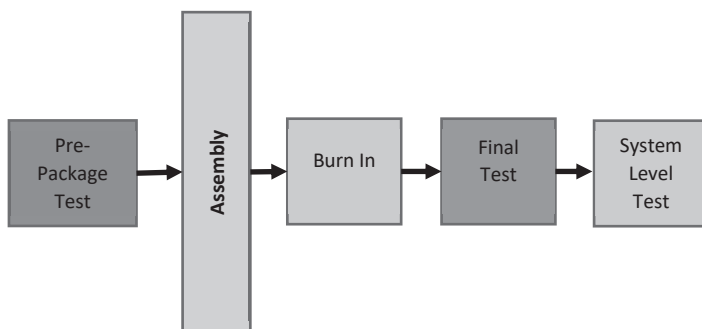


Figure 2: High level backend TEST MFG flow.

ML techniques can enhance the decisions on how we adapt our test plans to different units. For example: once we are done testing all die pre-assembly, we can use the pre-assembly data to grade the die along any number of vectors that are critical to

specific business end use; for example: yield, speed, power etc. This grading system can then be used to select the best combination of die that should go on a package. Such a scheme will be particularly useful as we enter the world of chips coming from different vendors, all going on a single package to make the final device.

The other aspect is optimizing our test flows using ML. All the die that are printed on a wafer need not be tested the same way. As mentioned in previous paragraphs, we can learn from our data and with use of ML techniques, start creating the most optimized test flow for each die. Doing this analysis offline is great, but how can we deliver that to be effective in extracting business values as measured by test time, yields, run rate, outgoing quality? To do this, we must architect the entire manufacturing system in such a way that we have different adaptive test levers: all the way from updating test lot's route based on ML predictions to all the way down to the most granular level of selecting which test patterns run on which units in which socket(s). Such a system gives us the most control over unit movement and content delivery. Such a system also requires that our test hardware and software systems be able to house our ML engines in the flow and able to interact with it – giving it data and taking directions from it. To do this, all manufacturing systems: from those that control lot movement to the operating systems that run on testers, need to have some basic requirements: like ability to run industry standard ML packages, a handshake protocol with data bases on querying for information and writing to them.

3. Sources of data to consider for optimizing key MFG indicators

Key manufacturing performance indicators (KPIs) that have significant business impact are typically outgoing quality, yields, performance bucketing, test time in each socket, overall throughput, or cycle time of test factories. When we think about designing adaptive test MFG flows with ML to optimize these indicators, we as test engineers have to think about the sources of data that we can use towards this, what are ingredients of a complete data, what format should we be writing it in and what type of tests should we be writing to help us along the way. This last topic we will discuss in next section.

As far as sources of data goes, in general, we want to tap into as many sources that will assist us in making quality ML models towards improving our KPIs. This will include fabrication process data, design rule data, test data as the die/unit makes its way through manufacturing flow and data from test equipments' used that give us information about the tool health. Here, we will specifically focus on test data.

In a very simplistic form, test data consists of name of the test that is being performed on the DUT and its output, with the output giving us information about what happened during the test. We can also include more granular pieces of information

to know details on exact events that happened during the test. For any given test, the actual syntax of what is written as test output will depend on how the test engineer wishes to see the results, tester operating system, how the output is connected to the data bases that store the data. In such a system, you need the test engineer to interpret the data for you. See left hand side, Figure 3. As we start working on products where we expect to get different chips from different vendors, such a system will not scale.

Test Name1, Test Name1 Result	Test Name1, Test Name1 Result, FormatSyntax, Context
1 Old format of storing test data.	1 New format of storing test data.
2 No information provided on how to decode (no syntax).	2 Syntax provides information regarding how to decode the test result.
3 If conditions that generate this result change, the end application consuming it is none the wiser.	3 If conditions that generate this result change, it will be reflected in context, making the end application consuming it adjust its decision.

Figure 3: Example of context aware test data (on right).

We need the output of our testing to have enough information so that it is consumable by other applications, like a ML engine, without the aid of the test engineer. To do this, the test data should have 3 components: test result + its context + test result format syntax (aka instructions on how to consume it). This is shown in right hand side of Figure 3. Here, test result is the raw result that comes out of running the test. Context will have the information of what were the conditions that defined the test instances (voltage, frequency, temperature, any other parameter that influences the output of the test). The third part, written here as test result format syntax, is a set of instructions on how to consume a given test result. One test engineer might for example write 40 different values indicating a specific measurement on each of the sub IPs. The instructions will give that information to end user.

The significance of the two fields here, outside of actual raw test result is quite enormous. It allows for a machine-readable format, with rules on how to understand it without having to sit down with a test engineer. But more importantly, by adding context to the data we generate, we make sure the ML models get applied only when the test results are generated with the right context. Any change in context will be identified and our output will adjust to the new context. This is an area where we need to have industry standard tools, although adoption of such tools will not be easy.

4. Prediction Measurements (PM):

Each test socket may potentially generate vast amounts of data. We tend to use what is generated and apply machine learning techniques to see if we can extract value towards improving one or more of our key indicators. However, a more deliberate approach would be to insert observations (tests) during our manufacturing flow that are not necessarily geared towards testing the device to its spec, but more towards giving us more information about the performance of individual electrical devices, like transistors, diodes, circuits etc. that can help us predict the performance of the complex logic or application blocks they are part of in the final CPU or chip. This is what we call prediction measurements or PMs. As an example: we know that the analog measurements that come from basic structures like a PLL or a digital sensor or an oscillator tend to be a good predictor of performance of the digital logic tests. We know today as industry is chasing higher and higher interface speeds with say PCIE etc., it is becoming harder and more expensive to test these IPs as part of our test flows. Can we then add specific readouts in our test flows that can be used to predict say speed performance of these IPs? Can we extend that logic to also create data sources that can predict our system performance for not only these IPs, but any other feature in general? We need more research done in this area from both industry and academia.

5. A glimpse of future:

This article will not be complete without thinking about what we as a test community should strive to do. As mentioned throughout this article, test is the most apt field for applications of ML. How much we can leverage will really come down to: are we writing the right types of tests, are we storing the right types of data and its context and in right formats, are we designing our manufacturing test infrastructure that makes it easy for ML engines to be tightly integrated within our test flows so we can control the movement of the units and content delivery. After we make all of this happen, we still need the ability to create ML models that are going to give us the right solutions towards optimizing our KPIs. Towards this, we must invest in developing systems that will make the domain experts in test state the constraints of the problem they want the ML solution to optimize against, specify the data sets and out comes the model. This is what happens typically when a test engineer sits down with a data scientist and for pushing the envelope of ML applications, we still absolutely need this interaction, no doubt about that. However, for many day-to-day use cases, we can empower the test engineers, who are domain experts in test, but may not have requisite training in the art of machine learning. This, sometimes, can create a barrier to openly embracing and applying ML techniques to problems at hand. Creating ML as a service (MLAAS), that can be called by anyone, anywhere and that can be given problem constraints and data sets, to create an output, is where there is scope for

industry and academia research. Again, adopting these techniques across industry can be a challenge, but this will create a host of ideas and solutions that will push this subject matter forward.

Finally, with the aid of ML and test infrastructure innovations, our goal is to build a self-monitoring, self-correcting MFG

flow, where our ML engines can monitor the data generated within the systems and react to that data real time, and our test infrastructure solutions can take the signals from our ML engine and correct our flows where necessary towards the most optimized KPIs that our businesses ask for.

Verifying Results of Quantum Circuit Compilation Flows

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Quantum computers aim to change the way we tackle certain problems in the future. Numerous quantum computing applications with a near-term perspective (e.g., for finance, chemistry, machine learning, optimization) and with a long-term perspective (i.e., cryptography, database search) are currently investigated. However, in order to realize those, a multitude of (computationally complex) design tasks have to be conducted—eventually forming a process called *quantum circuit compilation*. This results in descriptions of quantum algorithms at various abstraction levels which may significantly differ in their basis operations and structure. This is similar to the classical realm where, e.g., descriptions at the *Electronic System Level*, the *Register Transfer Level*, and the *Gate Level* exist. All this substantially changes the circuit description during the design flow. At the same time, all these steps should obviously preserve the originally intended functionality of the quantum circuit. In order to verify whether two quantum circuits indeed realize the same functionality, *equivalence checking* is usually conducted. In this brief summary paper, we provide an overview on how equivalence checking can be conducted for quantum circuits and, by this, how the results of corresponding compilation flows can be verified.

QUANTUM CIRCUIT COMPILATION

In the first part of this summary paper, we review the compilation flow as it got established in the recent years. Initially, quantum algorithms (often provided in terms of a *quantum circuit*) are described in a way which is agnostic of the device they are planned to be executed on. Similar to the conventional realm, where a compiler transforms high-level code into (machine-executable) assembly, a conceptual quantum algorithm needs to be *compiled* to a representation that conforms to all the restrictions imposed by the targeted device. This is commonly done in three steps:

- 1) *Synthesis*: Quantum computers built today typically only feature a limited (but universal) set of supported operations (called gates). Usually, this gate set consists of arbitrary single-qubit gates and a certain two-qubit gate (such as the CNOT). Thus, the gates of the original quantum circuit first have to be *synthesized* to the gate-set supported by the targeted device. Most importantly, since devices typically only support up to two-qubit gates, any gate acting on more than two qubits has to be decomposed into “elementary” gates.
- 2) *Mapping*: After the first step, the circuit just contains elementary gates supported by the device. However, current quantum computers (at least those based on superconducting qubits) only feature a rather limited connectivity between their physical qubits—only allowing two-qubit gates to be applied to certain pairs of qubits. Thus, the quantum circuit has to be *mapped* to the target architecture so that a mapping between the circuit’s *logical* and the device’s *physical* qubits is established which satisfies all connectivity constraints. In most cases, it is not possible to define such a mapping which conforms to *all* connectivity limitations globally. In these cases, the logical-to-physical qubit mapping is changed dynamically throughout the circuit by adding so-called *SWAP* gates into the circuit—effectively allowing to change the mapping of logical qubits to physical qubits so that all operations can be executed while, at the same time, all connectivity constraints are satisfied.
- 3) *Optimization*: After the previous step, circuits are ready to be executed on the targeted devices. However, the previous steps significantly increased the size of these circuits. Since today’s physical qubits are inherently affected by noise—leading to rather short coherence times and limited fidelity of the individual operations—and error correction is not yet an option, this severely impacts the achievable performance. Thus, several *optimizations* may be employed to reduce the circuit’s size and, hence, improve the actual performance on the quantum computer.

Example 1. An example of a quantum circuit G with 16 gates acting on three qubits is shown in Fig. 1a. This sequence of operations describes a small instance of the famous Grover search algorithm [1]. The small boxes with identifiers correspond to operations applied to single qubits such as X and H gates. Moreover, there are multiple-controlled X operations, where an X operation is only applied to a target qubit (denoted by \oplus) if all of its control qubits (denoted by \bullet) are in state $|1\rangle$. An exemplary device architecture (that of the IBMQ London quantum computer) is shown in Fig. 1c. It consists of five (physical) qubits and supports arbitrary single-qubit gates, while a CNOT operation may only be applied to connected qubits. If G shall be executed on this system, the Toffoli gate (the two-controlled NOT) first has to be realized using only the supported elementary gates. One possible synthesized version is shown in Fig. 1b. Mapping the resulting circuit to the architecture might result in a circuit \tilde{G} as shown in Fig. 1d—using only a single SWAP operation. Applying several optimizations to \tilde{G} allows to further eliminate nine single-qubit gates and results in the optimized circuit G' shown in Fig. 1e.

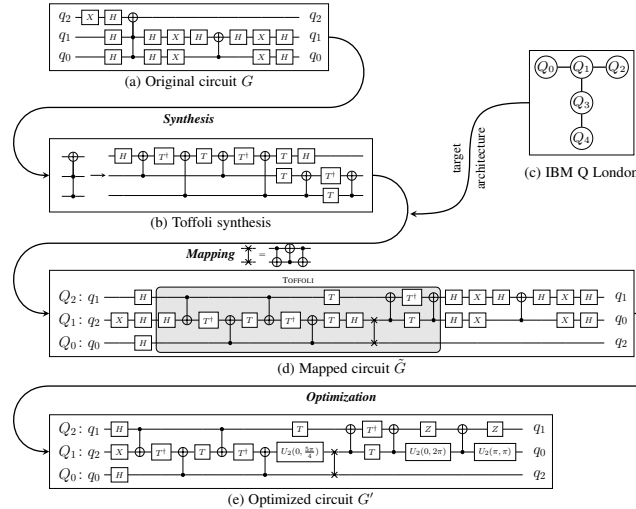


Figure 1: Exemplary illustration of the IBM Qiskit compilation flow

VERIFICATION OF QUANTUM CIRCUITS

Naturally, it is of utmost importance that the results of such compilation flows are correct, i.e., that the compiled quantum circuit still realizes the originally intended functionality. This motivates the development of methods for *verification* or, more precisely, *equivalence checking* of quantum circuits.

Checking the equivalence between two quantum circuits boils down to checking whether they indeed realize the same functionality. Mathematically, the quantum gates g_i of an n -qubit quantum circuit G are defined by $2^n \times 2^n$ unitary matrices U_i . Consequently, the functionality of a quantum circuit G with gates g_0, \dots, g_{m-1} is described by a unitary matrix U , which is obtained by consecutively multiplying the unitary matrix representations U_i of each gate g_i in reverse order, i.e., $U = U_{m-1} \cdots U_0$. Thus, checking the equivalence of two circuits G and G' amounts to building and comparing the circuits' system matrices U and U' . While conceptually simple, the exponential size of the involved matrices quickly renders many direct approaches infeasible. In fact, equivalence checking of quantum circuits has even been proven to be QMA-complete in the general case [2].

In the recent past, some methods addressing this problem have been proposed [3]–[8]. In the following, we review approaches (and a resulting verification flow) introduced in [3] which rests on the following observations:

- Quantum circuits are inherently reversible. Because of that, if two quantum circuits G and G' are equivalent, then concatenating the first circuit G with the inverse G'^{-1} of the second circuit would realize the identity function \mathbb{I} , i.e., $G \cdot G'^{-1} = \mathbb{I}$. Hence, checking whether G and G' are in fact equivalent can be conducted by starting with the identity and, then, applying operations of G and (inverted) operations of G' in a particular order until all operations have been applied (written as $G \rightarrow \mathbb{I} \leftarrow G'$). Whenever the final result again resembles the identity, the circuits are considered equivalent. If all the operations can be applied so that the respective intermediate computations remain as close to the identity as possible, substantial improvements can be achieved since the identity constitutes the best case for most representations of quantum functionality (e.g., linear in the number of qubits for decision diagrams). However, how to determine the “perfect” order of applications in order to keep the respective intermediate representation close to the identity, remains a notoriously difficult task. It has been shown in [9], that utilizing knowledge about the compilation flow allows to design a strategy which keeps the respectively occurring intermediate representations close to the identity in an almost perfect fashion. By this, the exponential complexity is frequently reduced to a linear or close-to-linear complexity—substantially reducing the runtime for verifying the results of compilation flows.

- Moreover, even in the case where the two considered quantum circuits are not equivalent, quantum characteristics can be exploited. In fact, due to the inherent reversibility of quantum operations, even small differences in quantum circuits frequently affect the *entire* functional representation. Hence, it may not always be necessary to check the complete functionality, but it is highly likely that the simulation of both computations with a couple of arbitrary input states (i.e., considering only a small part of the whole functionality) will already provide a counterexample showing the non-equivalence. This is in stark contrast to the classical realm, where the inevitable information loss introduced by many logic gates and the resulting masking effects often require a complete consideration of *all* possible input states or sophisticated schemes for constraint-based stimuli generation, fuzzing, etc. In [10], several different (random) stimuli generation schemes have been proposed that offer a trade-off between error-detection rate and efficiency.

These observations complement each other in many different ways. Trying to keep $G \rightarrow \mathbb{I} \leftarrow G'$ close to the identity proves very efficient in case two circuits are indeed equivalent—provided a “good” strategy can be employed. Conducting simulations with appropriately-chosen stimuli on the other hand allows to quickly detect non-equivalence even in cases where both circuits only differ slightly. Combining both ideas naturally leads to an equivalence checking flow as illustrated in Fig. 2.

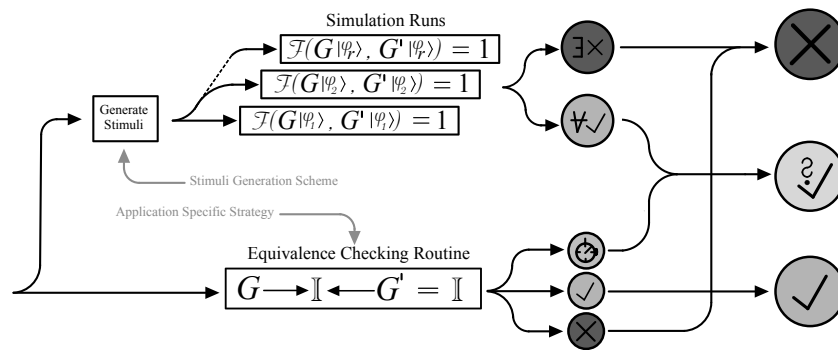


Figure 2: Equivalence checking flow

Here, a limited number of $r \ll 2^n$ simulation runs with stimuli chosen according to some generation scheme (e.g., random computational basis states) is started in parallel with the $G \rightarrow \mathbb{I} \leftarrow G'$ equivalence checking routine according to some strategy (e.g., a strategy tailored towards verifying compilation flow results). Should any of these simulations (with stimulus $|\varphi_i\rangle$) yield different outputs in both circuits (i.e., a fidelity $\mathcal{F}(G|\varphi_i\rangle, G'|\varphi_i\rangle) \neq 1$) or should the equivalence checking routine be able to determine a final result not resembling the identity, the non-equivalence of the circuits under consideration has been shown and all other executions can be aborted. On the other hand, the equivalence checking routine either manages to establish whether both circuits are equivalent or, in case it times out, leaves an indication (although no proof) that the circuits are likely to be equivalent, due to the fact that even small errors frequently effect the entire functionality.

QCEC - A TOOL FOR QUANTUM CIRCUIT EQUIVALENCE CHECKING

The methodology for verifying the results of quantum circuit compilation flows described above is available as an open-source software package called *QCEC* (available at <https://github.com/iic-jku/qcec>). It is mainly developed in C++, runs under any major operating system, and also provides Python bindings (and native integration with IBM Qiskit) in order to be as accessible as possible to its community. After getting the tool using `pip install jkq.qcec`, verifying that a quantum circuit has been compiled correctly by IBM Qiskit merely requires the following lines of Python:

```
1 from jkq.qcec import Configuration, Strategy, verify
2 from qiskit import QuantumCircuit, transpile

4 # create your quantum circuit and append measurements to save output mapping
5 qc = <...>
6 qc.measure_all()

8 # compile circuit to appropriate backend using some optimization level
9 qc_comp = transpile(qc, backend=<...>, optimization_level=<0 | 1 | 2 | 3>)

11 # verify the compilation result
12 result = verify(qc, qc_comp, strategy="compilationflow")
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