IEEE ELECTRONICS PACKAGING SOCIETY Newsletter

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Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Kitty Pearsall
Boss Precision. Inc.
Austin, TX

Hi there!

Wow! It is mid-year 2022. The past six months have been extremely busy. Our community is transitioning from all-virtual to hybrid gatherings, and slowly back to primarily in-person meetings. ECTC, the largest EPS Flagship Conference was held in person this past June in San Diego. It felt good to network and to attend technical sessions, and keynotes. I am sure that you agree with me.

Working together we have delivered on several of our goals highlighted in the EPS Strategic Plan. Currently, I want to share a few of these with you. I believe that you too, will also be excited about our Electronic Packaging Society's achievements to date.

Our society's goals for technology are progressing extremely well. Key is positioning EPS as the preferred information source of forward-looking packaging technology. The EPS VP Technology (and his team of Technical Committee Chairs) have been collaborating closely with other technical leaders and experts to continue to provide insightful material for our newsletter, our EPS eNews, and to the EPS membership. Since January the Technology Team has published 8 technical papers in eNews. In process are an additional 9 authors preparing for the remainder of the year's papers. Many thanks to the following authors for making this possible.

- Benson Chen—"Smart Manufacturing"
- Wendem Beyene—"Chiplets"
- Lei Sham—"The Bunch of Wires (BoW)—An Open-Source Physical Interface Enabling Chiplet Architectures"
- Patrick McCluskey and Zhaoxi Yao—"Challenges and Advances in Electric Propulsion Motor Thermal Management for Aircraft"
- Manos Tentzeris, Yepu Cui, and Kexin Hu—"Additively Manufactured Highly Integrated mm-Wave Packaging Structures"
- Debendra Das Sharma—"Universal Chiplet Interconnect Express (UCIe)®: An open standard for developing a successful chiplet ecosystem"
- Raj Pulugurtha—"Nano Packaging at ECTC"
- Raj Pulugurtha—"3D PEIM Invitation"

In addition to overseeing 25 plus conferences annually, our VP of Conferences and his team are paving the way for increased conferences in new locations not reached yet by EPS. Two significant examples are highlighted. First, the Design and Technology for Modern Electronic Systems (DTMES) was held in Addis Ababa, Ethiopia this year (EPS Santa Clara Valley Chapter sponsored). This was the first ever EPS conference in Africa. Second, an IEEE EPS India Workshop in collaboration with the India Electronics and Semiconductor Association Electronic Pkg is targeted for year-end in Bangalore. These new conferences present growth opportunities for our membership as well as disseminate knowledge to our community.

Per Stephen Welby, IEEE Executive Director & COO, ***"2022 has been a year of not just recovery, but of sustained growth".*** The same can be said for EPS. VP Membership reported that the membership retention YoY is 83% which is greater than the EPS strategic goal of 80%. Like IEEE, EPS also has had a positive YoY membership growth of 4.8% which is a bit more than the IEEE YoY of 3.1 %. All but Regions 9 and 10 have shown an increasing retention rate for the higher-grade members.

EPS has a solid Education program that covers early professionals, mid-career, and senior engineers in the Electronics Packaging Community. Year to date there have been 24 webinars, which is in line with the 40 webinars presented in full year 2021. However, prior to 2019 the average number of webinars was 5 per year. This increase is thought to be a result of Covid putting the brakes on in-person events, workshops, and other tutorials. The sharing of chapter meetings with other chapters has been highly successful.

(continued on page 9)

NEWSLETTER SUBMISSION DEADLINES

1 December 2022 for Winter issue 2023

15 June 2023 for Summer issue 2023

Submit all material to d.manning@ieee.org

EPS Officers

President: Kitty Pearsall, kitty.pearsall@gmail.com

VP (Technology): David McCann, david.mccann@rockleyphotonics.com

VP (Conferences): Sam Karikalan, sam.karikalan@broadcom.com

VP (Publications): Ravi Mahajan, ravi.v.mahajan@intel.com

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Jr. Past Pres.: Chris Bailey, C.Bailey@greenwich.ac.uk

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2022 Term End: Regions 1-6, 7, 9—Rozalia Beica, Xuejun Fan, Subramanian S. Iyer, Region 8—Tanja Braun, Karlheinz Bock, Region 10— Gu-Sung Kim

2023 Term End: Regions 1-6, 7, 9—Mark Poliks, Annette Teng, Patrick McCluskey, Jin Yang, Region 8—Steffen Kroehnert, Region 10—Yoichi Taira, Young Professional—Yan Liu

2024 Term End: Regions 1-6, 7, 9—Benson Chan, Pradeep Lall, Wolfgang Sauter, Region 10—Kishio Yokouchi, Chuan Seng Tan, Chin-Pin (CP) Hung

Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:
Ravi Mahajan

Co-Editor Special Topics:
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Co-Editor, Electrical Performance:
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Co-Editor, Components: Characterization and Modeling:
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Power & Energy:
Douglas Hopkins

RF & Thz Technologies:
Manos Tentzeris

Photonics—Communication, Sensing, Lighting:
Vipul Patel

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Peter Ramm

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Przemyslaw Gromala

Test:
Abram Detofsky

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Industry Programs: William T. Chen, William.Chen@aseus.com

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Region 10 Programs: Andrew Tay, andrew_tay@ieee.org

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Fellows Evaluation: S.W. Rickly Lee, rickylee@ust.hk

Long Range/Strategic Planning: Kitty Pearsall, kitty.pearsall@gmail.com

Nominations: Chris Bailey, C.Bailey@greenwich.ac.uk

Distinguished Lecturers

VP Education: Jeff Suhling, jsuhling@auburn.edu

Lecturers: Ramachandra Achar, Ph.D., Mudasir Ahmad, Kemal Aygün, Ph.D., Muhannad Bakir, Ph.D., W. Dale Becker, Ph.D., Wendem Beyene, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., William T. Chen, Ph.D., Xuejun Fan, Ph.D., Philip Garrou, Ph.D., Madhu Iyengar, Ph.D., Subu Iyer, Ph.D., Beth Keser, Ph.D., Pradeep Lall, Ph.D., John H. Lau, Ph.D., Ravi Mahajan, Ph.D., James E. Morris, Ph.D., Rajen Murugan, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Eric D. Perfecto, Mark Poliks, Ph.D., Gamal Refai-Ahmed, Ph.D, Jose Schutt-Aine, Ph.D., Nihal Sinnadurai, Ephraim Suhir, Ph.D., Chuan Seng Tan, Ph.D., Rao Tummala, Ph.D., E. Jan Vardaman, Paul Wesling, C.P. Wong, Ph.D., Jie Xue, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

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SFI Logo

2022 IEEE Rao R. Tummala Electronics Packaging Award

Douglas C. H. Yu
University of California, Retired
Irvine, CA USA

Sponsored by IEEE Electronics Packaging Society

"For contributions to the development of advanced packaging technologies and their implementation in high-volume manufacturing."

Douglas C.H. Yu's leadership in developing advanced packaging technologies has paved the way for new technology standards and semiconductor trends that have supported the continued scaling of microelectronics and are enhancing high-performance computing, wireless, and artificial intelligence applications. Among Yu's many accomplishments, at Taiwan Semiconductor Manufacturing Corporation he led the introduction of the copper/low-k dielectric interconnects, which provided a significant improvement in on-chip wiring performance. He also led the development of the innovative TSMC 3DFabric system integration technology platform, which includes chip-on-wafer-on-substrate (CoWoS), integrated fan-out (InFO) wafer-level-package, and system-on-integrated chip (SoIC) technologies. This holistic solution for advanced packaging is critical to continued improvement in performance, power, and form factor of heterogeneous integrated microelectronic systems for above-stated wide applications.

An IEEE Fellow and a Distinguished Fellow of TSMC Academy, Yu is vice president of Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan.

2022 IEEE Electronics Packaging Society Award Recipients

Charlie Zhai
Apple Inc., USA
2022 IEEE EPS Electronics Manufacturing Technology Award
For his vision and industry leadership in innovating and productizing advancedpackaging technology to reshape the mobile industry.

Mukta Farooq
IBM, USA
2022 IEEE EPS Outstanding Sustained Technical Contribution Award
For leadership and intellectual property in packaging technology including development and qualification of 3D logic modules and lead-free interconnect alloys.

Yueping Zhang
Nanyang Technological University
Singapore
2022 IEEE EPS Exceptional Technical Achievement Award
For seminal contributions to the development of antenna-in-package (AiP) technology.

Duixian Liu
IBM Thomas J. Watson Research Center, USA
2022 IEEE EPS Exceptional Technical Achievement Award
For seminal contributions to the development of antenna-in-package (AiP) technology.

Xiaoxiong (Kevin) Gu
Metawave Corporation, USA
2022 IEEE EPS Exceptional Technical Achievement Award
For seminal contributions to the development of antenna-in-package (AiP) technology.

Chris Bailey
University of Greenwich, United Kingdom
2022 IEEE EPS David Feldman Outstanding Contribution Award
For outstanding service and technical leadership to the Electronics Packaging Society resulting in the growth and relevancy of EPS in a fast-changing electronic packaging landscape.

Fumihiro Inoue
Yokohama National University, Japan
2022 Outstanding Young Engineer Award
For groundbreaking contributions to the development of 3D integration, including electro/electroless deposition, extreme Si thinning, wafer bonding and singulation process.

Peng Zhao
Nanyang Technological University, Singapore
Institute of Microelectronics (A*STAR), Singapore
2022 PhD Fellowship
For contributions to 3D packaging of trapped ion devices for application in quantum information processing.

Rajen Murugan
Texas Instruments, Inc., USA
2022 IEEE EPS Regional Contributions Award—Regions 1 – 7 & 9 (Americas)
For founding the EPS Dallas Chapter and demonstrating exemplary leadership and sustained technical contributions in enabling and promoting EPS and IEEE programs and activities in the Dallas Section and Region 5.

Rolf Aschenbrenner
Fraunhofer Institute for Reliability and Microintegration (IZM), Germany
2022 IEEE EPS Regional Contributions Award—Region 8 (Europe, Middle East and Africa)
For outstanding accomplishments in the development of new interconnect technologies for single chip packaging, as well as in various areas of 3D IC integration and 3D Packaging.

Masahiro Aoyagi
Kumamoto University, Japan
2022 IEEE EPS Regional Contributions Award—Region 10 (Asia & Pacific)
For contribution to enhance collaboration in Region 10, especially between Japan and Singapore and achievement to develop 3D LSI chip stacking technology with TSVs and micro-bumps.

Chris Bailey 2022 EurosimE Award Receipent

Chris Bailey, EPS Jr. Past President, received the EurosimE 2022 Achievement Award "for his outstanding contributions to thermal and multi-physics simulation and experiments in microsystems as well as research on various industrial applications."

Congratulations to IEEE EPS Senior Members New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between December 2021 and April 2022.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

For additional information or to apply online: https://www.ieee.org/membership/senior/

David Armstrong, Denver Section
Koushik Banerjee, Phoenix Section
Anandaroop Bhattacharya, Kharagpur Section
Hua Chen, Guangzhou Section
Vasiliki Giagka, Benelux Section
Blake Gray, Atlanta Section
Zhang Ju Hou, Guangzhou Section
Kenji Okada, Kansai Section
James Petroski, Cleveland Section
Herbert Stopper, Florida West Coast Section
Bruce Weiss, Milwaukee Section
Tiong Leh Yap, Singapore Section
Tianchun Ye, Beijing Section

ECTC 2022 Travel Award Winners

Congratulations to the winners of the 2022 ECTC travel award. The award is intended to assist students to attend ECTC.

Ramesh Kudalippalliyalil	Information Sciences Institute (ISI/USC)
Yu-Tao Yang	UCLA ECE
Zeinab Shaban	Tyndall National Institute, University College, Cork
Akeeb Hassan	Florida International University
Peng Zhao	Nanyang Technological University
Firas Alshatnawi	Binghamton University
Yi Zhou	Georgia Tech
Xiaofan Jia	Georgia Tech
Kruitkesh Sahoo	UCLA
Woosol Lee	University of Florida

Congratulations to the ECTC Volunteer Award Recipients

The EPS/ECTC Volunteer Award is given to those individuals who contribute to the success of the ECTC by volunteering in one of the conference committees, year after year. Here are the 2022 EPS/ECTC Volunteer Award winners:

10 year Volunteers

Kemal Aygun
Tz-Cheng Chiu
Gordon Elger
Jae-Woong Nah
Valerie Oberson
Dan Oh
P. Markondeya Raj
Katsuyuki Sakuma
Dwayne Shirley
Ivan Shubin
Yoichi Taira

EPS Major Awards Nomination Period Starts on September 15

All the EPS Major Award nominations will require line submission. The nomination period to input all the required documents runs from September 15 to January 21. The Electronics Packaging Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and EP Society.

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Must have been a member of the IEEE and EP Society for the past three (3) years (2020–2022), and renewed for 2023.

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. Work in the management of EPS Conferences or its BoG may be contributory, but it is not a requirement for the award.

Eligibility: No need to be a member of IEEE and EP Society.

IEEE William Chen Distinguished Service Award: To recognize and honor outstanding service and leadership to the Electronics Packaging Society and its sponsored activities.

Prize: US$5,000 and Certificate

Basis for Judging: Recipient is required to have made outstanding contributions to expanding the Society's impact in the electronic packaging field and profession through service and leadership within the EPS organization, including activities at the Chapter, Regional or BoG level or through the society's primary conferences and workshops. Examples would include serving as a conference chair, society officer, regional director, etc.

Eligibility: At the time of nomination, the nominee must have been continuously a member for the previous ten (10) years of IEEE and EPS with respect to the year of presentation of the award, and have already renewed the membership for the year of presentation of the award.

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the EP Society.

Prize: $2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction

of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in EPS's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for the past three (3) years (2020–2022), and renewed for 2023. There are no requirements for service to the IEEE or EP Society.

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the EP Society through invention, technical development, publications, or new product implementation.

Prize: $1,500 and Certificate

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the EPS Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Must have been a member of the IEEE and EPS (member grade or above) for the past three (3) years (2020–2022), and renewed for 2023, and must be 35 years of age, or younger, on December 31, 2023.

Regional Contributions Award: To recognize significant and outstanding leadership and contributions to the growth and impact of EPS programs and activities at the Region level. Maximum of one award annually from each Region/Groups of Regions (3 awards): Regions 1-7 & 9; Region 8; and Region 10.

Basis for Judging: Demonstrated service and leadership in areas that may include but are not limited to Chapter activities, Conference/Workshop activities, Membership Development, Student Programs and Technical Activities. The respective EPS Regional Advisory Committees will receive nominations, evaluate candidates, select a candidate(s), and present candidate(s) to EPS Awards Committee for review and approval.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for the past three (3) years (2020–2022), and renewed for 2023.

Guidelines for Nominators:

- A recipient of any EPS Major Award will be eligible for nomination for another EPS Major Award *after two award cycles have passed*. (i.e., Recipient of XX Award in 2020 becomes eligible for nomination for YY Award in 2023). For lists of past awardees, see http://eps.ieee.org/awards.html
- Past recipients of an award are not eligible to receive that same award. For lists of past awardees, see http://eps.ieee.org/awards.html
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- An individual may submit only one endorsement per award but may submit endorsement for more than one award.
- It is the responsibility of the nominator to ensure quality documentation to assist the Awards Committee in evaluating the candidate.
- Outstanding Sustained Technical Contribution Award is designed for the "practitioner", while the Electronics Manufacturing Technology Award intended for "Corporate Leadership".
- Complimentary material, such as candidate's picture, CV, list of publications and/or patents should be submitted separate from the award nomination.
- Self-nominations **will not** be considered.

EPS PhD Fellowship:

To promote, recognize, and support PhD level study and research within the Electronics Packaging Society's field of interest.

Prize: A plaque and a single annual award of US$5,000, applicable towards the student's research.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electronic packaging and a proven history of academic excellence, as documented in:

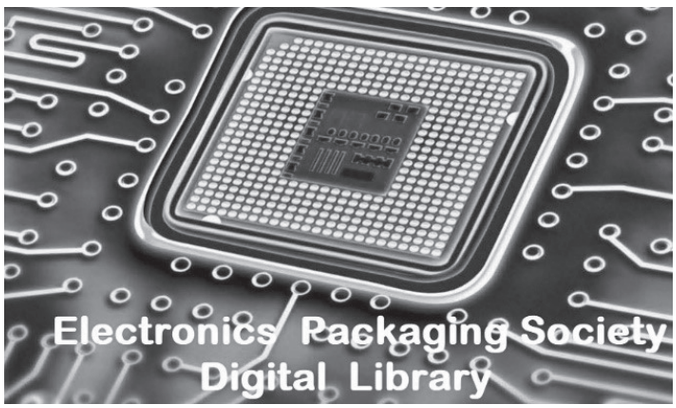
- Nomination by an IEEE EPS Member. Only one nomination per member per year.
- Two-page (maximum) statement by the student describing his or her education and
- Research interests, accomplishments, and impact on the electronics package industry.
- Proof of contributions to the community may consist of open literature publications (preferred) such as papers, patents, books, and conference presentations and reports (available to the public).
- At least one letter of recommendation from someone familiar with the student's work
- Student resume

Eligibility: Candidate must be an IEEE EPS member, at the time of nomination, and be pursuing a doctorate degree within the EPS field of interest on a full-time basis from an accredited graduate school or institution. The candidate must have studied with her/his advisor for at least 1 year, at the time of nomination, to be eligible. A Student who received a Fellowship award from another IEEE Society, within the same year, or is a previous EPS Fellowship winner is ineligible.

All Award nominations must be **online.** Nominations questions can be sent to the Society Awards Program director:

Patrick McCluskey
mcclupa@umd.edu

Winners will be notified by April 2023, and the awards will be presented at the 73rd Electronic Components and Technology Conference (ECTC). **Date and venue will be announced when determined.**



NEW—Society Member Digital Library

Beginning with the 2023 renewal cycle, EPS members will have access to the new EPS Society Digital Library!

This will include online access via Xplore to the Transactions on Components, Packaging and Manufacturing Technology (T-CPMT), EPS sponsored conference proceedings including ECTC, ESTC, ITherm and more!

Unlimited access to current and past issues of T-CPMT and proceedings for EPS sponsored conferences from current year to the early nineties.

IEEE Senior Membership: Are You In?

If you have been involved in the electronics packaging field for 10 years or more, chances are that you probably already have the necessary qualifications to be an IEEE Senior Member. Senior membership is the highest IEEE membership grade that can be applied for and is a recognition of sustained and significant performance in an IEEE-designated field. Individuals who are IEEE members can apply themselves for elevation to Senior Member or they can be nominated by others. Since a member can be nominated by someone else for Senior Membership, Society Chapters can play an important role in helping to identify and support applications for elevation. Nominating individuals in our Chapters is a great way to recognize their professional achievements and foster deeper personal and professional relationships with our peers. Individual members shouldn't hesitate to apply for Senior Member elevation on their own as well, and call upon their IEEE colleagues for support for their application. The requirements for Senior Member eligibility are very straightforward:

- The candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE-designated fields
- Candidates shall have been in professional practice for at least ten years
- Candidates shall have shown significant performance over a period of at least five of those years

As a member of EPS, the IEEE-designated field criteria will generally have been met. The criteria for ten years of professional practice can also take into account some portion of your educational experience as well as time spent in one's job or career, so a ten-year employment record isn't necessarily required. The final criteria of demonstrating significant performance over at least five of those ten years can be met in many different ways, including technical work, managerial responsibility, and publications to name a few. IEEE provides detailed information on the requirements for Senior Member grade at https://www.ieee.org/membership/senior/senior-requirements.html, along with sample cases that can be helpful for comparison to your own professional experiences.

Individuals applying for or nominating someone for Senior Member elevation can find additional information on the IEEE website at https://www.ieee.org/membership/grade-elevation.html and clicking on the Senior Member Grade link found there. Candidates applying for Senior Membership will need to supply three references from current IEEE members who are Fellows, Senior Members, or Honorary Members, and this is where EPS colleagues can support one another. Members of EPS chapters already have a group of local contacts that can help with nomination and reference support, simplifying and streamlining the process. Prospective applicants can find potential references through IEEE Collabratec via a link at the top of the EPS Membership page. There is also a link to the general Collabratec page on the MGA Senior Member Requirements page.

IEEE Senior Membership is a way for the Society to recognize the dedication and achievements of our members as well as a way to support our colleagues. If you have any questions about the Senior Membership application process or requirements, please don't hesitate to reach out to your local chapter or to us here at EPS for assistance.

Thanks
Alan Huffman, EPS VP Membership

PUBLICATIONS NEWS

2021 CPMT Best Transactions Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 200 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

Subscribers to this publication can access the papers on-line in IEEE Xplore at: http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870

Advanced Packaging Technologies Category
"Fan-Out Panel-Level Packaging of Mini-LED RGB Display" John H. Lau; Cheng-Ta Ko; Curry Lin; Tzvy-Jang Tseng; Kai-Ming Yang; Tim Xia; Puru Bruce Lin;Chia-Yu Peng; Eagle Lin; Leo Chang; Ning Liu; Show May Chiu; Tzu Nien Lee; Volume 11, Issue 5, May 2021

Abstract:
In this study, the feasibility of mini-light-emitting diode (LED) RGB display fabricated by a chip-first fan-out panel-level packaging is investigated. Emphasis is placed on the design, materials, process, fabrication, and reliability of the mini-LED RGB display package on a printed circuit board (PCB). The mini-LEDs under consideration and their sizes are red (125 × 250 × 100 μm), green (130 × 270 × 100 μm), and blue (130 × 270 × 100 μm). The spacing among the RGB mini-LEDs is 80 μm, the pixel-to-pixel spacing is also ~ 80 μm, and the pixel pitch is 625 μm. The temporary glass panel for making the redistribution layers (RDLs) of the package is 515 × 510 × 1.1 mm in size. To increase the SMT assembly yield on the PCB, the mini-LEDs are grouped into 4(2 × 2 pixels)-in-one surface mount device (SMD), that is, a total of 12 R, B, and G mini-LEDs. A PCB (132 mm × 77 mm) is designed and fabricated for the drop test of the mini-LED package. Thermal cycling of the mini-LED SMD PCB assembly is also performed by a nonlinear temperature- and time-dependent finite-element simulation.

URL: https://ieeexplore.ieee.org/document/9393937

Components: Characterization and Modeling Category
"Cascaded Multi-Core Vapor Chambers for Intra-Package Spreading of High Power, Heterogeneous Heat Loads" Soumya Bandyopadhyay; Amy M. Marconnet; Justin A. Weibel; Volume 11, Issue 6, June 2021

Abstract:
A cascaded multicore vapor chamber (CMVC) is designed for dissipating heat from high-flux hotspots simultaneously with a high-total-power background. Current thermal management strategies rely on spreading high local heat fluxes by conduction in the lid of electronics packages. Embedding vapor chambers (VCs) within the lid is an attractive option to directly address intrapackage hotspots. We investigate the design of intralid VCs, for a generic device having a total heat load of 476 W having a background heat flux of 0.75 W/mm 2 , with hotspots of 8 W/mm 2 over a 1-mm 2 area. A conventional VC design, having a single vapor core, will require a thick evaporator wick to avoid the capillary limit for large total power. The necessity for a thick wick then imposes a large thermal conduction resistance when the VC is exposed to high heat flux hotspots. The proposed CMVC architecture aims to address this limitation. The cascaded architecture comprises a bottom-tier VC having an array of multiple small vapor cores for spreading heat from the small hotspots. These small vapor cores have short paths of liquid return to the evaporator, such that they can handle their footprint heat load while using thin wicks, resulting in a low hotspot thermal resistance. Furthermore, local dampening of the hotspots by the bottom tier then reduces the thermal conduction resistance across the necessarily thick wick in the top tier. Hence, the cascaded architecture has the potential to significantly reduce the overall thermal resistance, relative to a single tier. To substantiate this design rationale, experiments are performed to illustrate that the resistance of a commercial VC can be significantly reduced by interfacing the heat source with an intermediate heat spreader. Reduced-order models are then used to understand the effect of the wick properties (porosity and particle size) and geometric parameters on the thermal performance of the CMVC for the representative power map. The optimal CMVC design offers a thermal resistance (0.66 K/W) that is significantly lower compared to a conventional single-core VC (1.76 K/W) owing to a reduction in the conduction resistances across the internal wicks. That parametric optimization results demonstrate that the thermal resistance of the CMVC is more sensitive to the wick porosity compared to the particle diameter. Furthermore, there exists a wide range of wick properties and vapor core sizes for which near-optimum thermal performance can be attained, which is particularly attractive from the standpoint of flexibility in design and manufacturing.

URL: https://ieeexplore.ieee.org/document/9391679

Electronics Manufacturing Category:
2021 "Towards 224Gb/s Electrical Signaling – Modulation, Equalization and Channel Options" Masum Hossain; Wendemagegnehu T. Beyene; Volume 11, Issue 3, March 2021

Abstract:
This article explores different modulation and signaling techniques with the goal to achieve 224-Gb/s link speed through electrical signaling. Focus of this work spans from interconnects to transceiver architecture from system and signaling point of view. In addition to traditional multilevel signaling pulse amplitude modulation-4 (PAM-4 and PAM-8), this work also compares simultaneous bidirectional signaling and multiwire encoding techniques as potential solutions beyond 224-Gb/s link. These signaling options are compared both from performance and implementation complexity point of view with possible improvements required to further extend the speed and reach of electrical signaling.

URL: https://ieeexplore.ieee.org/document/9336667

Best Associate Editor Award

To recognize the work and efforts of our Associate Editors, EPS instituted the Best Associate Editor Award. The 2022 recipients are:

Lavanya Aryasomayajula—Intel
Yogendra K. Joshi—Georgia Institute of Technology
Xiaoxiong (Kevin) Gu—Metawave Corporation

Most Popular Articles according to Xplore® usage statistics

Recent Advances and Trends in Advanced Packaging
John H. Lau
Publication Year: 2022, Page(s): 228–252

CPU Overclocking: A Performance Assessment of Air, Cold Plates, and Two-Phase Immersion Cooling
Bharath Ramakrishnan; Husam Alissa; Ioannis Manousakis; Robert Lankston; Ricardo Bianchini; Washington Kim; Rich Baca; Pulkit A. Misra; Inigo Goiri; Majid Jalili; Ashish Raniwala; Brijesh Warrier; Mark Monroe; Christian Belady; Mark Shaw; Marcus Fontoura
Publication Year: 2021, Page(s): 1703–1715

A Review of 5G Front-End Systems Package Integration
Atom O. Watanabe; Muhammad Ali; Sk Yeahia Been Sayeed; Rao R. Tummala; Markondeya Raj Pulugurtha
Publication Year: 2021, Page(s): 118–133

Thermal and Mechanical Characterization of 2.5-D and Fan-Out Chip on Substrate Chip-First and Chip-Last Packages
Meng-Kai Shih; Weihong Lai; Tsewei Liao; Karen Chen; Dao-Long Chen; C. P. Hung
Publication Year: 2022, Page(s): 297–305

A Review of Recent Research on Heat Transfer in Three-Dimensional Integrated Circuits (3-D ICs)
Swapnil S. Salvi; Ankur Jain
Publication Year: 2021, Page(s): 802–821

President's Column (*Continued from page 1*)

The Professional Development Courses offering IEEE Continuing Educational Units has been extended to include EurosimE in addition to the EPS Flagship Conferences.

Finally, through IEEE Xplore you have access to peer-reviewed journals, refereed papers from conference proceedings, and conference presentations. In addition, the EPS VP of Publications is developing a strategy to support the IEEE's Open Access (Multidisciplinary Open Access Journal) work effort.

Looking forward I want to increase our focus on EPS partnering with JIEP and the India Electronics and Semiconductor Association. Coming challenges for the next 18 months for EPS are Digitization, Artificial Intelligence, IOT, and Smart Manufacturing, how and where this fits in the EPS Strategic plan.

Lastly, I want to express my gratitude for the dedicated support provided to the EPS Board of Governors from all VPs, Directors, Members at large, Adhoc Leaders, volunteers, and appointees. I consider myself lucky to be supported by every one of you.

- Dave McCann, VP Technology
- Sam Karikalan, VP Conferences
- Ravi Mahajan, VP Publications and India Initiative Lead
- Jeff Suhling, VP Education
- Alan Huffman, VP Membership
- Pat Thompson, VP Finance
- Chris Bailey, Jr. Past President
- Toni Matilla, Director of Chapters
- Bill Chen, Director of Industry Programs
- Mark Poliks, Director of Student Programs
- Patrick McCluskey, Director of Awards
- Annette Teng, Director of Regions 1-7 & 9
- Tanja Braun, Director of Region 8
- Andrew Tay, Director of Region 10

Members at Large and Adhoc Leads

- Regions 1-7 and 9—Xuejun Fan, Subu Iyer, Rozalia Beica, Patrick McCluskey, Mark Poliks, Annette Teng, Jin Yang, Benson Chan, Pradeep Lall and Wolfgang Sauter
- Region 8—Karlheinz Bock, Tanja Braun, and Steffan Kroehnert
- Region 10—Gu-Sung Kim, Yoichi Taira, Chih-Pin Hung, Chuan-Seng Tan, and Kishio Yokouchi.
- Yan Liu—Young Professionals
- Marta Rencz—Women in Engineering representative.
- Ricky Lee—Fellows Evaluation Chair
- Yasumitsu Orii—Partnering with outside organizations
- Pradeep Lall—Partnering with IEEE Societies

Kitty Pearsall

EDUCATION/CAREER NEWS

EPS Achievement Certificate

Congratulations to these EPS Members on receiving the IEEE Achievement Certificate from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Ken Lawrence, CAES
Stoyan Stoyanov, University of Greenwich
Sreejith Kochupurackal Rajan, Georgia Institute of Technology
Nikhilendu Tiwary, Aalto University

Congratulations to these EPS Members on receiving the IEEE Certificate of Distinguished Achievement from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Chong Leong Gan, Micron Memory Taiwan Co. Ltd.
Scott Clary, Florida Institute of Technology

EPS Distinguished Lecturer Program

EPS Distinguished Lecturers are selected from among EPS Fellows, Award winners, and Society leaders, who are members of the technical community and experts in their field. They are available to present lectures and/or courses at EPS events—Chapters, Conferences, Workshops or Symposia; as well as IEEE Student Chapter events.

The EPS Distinguished Lecturer Program (DLP) aims at serving communities interested in the scientific, engineering, and production aspects of materials, component parts, modules, hybrids and micro-electronic systems for all electronic applications.

The Program strives to support EPS Chapters worldwide by helping them to invite leading researchers in their respective fields and IEEE Student Chapters to encourage students to pursue EPS related fields and to join the EPS society. The DLP talk is a major event in the life of the inviting Chapter.

EPS Distinguished Lecturers

Ramachandra Achar, Ph.D. (7/1/2020–6/30/2024)
Department of Electronics, Carleton University
Ottawa, Ontario, CANADA
Topics: CAD tools and methodologies for interconnects, packages, and systems with an emphasis on signal, power and EMI integrity

Mudasir Ahmad (1/2022–12/2025)
Google
CA, USA
Topics: Internet of Things (IoT), Advanced Packaging, 2.5D, Heterogeneous Silicon Photonics, Advanced Reliability (Thermomechanical, Mechanical Shock), Numerical Modeling, Advanced Thermal Solutions, Stochastic Analysis, Bayesian Inference, Machine Learning, Artificial Intelligence

Kemal Aygün, Ph.D. (7/1/2020–6/30/2024)
Intel Corporation
Chandler, AZ USA
Topics: Package/socket/board/interconnect technologies, electrical simulation methodology and lab metrologies

Muhannad Bakir, Ph.D. (1/2020–1/2024)
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA USA
Topics: Emerging interconnection architectures and technologies; heterogeneous system design and integration

W. Dale Becker, Ph.D. (7/1/2020–6/30/2024)
IBM
Poughkeepsie, NY USA
Topics: Electronic Package design and integration, system design, electrical modeling tools

Wendem Beyene, Ph.D. (7/1/2020–6/30/2024)
Meta
San Jose, CA
Topics: Electrical modeling and simulation techniques for analysis of interconnects, packages, and systems. Machine learning techniques

Karlheinz Bock, Ph.D. (7/2020–7/2024)
Technische Universität Dresden
Dresden, Germany
Topics: Multifunctionality & heterosystemintegration & additive manufacturing (IoT, Industry 4.0, tactile internet), packaging for mechanical, digital and power co-integration (automotive, machines, robots..), 2.5D and 3D electro-optical-RF interposer and board (high performance), heterointegration for flexible, bio, organic and large area electronics (open form factor)

Bill Bottoms, Ph.D. (6/2021–6/2025)
Third Millennium Test Solutions
Santa Clara, CA USA
Topics: Heterogeneous Integration, Semiconductor test technology, Emerging research materials, Packaging of electronic components and systems, the global network and its future requirements, the internet of things and Smart manufacturing

Chris Bower, Ph.D. (6/2021–6/2025)
X-Celeprint Inc.
North Carolina, USA

Topics: novel assembly methods, elastomer stamp micro-transfer-printing, heterogeneous integration, three-dimensional integration, manufacturing of micro-assembled displays and other large-format electronics.

William T. Chen, Ph.D. (1/2020–1/2024)
ASE (U.S.) INC
Santa Clara, CA USA
Topics: Semiconductor and Electronics Industry Trends and Roadmap

Xuejun Fan, Ph.D. (1/2020–1/2024)
Department of Mechanical Engineering
Lamar University
Beaumont TX USA
Topics: Design, modeling and reliability in micro-/nano- electronic packaging and microsystems

Philip Garrou, Ph.D. (1/2020–1/2024)
Microelectronic Consultants of North Carolina
Research Triangle Park, NC USA
Topics: Thin film technology; IC packaging and interconnect; Microelectronic materials; 3D-IC integration

Madhu Iyengar, Ph.D. (7/1/2020–6/30/2024)
Google
Mountain View, CA
Topics: Thermal component and system design for packages, servers, and data centers.

Subu Iyer, Ph.D. (6/2021–6/2025)
University of California, Los Angeles
Los Angeles, CA USA
Topics: Heterogeneous Integration; Flexible hybrid electronics; 3D interposer, and wafer scale integration and stacking

Beth Keser, Ph.D. (1/2020–1/2024)
Intel
San Diego, CA USA
Topics: Fan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; photoimageable liquid polymer films

Pradeep Lall, Ph.D. (1/2020–1/2024)
Auburn University
Auburn, AL, USA
Topics: Semiconductor Packaging, Modeling and Simulation, Reliability in Harsh Environments, Shock/Drop/Vibration, Cu Wirebonding, Flexible Hybrid Electronics, Additive Manufacturing, Prognostics and Health Management, LEDs, Micro CT Measurements

John H. Lau, Ph.D. (1/2020–1/2024)
ASM Pacific Technology
Hong Kong
Topics: Electronics and Photonics 2D and 3D packaging and manufacturing

Ravi Mahajan, Ph.D. (7/2020–7/2024)
Intel Corporation
Arizona, USA
Topics: Advanced Packaging Architectures, Assembly Processes and Thermal Management

James E. Morris, Ph.D. (1/2020–1/2024)
Department of Electrical and Computer Engineering
Portland State University
Portland, Oregon USA
Topics: Electrically conductive adhesives; Electronics packaging; Nanotechnologies

Rajen Muguran, Ph.D. (7/2022–7/2026)
Texas Instruments
Dallas, TX, USA
Topics: Multiphysics and System Co-Design modeling for complex analog and mixed-signal packaging, mmWave/THz signal integrity, power electronics packaging, and System-Level EMI/EMC modeling, analysis, and characterization.

Mervi Paulasto-Kröckel, Ph.D. (7/2020–7/2024)
Aalto University
Helsinki, Finland
Topics: MEMS, electronics reliability, automotive components and packaging, implantable electronics, dissimilar materials & interfaces

Eric D. Perfecto, (1/2020–1/2024)
IBM Research
Poughkeepsie, NY USA
Topics:Fine pitch interconnect, chip to chip and chip to laminate connection, UBM and solder selection, chip package interaction and 2.5D fabrication

Mark Poliks, Ph.D. (1/2020 – 1/2024)
Binghamton University (SUNY)
Binghamton, NY USA
Topics: Materials and Processes, Advanced Manufacturing, Flexible Hybrid Electronics, High Speed and Additive

Gamal Refai-Ahmed, Ph.D. (7/1/2022–6/30/2026)
Xilinx
San Jose, CA, USA
Topics: Thermo-mechanical Semiconductor and Electronics Industry Roadmap and directions, Advanced holistic Thermo-mechanical solution, assembly and reliability of Heterogeneous Packaging and Silicon Photonics, Future thermo-mechanical technology, architecture for component and system

Jose Schutt-Aine, Ph.D. (1/2020–1/2024)
University of Illinois
Champaign, IL, USA
Topics: High-Frequency Measurements, Mixed-Signal Design, High-Performance Computing, electromagnetic Modeling, Signal Integrity, CAD Tools for Interconnects and Packages, Machine Learning for High-Speed System Modeling

Nihal Sinnadurai (1/2020–1/2024)
Suffolk IP11 9RZ UK
Topics: Accelerated Ageing for Reliability Assurance-theory and practical methods-including HAST (my invention originally); The use of encapsulation and plastic packaging and reliability evaluation method; PCB & Hybrid technologies; Thermal management and design

Ephraim Suhir, Ph.D. (1/2020–1/2024)
Los Altos, CA 94024 USA
Topics: Accelerated life testing; Probabilistic physical design for reliability; Bonded assemblies; Thermal stress; Predictive modeling; Fiber optics structures: design for reliability; Dynamic response to shocks and vibrations

Chuan Seng Tan, Ph.D. (6/2019–6/2023)
Nanyang Technologica University
Singapore
Topics: 3D Integration and packaging, Fine Pitch Cu-Cu Bonding Through Silicon Vias (TSVs), Group IV Semiconductors: Material Growth, Engineered Substrates, and Device Applications

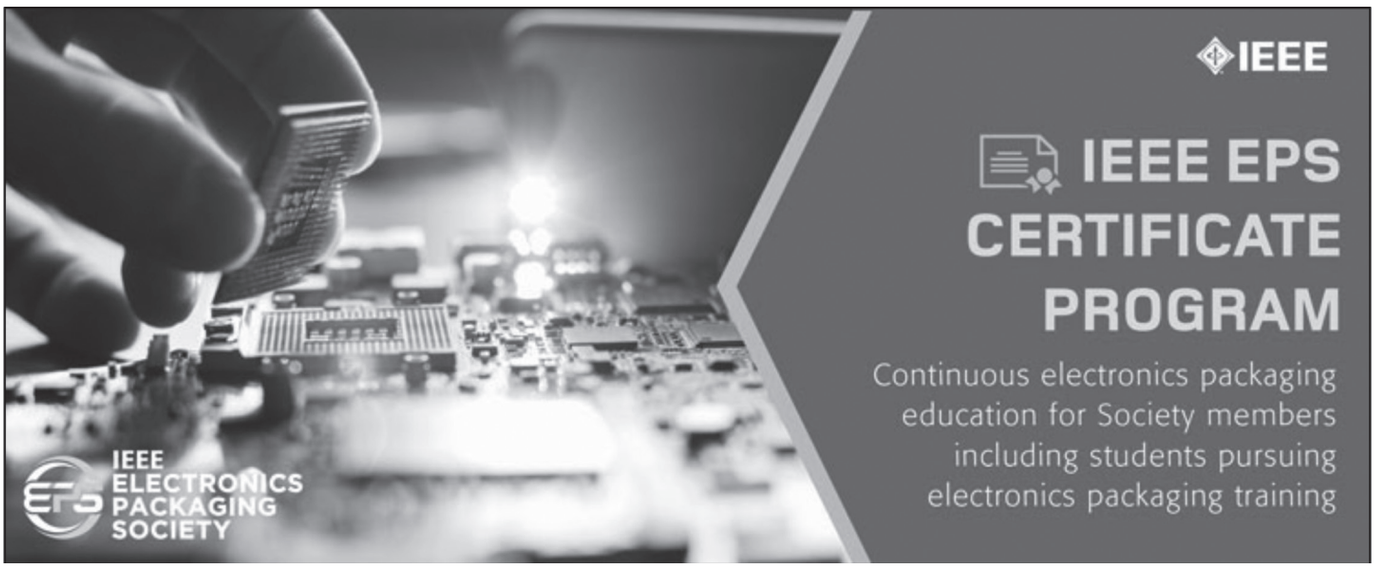
Rao Tummala, Ph.D. (1/2020–1/2024)
Microsystems Packaging Research Center (PRC)
Georgia Institute of Technology
Atlanta, GA USA
Topics: Electronics Packaging

E. Jan Vardaman (1/2020–1/2024)
TechSearch International, Inc.
Austin, TX USA
Topics: International developments in semiconductor packaging, manufacturing and assembly; SiP: Business and technology Trends; drivers in advanced packaging; Flip chip and wafer level packaging

Paul Wesling (1/2020–1/2024)
Saratoga, CA USA
Topics: Origins of Silicon Valley and the Electronics Packaging Society; the IEEE/SEMI/ASME Heterogeneous Integration Roadmap and how to use it (as editor for the 2019 Roadmap).

C.P. Wong, Ph.D. (1/2020–1/2024)
Georgia Institute of Technology
Atlanta, GA, USA
Topics: Materials

Jie Xue, Ph.D. (1/2020–1/2024)
Cisco Systems, Inc
San Jose, CA, USA
Topics: Advanced Packaging for Networking Application; Impact of Internet of Everything (IoE) to Semiconductor Industry ecosystem; High performance substrate technologies; Trends and challenges of Silicon Photonics for datacenter and networking applications



EPS Certificate Program

The IEEE Electronics Packaging Society Certificate Program provides a pathway for early and mid to late-career professionals to highlight their accomplishments.

Criteria for all Certificates: Must be an IEEE Electronics Packaging Society Member.

There are three Certificates you may apply for, which are noted below.

EPS Achievement Certificate

The first level ***EPS Achievement Certificate*** is aimed at early-career professionals working in the field of electronics packaging.

It is especially intended to encourage the career development of young professionals including advanced graduate students.

Criteria: Current EPS Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of the following:

1) IEEE EPS Webinar (1 PDH)—must complete **PDH evaluation**.
2) Professional Development Courses—must complete survey and CEU credit form. Previous ECTC PDCs from the last 10 years can be used towards this if the CEU application was completed at the time of the course. PDCs from ESTC and EPTC 2018 and forward can be used.
   - Electronic Components and Technology Conference (USA) = 4 PDHs
   - Electronic Systems-Integration Technology Conference (Europe) = 3 PDHs
   - Electronic Packaging Technology Conference (Asia) = 4 PDHs
3) Author of IEEE T-CPMT and/or EPS conference paper(s) (5 PDHs)—paper must be published in IEEE Xplore within the last 5 years.
4) Reviewer for IEEE T-CPMT (3 Reviews = 5 PDH) within the last 5 years.

Once you have completed any combination of the above and received 15 PDHs, please complete the certificate form to request your Electronics Packaging Society Certificate of Achievement.

EPS Distinguished Achievement Certificate for Technical Leadership and Expertise

Criteria: Must be a current EPS member

There are five high-level focus areas for this new certificate. These areas include:

1) Being a recognized authority of technical expertise in one's field.

Being a recognized authority of technical expertise in electronics packaging. Examples include being an advanced member of the technical staff at a company (e.g. Fellow, Senior Technical Staff, Distinguished Engineer, etc.), making technical contributions as a Member or Fellow of professional associations/societies related to electronics packaging (e.g., IEEE, IMAPs, SMTA, ASME, etc.), and being an invited speaker at companies, technical conferences, and EPS Chapter meetings.

2) Being a subject matter expert (SME) in electronics packaging at conferences, keynotes, webinars, blogs.

Methods to demonstrate participation as a SME include abstracts accepted and papers presented at conferences, giving keynote lectures at conferences or professional society meetings, presenting webinars for EPS and other IEEE Societies, and serving on technical panels at conferences and other venues.

3) Demonstrating sustained technical contributions to the electronics packaging.

Demonstrating sustained technical contributions to industry including publishing well-cited technical papers at conferences and in journals, book chapters, and patents; serving as an editor of a journal or reference book; and being a leader or participant in industry blogs, focus groups, technical roadmaps, newsletters, and forums.

4) Documenting advanced technical recognitions in electronics packaging.

Methods to document technical recognitions include receiving technical awards from a company, institute, professional society, or academic institution; being the acknowledged inventor of a seminal technology or process important to industry; serving as the point person for global high-level task force activity; and being elected to be a Member of an organization such as the US National Academy of Engineering, Royal Academy of Engineering, Chinese Academy of Engineering, IBM Academy of Technology, etc.

5) Provide at least one endorsement letter.

Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31.

EPS Distinguished Achievement Certificate for Professional Engagement and Service

Criteria: Must be a current EPS member

There are four high-level areas of focus for this new certificate. These areas include:

1) Demonstrating leadership in the electronics packaging field.

Leadership and broad impact activities in electronics packaging can be documented from outstanding accomplishments during industry employment or for notable volunteer contributions to the profession and society.

2) Illustrating broad impact/influence in the electronics packaging field.

Examples of significant professional service include serving as an officer in a technical society at the international, national, or local chapter level; participating in packaging related technical committees, councils, or affinity groups; contributing to technology roadmaps such as the Heterogeneous Integration Roadmap (HIR); and receiving a professional society or industry award based on service contributions.

3) Providing extensive service and "give back" to the profession and/or industry; and

Documentation of "give-back" to one's technical community can be accomplished via demonstrations of coaching and mentoring of co-workers, young professionals, and students.

4) Provide at least one endorsement letter.

Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1–June 30 and Aug 30–Oct 31.

More details on the Certificate Program are available on the EPS website at https://eps.ieee.org/education/eps-certificate-program.html. The EPS Certificate Program is sponsored by the IEEE EPS VP Education and is offered only to EPS members. For questions, please contact Jeff Suhling (jsuhling@auburn.edu).

EPS Resource Center

The IEEE EPS Resource Centers contains valuable, technical content from reputable experts to enhance research or industry work, implement trainings, or earn CEU/PDH credits—all of which are universally available on demand.

IEEE EPS Resource Centers benefits include:

- Access to valuable technical community content
- Access to content 24 hours a day, 7 days a week through an easy-to-use global portal
- Available at no cost for EPS members
- Opportunities to earn CEUs and PDHs

Top webinars:

- The Evolution of Lead-Free Solder Alloy
- Powering Heterogeneous Integration: An Overview of the Integrated Power Electronics Chapter of the HIR Roadmap
- Thermal Management Challenges and Opportunities for Heterogeneous Packages
- Overview of the Integrated Photonics Chapter of the Heterogeneous Integration Roadmap
- Advanced Packaging for Autonomous Driving

https://resourcecenter.eps.ieee.org/

The 72nd ECTC Conference—Back In-Person

Submitted by Michael Mayer, Assistant Program Chair, IEEE ECTC 2023

This year's IEEE Electronic Components and Technology Conference (ECTC) saw the return to an in-person event after the previous instances were virtual conferences. ECTC took place once again in San Diego, California, at the rejuvenated Sheraton San Diego Hotel and Marina, from May 31 to June 3, 2022. The conference brought together a total of 1,509 industry professionals, academics, and students in attendance from 24 countries.

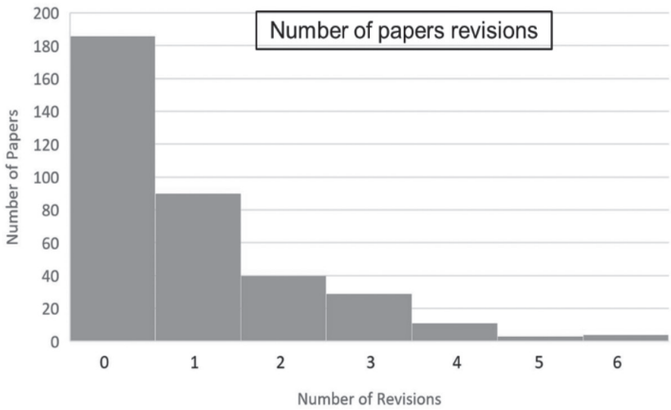
The 72nd ECTC included 362 technical contributions, which were organized into 36 oral sessions and 5 interactive presentation (IP) sessions. There were 9 special sessions. The 16 professional development courses (PDCs) were attended by 337 attendees. The conference had more than 100 exhibitors at the Technology Corner Exhibit, a tribute to the quality of the conference and its attendees. The conference benefited from a strong number of sponsors and sponsorship, further testament to the value delivered by this flagship conference.

Preparations for the 72nd ECTC started last October, when the professional volunteers serving in ECTC's technical subcommittees reviewed a strong number of 488 submitted abstracts. Ultimately, 71% of the submissions were accepted, leading to 362 presentations at the conference. This year, 54% of the submitted abstracts were from corporations, and 46% were from academia and from research institutions. In a testimony to the diversity of the industry and the conference, abstracts were received from 25 countries with the Unites States, Taiwan and South Korea leading the way in number of abstract submissions. Due to travel restrictions, mainly from Asia countries about 1/3 of the papers were presented via a pre-recorded format with written questions sent to the authors directly. Affected also by travel restrictions was our ECTC 2022 General Chair, Rozalia Beica, who over a year of weekly telecoms directed the ExComm resulting in an outstanding conference.

Ten technical subcommittees decided on the conference program at the virtual Technical Program Committee's annual planning meeting on November 5, 2021. The technical subcommittee chairs and session chairs did an excellent job developing interesting sessions and communicating with their session authors, to ensure non-commercial and previously unpublished manuscripts to be ready in time for the conference. The session chairs reviewed

	in person	virtual
Technical Sessions	162	90
Interactive Presentations	60	50
Total	222	140

Distribution on in person and virtual presentations at the 20222 ECTC.



the submitted manuscripts for quality and novelty and in some cases requested edits prior to final acceptance. ECTC again used the IEEE Computer Society Conference Publishing Services to receive and process manuscripts. As in previous years, the IEEE Cross-Check system was used to ensure that all of the ECTC manuscripts maintain a high level of original content. Over 50% of the papers required at least 1 revision, some had up to 6 revisions.

From Tuesday May 31 to Thursday June 2, we had the pleasure to attend a series of special sessions, special panels, and plenary presentations. As usual, the first day of the conference, the Tuesday following Memorial Day, featured PDCs and a variety of special sessions. This year, the conference had eight morning PDCs, running from 8 a.m. to noon, and another eight afternoon PDCs, running from 1:30 p.m. to 5:15 p.m. The total number of PDC attendees was 334. The courses continued to serve a convenient way for students and engineers to quickly get "up to speed" on the current topics of importance in electronics packaging. A total of 2 PDCs were new, and 1 PCD was virtual.

For the first time, we had the high number of six special event organized on Tuesday. In the morning from 8:30 to 10:00,

72nd ECTC during in-person lunch.

ECTC Special sessions were very well attended.

Chukwudi Okoro—Corning Inc., and Benson Chan – Binghamton University, organized a special session on high volume manufacturing of MicroLED display technology with six invited panelists from Lumiode, PARC, Playnitride, XDisplay, Corning Inc., and Yole Development.

Tuesday morning was also the occasion of the IEEE EPS Heterogeneous Integration Roadmap (HIR) special session from 10:30 am to 12 pm. This session was chaired by Amr Helmy—Univ. of Toronto and Seoung Wook Yoon—Samsung. This activity is organized under the auspices of IEEE EPS.

Next was the special session on chiplet to co-packaged optics from 1:30 pm to 3 pm, chaired by E. Jan Vardaman—TechSearch International, with panelist from Intel, Cisco, Marvell and AMD.

It was followed by the special session on IC substrate evolution towards next generation heterogeneously integrated high performance applications, 3:30 pm to 5 pm, chaired by Kuldip Johal—Atotech Group, and Bora Baloglu—Amkor. Panelist came from Intel, Amkor, AT&S, Ajinomoto Tine-Techno USA, and Atotech.

The ECTC Student Reception, sponsored by Texas Instruments, was held on Tuesday from 5 pm to 6 pm. A steady stream of student attendees took advantage of the opportunity to mingle and network with professionals in the field. Right after this, the General Chair's Speakers Reception was given from 6-7 pm for Speakers and Session Chairs. These receptions provided a great start to the conference, and helped prepare everyone for the following three days filled with technical presentations and networking opportunities. The Young Professionals Networking Panel and Reception took place from 7 pm to 7:45 pm and was chaired by Yan Liu—Medtronic, and Adel Bajwa – Kulicke and Soffa.

The Tuesday program ended with the EPS President's Panel Session from 7:45 pm to 9:15 pm, chaired by Kitty Pearsall—EPS President and Boss Precision, and Christopher Riso—Booz Allen Hamilton. Panelist were from the Office of the Undersecretary of Defense for Research and Engineering, Intel, and Qorvo.

On Wednesday, we were also able to enjoy an excellent keynote presentation from Chris Koopmans, COO, Marvell. Chris was virtually introduced by Rozalia Beica, the 2022 ECTC General Chair. The presentation focused on cloud-optimized silicon to accelerate data infrastructure. Awards for best and outstanding papers from the virtual 71st ECTC 2021 and the Intel Best Student Paper Award were presented by Allan Hoffman.

The Diversity and Career Growth Panel and Reception was co-organized with ITherm and chaired for ECTC by Kim Yess—Brewer Science, and for ITherm by Christina Amon—University of Toronto. Francoise von Trapp—3D InCites, served as moderator during the panel on Wednesday which lasted from 6:30 pm to 7:30 pm. Panelists were from IBM, Lam Research, Edwards Vacuum, and Cadence.

Texas Instruments Student reception.

Tuesday Luncheon: Keynote speaker and 2021 Best and outstanding papers Awards.

Also on Wednesday, Rozalia Beica—AT&S and General Chair ECTC, organized the plenary session on the digital transformation enabling future growth of semiconductor and advanced packaging, from 7:45 pm to 9:15 pm. Panelist were from Intel, TSMC, Yole Development, Onto Innovation, Samsung, and Atotech.

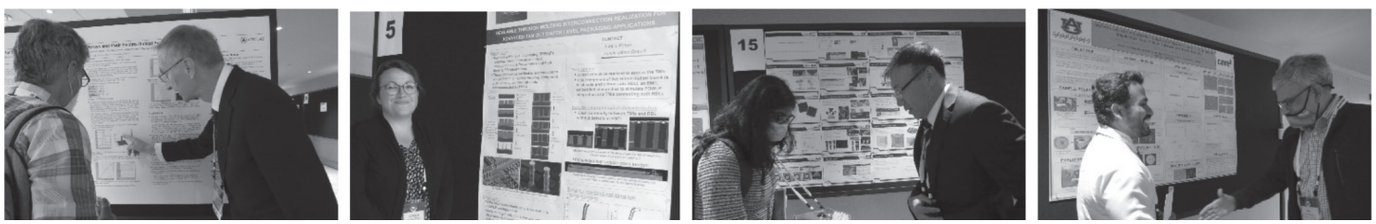
On Thursday from 8 pm to 9:30 pm, the EPS Seminar took place about interconnect technologies for chiplets, chaired by Yasumitsu Orii—Nagase and Shigenori Aoki—Lintec. Panelists were from Intel, IBM, Unimicron, TSMC, SPIL, and Furukawa Electric.

Each day at ECTC begins with the Speakers Breakfast in which the presenters and session chairs meet and take care of the preparatory work for their respective sessions. The PDC Chair, Kitty Pearsall, provided instructions to the PDC instructors and proctors on Tuesday morning, and Karlheinz Bock, the Program Chair, hosted these breakfast meetings.

Wednesday marks the start of the technical sessions with six sessions running in parallel throughout each of the three days. Each oral session featured seven paper presentations, and the interactive presentation sessions featured between15 and 25 papers. Wednesday morning started with large crowds in the six sessions with titles "Advanced Packaging for Heterogeneous Integration and High-Performance Computing", "High Performance Dielectric Materials for Advanced Packaging", "Antenna-in-Package for Communication, Radar and Energy Transfer", and "Hybrid Bonding and Innovations for 3D Integration", "Bonding Technology: Novel Assembly Methods and Processes", and "Emerging Modeling Including AI and Machine Learning". In parallel, the first of five interactive sessions took place from 9–11 am, with 25 paper presentations. High session attendance was noted also after the keynote luncheon in the afternoon sessions, with the topics "Advanced Flip Chip and Embedded Substrate Technologies", "Hybrid and Direct Bonding Development and Characterization", "Millimeter-Wave Antenna-In-Package: Design, Manufacturing and Test", "Novel Photonics Packaging Technology", "Automotive and Harsh Environment", and "Manufacturing and Assembly Process Modeling". Again in parallel, the second interactive session took place from 2–4 pm, with 23 paper presentations. Attendees rated all oral and interactive session paper ratings only through the ECTC mobile app "Whova".

The Thursday morning sessions were well attended and covered the topics "Technologies for Heterogeneous Integration, Automotive and Power Electronics", "Novel Bonding and Stacking Technologies", "Enhanced Methods & Processes for Heterogeneous Integration Assembly", "Hybrid & Direct Bonding Innovation, Optimization & Yield Improvement", "Novel Characterization Techniques and Test Methods", and "Flexible, Wearable Sensors and Electronics". Thursday afternoon included the sessions "Advances in Fan-Out Panel Level Packaging", "Enhancements in Fine-Pitch Interconnects, Redistribution Layers and Through-Vias", "Millimeter-Wave RF Components and Modules for 5G", "AI, Quantum Computing and Novel 3D Packaging Solutions",

Speaker Breakfast and Technical Sub-committees.



ECTC Interactive Presentations.

Thursday EPS Luncheon presented Best Transactions paper, Best Editors, New IEEE Fellows and Major Awards.

Network opportunities at the ECTC.

Best Session Paper

Proof of Concept: Glass-Membrane Based Differential Pressure Sensor
Anatoly Glukhovskoy, Maren S. Prediger, Jennifer Schäfer—Leibniz University; Norbert Ambrosius, Aaron Vogt, Rafael Santos, Roman Ostholt— LPKF Laser & Electronics AG; Marc Christopher Wurz—Leibniz University

2) Best Interactive Presentation Paper
System in Package Embedding III-V Chips by Fan-Out Wafer Level Packaging for RF Applications
Arnaud Garnier, Laetitia Castagné, Florent Gréco— CEA-Leti; Thomas Guillemet—Thales DMS; Laurent Maréchal, Mehdy Neffati—United Monolithic Semiconductors; Rémi Franiatte, Perceval Coudrain—CEA-Leti; Stéphane Piotrowicz—III-V Lab; Gilles Simon—CEA-Leti

3) Outstanding Session Paper
Ultra-Thinning of 20-nm Node DRAMs Down to 3 µm for Wafer-on-Wafer (WOW) Applications
Zhiwen Chen, Naoko Araki, Youngsuk Kim, Tadashi Fukuda, Koji Sakui, Tomoji Nakamura - Tokyo Institute of Technology; Tatsuji Kobayashi, Takashi Obara—Micron Memory Japan; Takayuki Ohba—Tokyo Institute of Technology

4) Outstanding Interactive Presentation Paper
Cu-Recrystallization and the Formation of Epitaxial and Non-Epitaxial Cu/Cu/Cu Interfaces in Stacked Blind Micro Via Structures
Tobias Bernhard, S. Dieter, Roger Massey, S. Kempa, E. Steinhäuser, Frank Brüning—Atotech Deutschland GmbH

5) Intel Best Student Session Paper
Mechanical Behavior and Reliability of SAC+Bi Lead Free Solders with Various Levels of Bismuth
KM Rafidh Hassan, Jing Wu, Mohammad S. Alam, Jeffrey Suhling, and Pradeep Lall—Auburn University

"Advanced Processes for Manufacturing and Yield Enhancement", and "Thermal Management and Warpage Analysis of Highly Integrated Packages".

The IEEE Electronics Packaging Society President, Kitty Pearsall, presided over the luncheon on Thursday and presented the EPS Society Awards and introduced the society new Fellows. The recipients were presented with a certificate and warm applause from the audience.

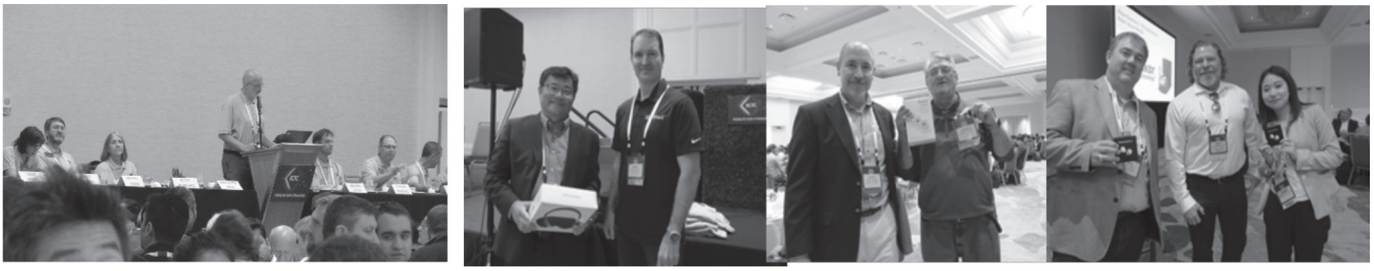
The ECTC 2022 Technical Program Committee meeting was held on Thursday at 5:30 p.m. Florian Herrault, who will serve as the Program Chair for ECTC 2023, chaired this meeting and presented the statistics of the 72nd ECTC and the timeline for the run up to the 73rd ECTC that is planned to be held in Orlando next year. Florian Herrault also introduced Michael Mayer of the University of Waterloo as the Assistant Program Chair of the 73rd ECTC. This meeting also enabled the ECTC technical program subcommittees to get in touch with potential new members of their committees.

The Gala Reception on Thursday evening was the highlight of the week for the conference attendees, exhibitors, sponsors, and their guests. It was setup outside between San Diego bay and the hotel, in the shade of large trees. It was a time to celebrate the success of the ECTC by socializing and enjoying the excellent food and beverages that were supported by the Gala Reception Gold and Silver sponsors.

2021 ECTC Best Paper Awards

Friday morning sessions were also well attended, covering the topics "Advancements in 2.5D and 3D Packaging Technology", "Soldered and Sintered Interconnections", "Interconnection Reliability", "Packaging Assembly: Solder, Sintering, and Thermal Interface Materials", "Materials and Processes for Fan-Out and Advanced Packaging", and "High-Speed Challenges in Power and Signal Integrity". Friday afternoon included the sessions "Fan-Out Packaging Technologies and Applications", "Advanced Interconnect and Wire Bond Technologies for Flexible Device Applications", "Advanced Reliability Modeling and Characterization", "Processing Enhancements in Fan-Out and Heterogeneous Integration", "Packaging with Additive Manufacturing for Harsh Conditions", and "Modeling and Characterization of Interfaces and Interconnects".

The Technology Corner exhibit area hosted more than 100 exhibitors. Exhibitors had multiple resources available within their virtual booth, offering virtual introductions, brochure materials, staff contact information, and an opportunity to submit inquiries and discuss directly with exhibit members.



Friday Luncheon and Raffle process presented by their sponsors.

ECTC Technology Corner.

Overall, the 72nd ECTC was an inspiring experience making us realize what we had lost during the two years of virtual ECTCs. The in-person participation energizes many of us in a way the online meetings cannot. The strength of the packaging community manifested itself by the relatively high number of attendees given the fact that several organizations still were restricting travel of their employees. We also had a very strong exhibitor presence, excellent sponsorship, and many high-quality technical presentations with excellent presentation attendance. The ECTC Executive Committee sincerely thanks all the attendees, exhibitors, and conference sponsors for their support as well as all the committee members and chairs who are volunteering their time to help organize the sessions and make ECTC such a success every year. Very special thanks also to our excellent event management team for bringing back the in-person reality flawlessly. See all the conference pictures at Flicker and keep in touch with the ECTC through LinkedIn.

The 73rd ECTC will be held at The JW Marriott Orlando Grande Lakes, Orlando, Florida, USA, May 30–June 2, 2023. Ibrahim Guven from Virginia Commonwealth University will be the General Chair of this conference. The Call for Papers and PDC Proposals will be available at www.ectc.net, and the abstract submission will close on October 10, 2022. So get those abstracts ready and submit them as soon as abstract submission opens.

See you all in Orlando in 2023!

IEEE Electronics Packaging Society (EPS) Malaysia Chapter

IEEE IEMT 2022 invites you to submit your work to the 39th IEMT 2022 that will be held in Le Meridian, Putrajaya, Malaysia. It is an international event organized by the IEEE-EPS, Malaysia Chapter, with co-sponsorship from IEEE Electronic Packaging Society (EPS). The IEMT typically attracts more than 400 attendees over the world. The last IEMT 2018 (Melaka, Malaysia) hosted 600 attendees, with 100 accepted papers and interactive presentation featured in 16 sessions. IEMT 2022 welcomes papers covering electronics packaging technology in diverse semiconductor market. This segment includes telecommunication, data center, automotive, EV, healthcare, aerospace, defense and others.

[https://www.iemt.com.my/]

Scope of Papers Solicited

Abstract should include original and previously unpublished, non-confidential and non-commercial information on new developments, technology and knowledge in the areas including, but not limited to those given below.

- Advanced Packaging—2D, 2.5D, 3.0D, Chiplets, WLCSP, FOWLP, FOPLP & HI
- Thermal/Mechanical/Electrical Simulation & Characterization
- Material & Processing
- Emerging Packaging—Opto, Medical, Nano Technology, Wearable Electronics
- Interconnections Technologies—TSV, μ-bump, hybrid bond, FC and embedded
- LED, MEMS, NEMS & Sensor Packaging & IoT
- IC Testing Technology
- Surface Mount Technology
- Quality, Reliability & Failure Analysis
- High-Speed, Wireless & Components

Keynote Speakers

Prof. Chris Bailey
Director of Computational Mechanics and Reliability Group
University of Greenwich

Mr Chew CH
Senior Director
OnSemi

Mr Terrence Tan
Senior Principal Engineer,
Manufacturing and Product Engineering
Intel

Dr.Veer Dhandapani
Senior Director of Product Development
NXP Semiconductors

Mr. Laurent Herard
Group VP—Head of Back End Manufacturing and Technology R&D
STMicroelectronics

Bernhard Knot
Head of Backend Innovation
Infineon

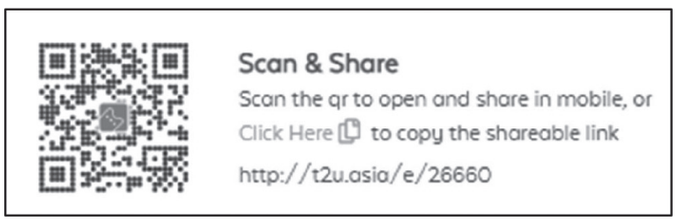
E. Jan Vardaman
President and Founder of TechSearch International, Inc

Rolf Aschenbrenner
Deputy Director and Head of SIIT
Department
Fraunhofer Institute (IZM)

https://www.iemt.com.my/program/iemt2022-keynotes/

Conference Registration

IEMT 2022—39th International Electronics Manufacturing Technology Conference 2022



http://t2u.asia/e/26660

If you have any questions, contact:
Conference Secretariat
E-mail: iemtmalaysia@gmail.com
Conference Web: https://www.iemt.com.my/

Top Conference Papers Based on Usage

2021 IEEE 71st Electronic Components and Technology Conference (ECTC)

(June 1–July 4, 2021)

Wafer Level System Integration of the Fifth Generation CoWoS®-S with High Performance Si Interposer at 2500 mm^2
P. K. Huang; C. Y. Lu; W. H. Wei; Christine Chiu; K. C. Ting; Clark Hu; C.H. Tsai; S. Y. Hou; W. C. Chiou; C. T. Wang; Douglas Yu

Die Embedding Challenges for EMIB Advanced Packaging Technology
Gang Duan; Yosuke Kanaoka; Robin McRee; Bai Nie; Rahul Manepalli

Heterogeneous Integration of a Compact Universal Photonic Engine for Silicon Photonics Applications in HPC
H. Hsia; C.H. Tsai; K.C. Ting; F.W. Kuo; C.C. Lin; C.T. Wang; S.Y. Hou; W.C. Chiou; Douglas C.H. Yu

InFO_oS (Integrated Fan-Out on Substrate) Technology for Advanced Chiplet Integration
Y. P. Chiang; S. P. Tai; W.C. Wu; John Yeh; C. T. Wang; Douglas C. H. Yu

SoIS- An Ultra Large Size Integrated Substrate Technology Platform for HPC Applications
Jiun Yi Wu; Chien-Hsun Chen; Chien-Hsun Lee; Chung-Shi Liu; Douglas C. H. Yu

2021 20th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(June 1–4, 2021)

The effectiveness of heat extraction by the drain metal contact of β-Ga2O3 MOSFETs
Samuel H. Kim; Daniel Shoemaker; Bikramjit Chatterjee; Kelson D. Chabak; Andrew J. Green; Kyle J. Liddy; Gregg H. Jessen; Samuel Graham; Sukwon Choi

Hybrid Two-Phase Cooling Technology For Next-Generation Servers: Thermal Performance Analysis
Raffaele L. Amalfi; Francois P. Faraldo; Todd Salamon; Ryan Enright; Filippo Cataldo; Jackson B. Marcinichen; John R. Thome

Package-Level Integration of Liquid Cooling Technology with Microchannel IHS for High Power Cooling

Je-Young Chang; Devdatta Kulkarni; Ravi Mahajan; Michael Jorgensen; Nick Neal; Rich Dischler; Aravind Dasu; Sandeep Ahuja; Rajiv Mongia

Hybrid Electric Aircraft Thermal Management: Now, New Visions and Future Concepts and Formulation
Terry J. Hendricks; Calin Tarau; Rodger W. Dyson

Heat Spreading and Heat Removal Needs of a Novel Power Electronics Package with Integrated Cooling
Ahmet Mete Muslu; Ryan Wong; Vanessa Smet; Yogendra Joshi

2021 IEEE 23rd Electronics Packaging Technology Conference (EPTC)

(December 1–30, 2021)

High Reliability Solution of 2.5D Package Technologies
Hsin Jou Lin; Vito Lin; Joe Lin; Ying Ju Lu; David Wang; Yu Po Wang

Cu CMP Dishing in High Density Cu Pad for Fine Pitch Wafer-to-Wafer (W2W) Hybrid Bonding
HongMiao Ji; King-Jien Chui

EPTC 2021 Invited Technology Talk: Roadmap Based on Holistic Understanding of Thermo-Mechanical Challenges from Package to System to Maximize Silicon Performance
Gamal Refai-Ahmed; Suresh Ramalingam; Tahir Cader; Jason Strader; Jari Huttunen; Anthony Torza; Srikanth Rangarajan; Bahgat Sammakia; Vadim Gektin; Hussam Kabbani

Fan-Out Embedded Bridge Solution in HPC Application
Shuai-Lin Bradley Liu; Nicholas Kao; Teny Shih; Yu-Po Wang

Wafer-to-Wafer Hybrid Bonding Challenges for 3D IC Applications
H. Y. Li; Hong Miao Ji; Alfred Neo Siang Kiat; Masaya Kawano

Upcoming Conferences

Dear Members and Patrons of the IEEE Electronics Packaging Society,

As always the health and safety of our members and participants is our first priority. Please know that our thoughts are with those affected by the COVID-19 outbreak.

We will continue to closely monitor the developments related to this pandemic and work diligently with the IEEE and our conference organizing committees worldwide on our preparedness. Please reference the IEEE MCE Health and Safety page for the latest information: https://ieeemce.org/event-health-safety/

Before traveling to any EPS sponsored conference, we recommend that you stay informed of any information your local health agencies and those at the conference location may make available and take reasonable precautions to protect yourself.

2022 23rd International Conference on Electronic Packaging Technology (ICEPT)
Dalian, China
Aug 10, 2022–Aug 13, 2022

2022 IEEE International Workshop on Integrated Power Packaging (IWIPP)
Grenoble, France
Aug 24, 2022–Aug 26, 2022

2022 IEEE 9th Electronics System-Integration Technology Conference (ESTC)
Sibiu, Romania
Sep 13, 2022–Sep 16, 2022

2022 44th Annual EOS/ESD Symposium (EOS/ESD)
Reno, NV USA
Sep 18, 2022–Sep 23, 2022

2022 13th International Conference on Computing Communication and Networking Technologies (ICCCNT)
Kharagpur, India
Oct 3, 2022–Oct 5, 2022

2022 IEEE 31st Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
San Jose, CA USA
Oct 9, 2022–Oct 12, 2022

2022 IEEE 39th International Electronics Manufacturing Technology Conference (IEMT)
Putrajaya, Malaysia
Oct 19, 2022–Oct 21, 2022

2022 IEEE 67th Holm Conference on Electrical Contacts (HLM)
Tampa, FL USA
Oct 23, 2022–Oct 26, 2022

2022 17th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)
Taipei, Taiwan
Oct 26, 2022–Oct 28, 2022

2022 IEEE CPMT Symposium Japan (ICSJ)
Kyoto, Japan
Nov 9, 2022–Nov 11, 2022

2022 IEEE 24th Electronics Packaging Technology Conference (EPTC)
Singapore
Dec 7, 2022–Dec 9, 2022

2022 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)
Urbana, IL USA

Abstracts Due: September 5, 2022

ITherm 2023
ORLANDO, FL

22nd Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems

May 30 – June 2, 2023

Important Dates

Abstract Deadline:	**Sept. 5, 2022**
Notification of Acceptance:	Oct. 17, 2022
Draft Paper Submission:	Dec. 19, 2022
Reviews Returned:	Feb. 6, 2023
Final Paper Submission:	Mar. 6, 2023

Call for Abstracts

The IEEE ITherm Conference is the leading international conference for scientific and engineering exploration of thermal, thermomechanical and emerging technology issues associated with electronic devices, packages, and systems. ITherm 2023 will be a physical conference held along with the 73rd ECTC. Joint ITherm/ECTC registrations will be available at a significant discount. All abstracts are followed by full papers to be peer reviewed and published in the IEEE Xplore ITherm proceedings. Student first authors will have the opportunity to apply for ITherm travel grants, covering registration and 2 or 3 night stay at the conference hotel, in order to participate in the Student Poster and Networking Session. ITherm 2023 will also feature keynotes by prominent speakers, vendor exhibits, panel discussions, invited technology talks, ECTC/ITherm joint networking events and short courses, an art-in-science exhibition, and a student design competition. Original papers are solicited in the following areas of interest:

Component-Level Thermal Management
- 3D Packaging & Heterogeneous Integration
- Package-Integrated Thermal Management
- Embedded Cooling
- Hotspot and Impingement Cooling
- Thermal Interface Materials and Heat Spreaders
- Thermoelectric and Peltier Devices
- Heat Pipes, Vapor Chambers and Thermosyphons
- Single / Two-Phase Cold Plates and Heat Sinks
- RF and Power Electronics
- LEDs, Photovoltaics, and Optoelectronics
- Thermal Management of Electric Machines
- Pulsed Power Dissipation

System-Level Thermal Management
- Air Cooling Techniques and Heat Exchangers
- Liquid Cooling Solutions
- Immersion Cooling and Refrigeration
- Pumps, Compressors, Fans and Blowers
- Phase Change Materials
- Automotive, Batteries and Thermal Storage
- Mobile and Internet of Things
- Telecommunication Systems
- Space and Aerospace
- Data Center Thermal Management
- Thermal Management in Electric Aircraft
- Modeling of Complex Thermal Systems
- Next-Gen Electronics Systems Co-Design

Mechanics & Reliability
- Thermo-Mechanical Modeling and Simulation
- Mechanics and Reliability of Solder Joints and Interconnects
- Materials Characterization, Processing, and Models
- Failure Mechanics, Fatigue, and Damage Modeling
- Measurement of Deformations, Strains and Stresses
- Shock, Drop and Vibrational Analysis
- TSV / 3D Reliability and Packaging
- Mechanics in Assembly and Manufacturing
- Applied Reliability and Failure Analysis
- Process-Structure-Property Relations / Multi-Scale Analyses
- Accelerated Stress Testing and Modeling
- Lifetime Prognostics and Condition Monitoring

Emerging Technologies and Fundamentals
- Boiling, Evaporation, and Condensation
- Convection in Microchannels, Microgaps, and Jets
- Pulsating / Oscillating and Non-Conventional Heat Pipes
- Nanoscale and Transistor-Level Thermal Transport
- Novel Materials and Fabrication Techniques
- Measurement and Diagnostic Techniques
- Numerical Methods, Nano-to-Macro Scale
- Experimental Methods, Nano-to-Macro Scale
- Prognostic Health Management and Reliability Analysis
- Wearable, Flexible, and Printed Electronics
- Additive Manufacturing
- Silicon Fabrication for Thermal Management Devices
- Predictive Analytics and Machine Learning

ITherm provides an opportunity for industrial and university participation in the form of financial support to ITherm 2023. All contributors will be given strong recognition both onsite and in the conference materials.

Join the ITherm LinkedIn Group
https://www.linkedin.com/groups/8650280

General Inquiries:
Dr. Milnes P. David, Communication Chair
milnespd@us.ibm.com

Program Inquiries:
Dr. Ashish Gupta, Program Chair
ashish.x.gupta@intel.com
Prof. Amy Marconnet, Vice Program Chair
amy.marconnet.itherm@gmail.com

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IEEE ELECTRONICS PACKAGING SOCIETY

EPTC 2022

24th Electronics Packaging Technology Conference

7th – 9th Dec 2022, Singapore

IEEE EPS Flagship Conference

3RD CALL FOR PAPERS

ABOUT EPTC

The 24th IEEE Electronics Packaging Technology Conference (EPTC2022) is an international event organized by the IEEE RS/EPS/EDS Singapore Chapters and co-sponsored by the IEEE Electronics Packaging Society (EPS). Since its inauguration in 1997, EPTC has been established as a highly reputed international electronics packaging conference and is the EPS flagship conference in the Asia-Pacific Region. It aims to cover the complete spectrum of electronics packaging technology. Topics include modules, components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, LED, IoT, 5G, emerging technologies, 2.5D/3D integration technology, smart manufacturing, automation and AI. EPTC2022 conference will feature keynotes, technical sessions, technology talks, an exhibition and networking activities.

The EPTC technical program Committee, with more than 100 experts from diverse technology areas in semiconductor packaging, is committed to creating an engaging technical program for the international packaging community. Technology Corner Exhibits will supplement the technical program, which will allow leading companies to exhibit their latest technologies and products. Last year, the 23rd EPTC was conducted on a virtual platform due to the pandemic. More than 496 attended from more than 30 countries worldwide, with 150 video presentations across 26 technical sessions. This year the conference will be in-person. Currently, fully-vaccinated persons need not be tested to enter Singapore, and no quarantine period is necessary.

CONFERENCE TOPICS

You are invited to submit abstract(s) on new research findings and developments in the following packaging categories:

Advanced Packaging: Flip-chip, 2.5D & 3D, embedded passives & actives on substrates, chiplets, System in Packaging, embedded chip packaging technologies, panel-level packaging, RF, microwave & millimeter-wave, Power and Rugged Electronics Packaging, advanced packaging solutions for 5G, IoT, cloud computing, autonomous vehicles, antennas, sensors, power transfer, EM shielding, RF to THz communications.

TSV/Wafer Level Packaging: Wafer-level packaging, embedded chip packaging, 2.5D/3D integration, Silicon, SiC & Glass interposer, CoWoS, FoCoS, InFo, eWLB, Embedded Multi-die Interconnect Bridge (EMIB), bumping technologies.

Interconnection Technologies: Au/Ag/Cu/Al wire-bond / wedge bond technology, Flip-Chip & Cu pillar, solder alternatives, Cu to Cu, wafer-level bonding & die attachment (Pb-free), Fan-out, panel-level, chiplets, SiP, micro-bump, high I/O thermo-compression/hybrid bonding, fine-pitch/multi-layer RDL, printable interconnects, conductive/ non-conductive adhesives, low-temperature solder, interconnects design and technology for emerging applications.

Emerging Technologies: Novel and unique packaging and material technologies for soft and intelligent packaging, flexible hybrid electronics, implantable biosensors and bioelectronics, packaging for extreme harsh environments, green/bio-resorbable packaging, packaging of MEMS & NEMS, packaging for wide bandgap devices, quantum computing, electro-optical integration, AI, ML, packaging sensing and communication.

Materials and Processing: Photoresist, polymer dielectrics, solder, die-attach, underfill, substrates, lead-frames, materials for wafer & panel-level packaging; harsh environments, wafer bonding/debond materials, emerging electronic materials & processes, novel solder metallurgies, molding compounds, thermal interface materials, advanced wire-bonding, conductive adhesives, PCB for advanced packaging, assembly processes using newer materials. Advances in process technology for large/ultra-large packages (SiP, SIM, MCP), high power, high frequency 5G/RF packaging, TSV and 3D stacking – chip to wafer, wafer to wafer bonding, collective die to the wafer.

Assembly and Manufacturing Technology: Embedded/hybrid package manufacturing processes, warpage control and management in board-level assembly, thin die/package handling and assembly advance in flexible and printed electronics, large/ultra-large package (SiP, SIM, MCP) integration and processing, thermally enhanced packaging and assembly challenges. advances in additive manufacturing for packaging substrates, equipment parts, chiplets – assembly challenges, materials and integration

Electrical Simulation & Characterization: Power plane modelling, signal integrity analysis by simulations and characterization, 2D/2.5D/3D package level high-speed signal design, characterization, and test methodologies.

Mechanical Simulation & Characterization: Thermal-mechanical interaction study, moisture, fracture, fatigue, dynamic impact modelling and characterization, process modelling.

Thermal Characterization & Management: Thermal characterization and simulation, component, system and product level thermal management and characterization.

Quality, Reliability & Failure Analysis: Silicon, component, board and system-level reliability assessment, interfacial adhesion, accelerated testing, failure characterization.

Advanced Optoelectronics and Displays: Design, simulation, interconnection , packaging, integration and materials for optoelectronics and novel displays - micro/mini/nano LED, foldable and flexible displays, Augmented Reality and Virtual Reality and wearable displays, Si and III-V photonics, optical sensors, interconnects, interposers, quantum device packaging, photonics SiP, free-space optical communications, waveguide, automotive photonics, 3D sensing, optoelectronic fiber coupling assembly, materials and reliability, fiber optic transceivers.

Smart Manufacturing and Packaging Equipment Technology: Smart Manufacturing in packaging, cycle time, data analytics, advanced metrology, Machine Learning, AI, and advanced equipment for assembly, packaging and handling.

IMPORTANT DATES

Online abstract submission start	April 20, 2022
Closing of abstract submission	**July 15, 2022**
Notification of acceptance	August 1, 2022

Please check http://www.eptc-ieee.net for the latest updates.

ABSTRACT AND PAPER SUBMISSION

You are invited to submit an abstract between 500–750 words long and clearly state the purpose, methodology, results (including data, drawings, graphs and photographs) and conclusions of the work. Additional details on abstract submission can be found on the EPTC website. Abstracts must be received by July 15, 2022. Your submission must be cleared by your management and co-authors and include the authors' affiliations and email addresses. All submissions should be made in English, either in pdf or MS Words format. Please select the appropriate technical committee per your abstract content from the drop-down list so that the right technical committee can evaluate your submission for acceptance. Accepted abstracts will be notified for the full-paper submission with instructions for publication by August 1, 2022. At the discretion of the technical committee, submitted abstracts may be considered for interactive presentation. The final manuscript for publication in the conference proceedings is due on September 10, 2022. The conference proceeding is an official IEEE publication, and the accepted papers that are registered and presented (oral & interactive) will be available in IEEE Xplore.

BEST PAPER AWARDS

Awards in the form of cash and certificates will be given to the best oral papers from Academia, Industry and Students. More details are available on the EPTC website.

CALL FOR TECHNOLOGY TALKS

We invite industry and academic experts in packaging R&D and manufacturing supplier industries (materials, equipment and services) on technology innovation, challenges, potential gaps, and product and services road map. More details are updated on the conference website, and technological talk proposals can be submitted at technicalchair@eptc-ieee.net.

CALL FOR PROFESSIONAL DEVELOPMENT COURSES

EPTC2022 would like to offer PDCs from the industry and academic experts in electronics packaging. More details are updated on the conference website, and proposals for PDC can be submitted at pdcchair@eptc-ieee.net.

CALL FOR EXHIBITION / SPONSORSHIPS

Detailed exhibition and sponsorship opportunities are available on the conference website. For enquiries, please email exhibition@eptc-ieee.net or sponsorship@eptc-ieee.net.

STUDENT TRAVEL GRANTS FOR EPTC

To widen the representation of female students and students from underrepresented countries in the electronic packaging field and to encourage these students to become members of the IEEE Electronic Packaging Society (EPS) and actively participate in the flagship conferences of the society, up to 6 Student Travel Grants will be offered for EPTC annually with at least two for female student authors and one for a student from a country historically underrepresented at EPTC.

Financial: Each intracontinental student would have expenses related to travel to the conference reimbursed up to US$1500, and each intercontinental student would have expenses related to travel to the conference reimbursed up to US$2100. Economy air travel would be an allowable expense, as would hotel lodging and the conference student registration fee, although the student registration fee would not be waived. Students who are not members would be required to join, but the society would reimburse their first year's dues as a travel expense.

Judging: Abstracts submitted with a student as the first and presenting author would be evaluated and ranked by the respective conference's technical program committee, and the top 15 abstracts for EPTC would be invited to submit an extended abstract or full paper. The awards committee would then review and rank order the submitted extended abstracts or full papers and notify the winners of their selection for the award.

Recognition: Winning students would be recognized in the advance program and at the awards luncheon ceremony.

Affiliate Membership Subsidy Program at EPTC

With the Affiliate Membership Subsidy Program (AMSP), non-member conference registrations will be offered an EPS affiliate membership for the following year at no cost. Any non-IEEE member registrant who wishes to take advantage of this will be required to submit a membership application to IEEE in the normal way, and EPS will cover the cost of the affiliate membership once the application is approved, at the cost of US$76.50 (EPS will waive its US$15 membership fee that would normally be included in the $91.50 total affiliate membership price). For more details please visit the EPTC website.

More details of conference, please visit EPTC2022 Website

Organized by

IEEE Singapore
RS/EPS/EDS Chapters

Chandra Bhesetti, PhD
General Chair
Institute of Microelectronics
generalchair@eptc-ieee.net

Prayudi Lianto, PhD
Technical Chair
Applied Materials
techchair@eptc-ieee.net

Sponsored by

IEEE ELECTRONICS PACKAGING SOCIETY

For more updates, please subscribe EPTC emailing

Selected Nanotechnology Advances in Interconnections, Power, RF and Sensor Integration - A View from ECTC 2022

Ting-Chia Huang (Kulicke and Soffa), Atom Watanabe (IBM), Alfred Zinn (Kuprion Inc),

Abdulhameed Abdal (University of California, San Diego)

and P. Markondeya Raj (Florida International University)

Nanopackaging can be defined as the packaging of devices and systems with nanoscale materials, structures, designs and process integration for improved performance, miniaturization, functionality, reliability and cost. Nanopackaging seeks to bridge the gap between nanoscale ICs, and the rest of the milliscale and microscale system components. Furthermore, all major aspects of future system integration: improved functional density, higher power densities and power efficiency, higher bandwidth with lower power, improved thermal management, sensor fusion and integration, and better reliability rely on Nanopackaging. These examples are illustrated in Fig. 1. ECTC 2022 showcased some of the nanotechnology advances that have been systematically addressing the challenges associated with heterogeneous integration. This newsletter article describes these advances in the respective categories.

Nanopackaging to Enable High-Bandwidth Computing - Fine-Pitch Cu Interconnections:

Driven by the trend of miniaturization and heterogeneous integration, a groundbreaking pad-to-pad assembly and interconnection technology beyond solder microbumps has been recognized as a critical building block for enhanced signal integrity and higher bandwidth at a smaller form factor. Nanotechnology has played a critical role to close the interconnections gap between the transistor level and packaging level and opens up new opportunities for designing the next generation of packaging materials. In this year's ECTC, direct hybrid Cu to Cu bonding has achieved a lot of attention because of its ability to enable BEOL-like vertical interconnections on a packaging level with nanoscale bonded layers.

Direct hybrid Cu-to-Cu bonding with dielectrics (e.g., TEOS, SiCN and SiOx) has been widely adapted by the memory manufacturers for a projected >8x die stacking. At this scale, the power delivery and thermal management have become a bottleneck with existing microbumps due to the elongated chip-to-chip interconnections and inferior thermal conductivity of underfill material. SK Hynix and Samsung have both demonstrated a relatively mature Wafer-to-Wafer (W2W) hybrid bonding for DRAM application, where a nanoscaled smooth dielectric along with a precisely-controlled Cu dishing (< 5 μm) achieved by chemical mechanical polishing (CMP) is considered as the main enabler of void-free interconnections. Though the adaptation of hybrid bonding to Die to Wafer (D2W) is considered more challenging, Samsung has successfully demonstrated a 12-Si stack D2W hybrid bonding with a 20% reduction of thermal resistance compared to the state-of-the-art microbump. This year, we also found that electron backscatter diffraction (EBSD) and high-resolution transmission electron microscopy (HR-TEM) are widely used to confirm the Cu grain growth across the bonded interface. To provide a more systematic approach to correlate the electrical design, the hybrid bonding conditions and the resulting performance, Applied Materials published a modeling platform, Materials to Systems Co-optimization (MSCO^{TM}), to capture the effect of process variables (e.g., CMP and misalignment) on the insertion loss and electromigration reliability. In the electromagnetic simulation, a 50 nm contact resistance layer was applied to model the bonded interface. The insertion loss at high frequency can then be predicted by altering the permeability of this thin layer.

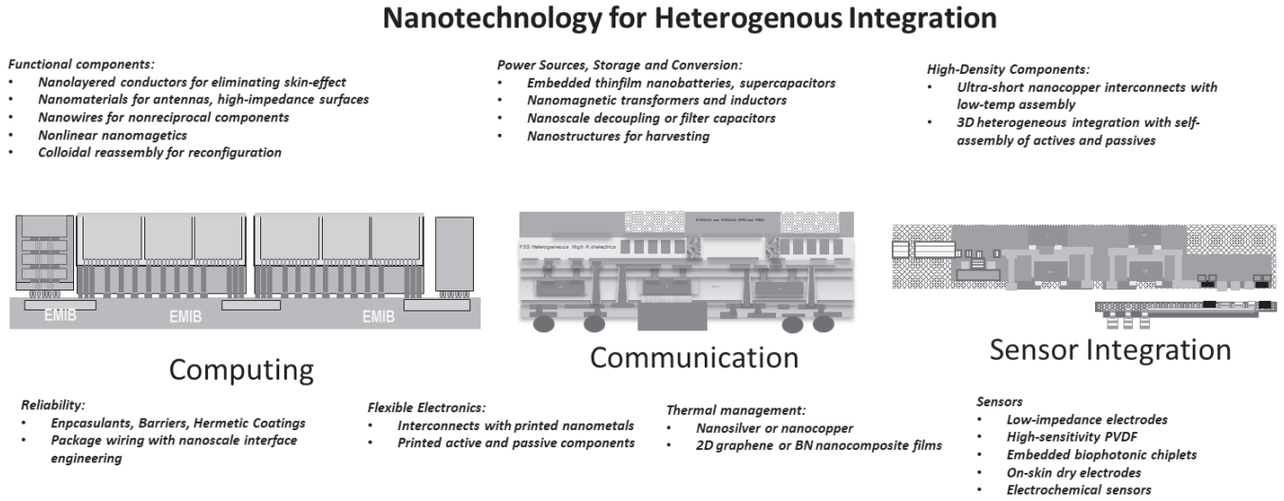


Fig. 1: Selected nanotechnology solutions for advancing future packaging (the left-side figure on Computing is courtesy of Ravi Mahajan (Intel)).

While the hybrid bonding technology continues to advance, some intrinsic limitations still need to be addressed before it can be extended beyond the 3D stacking. For instance, the thermal budget typically needed for post-annealing is significant, a nonuniform copper density from the routing design creates topographical variation after the CMP process. A highly rigorous roughness requirement of less than 1 nm is desired for a high bonded strength. In this year's ECTC, nanotechnology has emerged as a possible solution to the aforementioned challenges [1-6]. Chiu et al., from Industrial Technology Research Institute (ITRI) has demonstrated a low-temperature Cu-to-Cu bonding using nanocrystalline Cu (nc-Cu) [1]. The nc-Cu with 13 nm grain size was deposited by PVD with an overall film thickness of 2 μm. The final assembly was then completed with a pre-bonding under vacuum at room temperature followed by low-temperature annealing at 150 °C for 1 h. The paper from Zhang et. al. provided a thorough guideline of an ideal electroplated copper tailored for hybrid Cu bonding [2]. By using a highly engineered electrolytic plating Cu formula, a nanograined Cu with a grain size of 100±10 nm has demonstrated multiple desired properties, such as a stable as-plated microstructure up to 153 days at room temperature, a high percentage of (111) preferred grain orientation, a 7 times faster grain growth rate at 120 °C, and the compatibility to standard BEOL geometry. Though the fundamental mechanism that correlates the electrochemistry and metallurgical microstructure still remains unclear, the grain engineering at the nanoscale is anticipated to be the core technology for the next advancement in hybrid bonding. For direct hybrid Cu to Cu bonding, a precisely-controlled Cu recess or dishing after CMP is essential to achieve a void-free bonded interface. A 3-5 nm Cu recess relative to the dielectric surface is typically desired; however, it is harder to achieve at finer Cu pads. With an insufficient Cu recess, the Cu thermal expansion will delaminate the pre-bonded dielectric during the post-annealing step. TEL Technology Center proposed a cyclical wet atomic layer etching method, which includes two key alternating steps. First, an insoluble, self-limiting Cu passivation layer is formed in the complexing solution; and second, the newly formed Cu passivation layer is selectively dissolved in the dissolution solution. A well-controlled etching rate of 0.26 nm per cycle, corresponding to 1 nm per minute, was demonstrated as a promising downstream process to control the Cu recess after CMP.

Copper that is oriented in <111> direction and nanotwinned has shown promise for low-temperature bonding at 150 – 200 ºC even in mild vacuum of 10^{-4} to 10^{-3} torr. The enhanced surface diffusivity results in faster bonding, and was of specific interest at ECTC 2022 [3-4]. Beyond the typical Cu dielectric bonding, nanotechnology was used to engineer the bonding interfaces for interconnections

and assembly. Fang et. al. from Semiconductor Technology Innovation Center Corporation showed the potential of using Au nanoparticles (NPs) for Cu surface modification [5]. The Au NPs were first deposited onto Cu with high-pressure magnetron sputtering. The Au NP deposition not only passivates the underneath Cu but also reduces the surface roughness caused by Cu electroplating, and more importantly, accelerates the Au-to-Au interdiffusion to form the physical joints. With the Au NP intermediates, direct bonding can be achieved at 200 °C for 3 minutes even with a surface roughness of 18 nm, under a pressure of 30 MPa without post-annealing. Fraunhofer IZM has demonstrated nanoporous Au (NPG) as a promising replacement for existing Cu hybrid bonding for wafer-level packaging [6]. The NPG was fabricated by dealloying the Ag from electroplated Ag with 20-25 at% Au, where wet etching or plasma etching could be applied. In this paper, 15-100 μm bump sizes were fabricated and analyzed with a most aggressive test vehicle consisting of a 1 μm diameter NPG bump at 1.8 μm pitch. The assembly was successfully achieved with a 60x60 μm^2 bump size at 150°C bonding temperature and 10 MPa pressure. The as-bonded shear strength is 10-15 MPa, which can be further enhanced to 30-35 MPa if a higher temperature post-annealing is applied to densify the nanostructure.

Nanopackaging for Sensor Fusion and System Integration with Flexible and Stretchable Substrates:

Growing market demand for wearable technology in health-monitoring applications has been driving key innovations in package integration of flexible electronics. Wearable health-monitoring technologies can be classified into many categories: 1) neural recording applications such as continuous biopotential recording for electrocardiogram (ECG) or electromyogram (EMG) tracking, 2) biophotonic monitoring for monitoring blood flow and oxygenation, 3) electrochemical monitoring for glucose, uric acid and other biomarkers such as sweat analytes, and 4) wearable imaging systems. However, as the functional demands grow for wearable electronics, so does the need for component integration for power telemetry, signal processing and wireless communication. The EPS HIR team reviewed the key building blocks for emerging health-monitoring and therapeutic systems a ECTC 2022. The ability to integrate power sources (thin batteries, RF induction and energy harvesting), sensors (chemical, electrical, optical and MEMS), RF (components and communications) and displays in thin flexible and comfortably wearable formats will be critical. Nanopackaging allows such seamless integration of sensors, signal processing and wireless communication – all in the smallest form-factor for unobtrusive electronics that are almost invisible as on-skin patches such as Band-aid®. Advanced component integration technologies with flex and fabric integration are the key enablers for this technology evolution. Nanosensor packaging is becoming critical to integrate new health-monitoring functions for continuous feedback to the user. This includes muscle function analysis without constraining the user. For example, two papers at ECTC 2022 highlight the use of use of EMG sensors to monitor defective muscle function. One of them by Hokoo Kim et al. (Georgia Tech), focuses on monitoring volumetric muscle loss (VML) through aerosol jet printing of graphene and polyimide stacks [7]. This can replace needle-type wired electrodes that are invasive, obtrusive, and restrict the behavior of the subjects. About 3.4 dB in muscle activity is shown between the healthy and injured muscles. These are then integrated with flexible or stretchable package substrates through a "soft" package for wearable health-monitoring functions. Low-impedance stretchable electrodes has always been a key focus at the IEEE-NANO conference, the flagship conference from IEEE Nanotechnology Council.

Nanopackaging for sensors has been enabling new wearable sensor patches with high sensitivity. Conducting polymers such as polymer poly(3,4ethylenedioxythiophene):poly(styrenesuflonate) (PEDOT:PSS) have been widely investigated for nanosensor applications due to their volumetric capacitance owing to their 3-D interpenetrated electronic and ionic structures. However, commercially available PEDOT:PSS are brittle and suffer from poor mechanical adhesion. Recent advances in organic

block copolymers such as poly(poly(ethylene glycol) methyl ether acrylate) (PPEGMEA) enable better stretchability of PEDOT:PSS to conform on the skin for surface electromyography (sEMG) [8]. A synthesized library of PEDOT with PSS(1)-b-PPEGMEA(x) by varying blocks (1-6) of PPEGMEA were tested for stretchability and conductivity. By increasing blocks of PPEGMEA, the stretchability of PEDOT:PSS increased at the expense of its electrical properties. Nevertheless, it was observed that the longer chain of PPEGMEA such as Block-6 outperform commercially available PEDOT:PSS as sEMG electrodes, owing to its elastic modulus match to the skin (~ 10 MPa). Moreover, Polat et al. (UCSD) demonstrated an ultrasensitive piezoresistive composite made from graphene, decorated with gold nanoislands, and spray coated with PEDOT:PSS for monitoring swallowing behavior of dysphagia [9]. The nanocomposite allows high resolution strain of 0.0001% and a strain gauge factor of 100 due to the increased scattering of metallic structures, piezoresistivity of graphene, and complementary conducting paths through PEDOT:PSS dough. The nanocomposite was packaged in poly(dimethylsiloxane) (PDMS) in different ratios to adhere to the human skin. Fig. 2 shows the epidermal sensor, scanning electronic micrograph (SEM) of gold nanoislands, and the synthesized PEDOT:PSS.

Liquid boluses with different volumes were tested to monitor the tensile strain from skin deformation during swallowing. Integrating the epidermal nanosensor with customized PCB allows real-time and remote monitoring of swallowing activities. This technology can replace the conventional technique used such as video fluoroscopy to monitor abnormal swallowing behaviors, requiring patient visitation and an experienced pathologist. However, due to the increase demand of wearable electronics, wireless communication and advanced fabrication methods are required to allow small form-factors of devices ensuring optimal usability and comfortability.

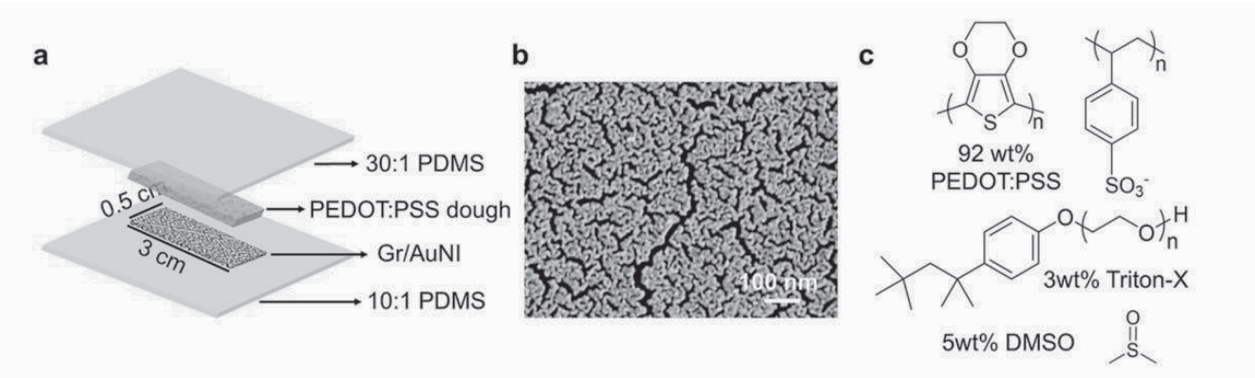


Fig. 2: (a) Epidermal nanocomposite sensor, (b) Gold nanoislands, (c) Chemical structure of modified PEDOT:PSS dough adapted from [8].

Sensor fusion and reliable seamless wireless connectivity with external electronic readers through simplified circuit topologies, advanced telemetry components and 3D package integration are identified as the main barriers to the success of this technology. The primary focus of the work in this area is to develop a new class of embedded-component flexible fan-out packages with RF or multiferroic telemetry, compliant piezoelectric transducers, and passive RF backscattering telemetry to address this barrier. A key advance by Hassan et al., at FIU is in the self-healing of interconnects with remote thermal actuation to mitigate crack growth and propagation during bending or other flex studies [10]. By modifying silver-polyurethane composites with a low-melting point thermoplastic such as PCL (polycapralactone), cracks are healed through a thermal actuation. The material flows into the cracks to heal the composites. This can be further extended with remote localized heat generation by loading the adhesives with ferrite nanoparticles that generate heat through irradiation from an external electromagnetic energy source at 30-100 kHz.

Laser ablation of copper traces with backside insulated polyimide (PI) attached to oxygen plasma treated PDMS introduce a novel approach to fabricate stretchable PCB designs that can easily conform to the skin. Packaging devices such as passive and active components are embedded in the elastomer in an island-bridge design by serpentine copper interconnects enhance the overall elastic stretchability in miniaturized form factors. Therefore, wireless communication through chip antennas or Bluetooth® allows seamless data transfer of EMG, ECG, EEG, or strain sensing for cloud computing with machine learning capabilities. New state-of-the-art wearable stretchable electronics will require advanced materials easily integrated into high-density prepackaged elastomers for on-demand and continuous monitoring of electrophysical signals. Stretchable packages have been evaluated by et al. at ECTC 2022 by Al-Haidari et al., (SUNY, Binghampton) with materials based on silver-elastomer composites that are further aided by designed serpentine structures [11]. In order to enhance the interconnection reliability between device pads and flexible or stretchable substrates, Stemmerman et al., from SunRay Scientific, in collaboration with SUNY Binghamton and AFRL, showed innovative magnetically-aligned anisotropic conductive epoxy to form stretchable vertical conducting paths between the bonding pads. Stretchability is achieved with innovative liquid metal network-forming nanoparticles that are passivated with a native oxide and organic moieties for processability. These passive networks rupture and result in the liquid metal particles (gallium alloys) to fuse and form the stretchable conductors.

Nanopackaging for Vertical Power Delivery:

Vertical power delivery is becoming a key enabler for enhancing computing performance. In order to improve the backside power delivery, nano through-silicon vias are processed from the backside power rails to the front-side metal wires to enable high-density electrical connections. In this work by Jourdain et al. (IMEC Belgium), various metallization schemes were studied to obtain the lowest resistance [12]. In a related work, TSVs were integrated with CNTs to further increase the power integrity at high frequencies [13]. Parasitic capacitance and signal losses were shown to be lower, particularly at higher frequencies of above 15 GHz. For lowering the impedance, it is also critical to vertically-integrate decoupling capacitors close to the processor, either inside the substrate as buried multiterminal components, on the landside as surface-assembled capacitors, or eventually in the active or passive silicon interposer as substrate-embedded capacitors. One key design avenue to increase the power density is to increase the surface area through nanoporous silicon and conformal dielectrics and counter electrodes that are typically deposited from ALD (atomic layer deposition). Capacitances of > 1 $\mu F/mm^2$ have already been demonstrated and the densities are projected to reach above 2.5 $\mu F/mm^2$. Planar capacitors provide multiterminal access to the electrodes. This aims to reduce the packaging inductance by cancelling inductance with the current propagation in opposite directions. Murata reported such silicon-based decoupling capacitors, as compared to MLCC, for high-frequency and high-speed circuit applications [14]. Their previous research work include tripod trench structures, enabling higher density and presenting several times smaller area than conventional passives. In ECTC 2022, Jatloui et al. described Murata's latest silicon process method based on 3D Nanoporous structures, which allows them to raise the effective density to greater than 1.3 $\mu F/mm^2$ while reducing the active capacitor area thickness and, as a result, the capacitor thickness to less than 50 μm. These devices have low ESL (few pH) and ESR (few m Ω), allowing them to obtain high-performance PDNs with low impedance over a wide frequency spectrum.

Nanopackaging for RF-to-THz applications:

For radio-frequency (RF), mmWave and THz-enabled 5G-6G systems, nanopackaging provides solutions in lowering conductor losses, on-chip and off-chip integration with CNT or graphene nanodevices, integrating functional components such as circulators and isolators with anisotropic nanomagnetic structures, nonlinear magnetic nanostructures for enhancing SNR, enhanced thermal management and

others. Nanopackaging will extend the individual nanodevices from graphene, CNT and Cd_3As_2, wide bandgap AlGaN/GaN or p-Diamond FETs to result in THz functional modules. The resulting modules will feature ultra-reconfigurable antennas, reflectarrays and intelligent reflective surfaces based on phase-change-materials, THz Emitters and Detectors amongst others. Graphene has emerged as a material suitable for THz plasmonic detection and emission applications due to its high carrier mobility and controllable carrier concentration. Because of their electron transport, graphene can attain high intrinsic current-gain cutoff frequencies and maximum oscillation frequency of > 100 GHz. However, graphene is susceptible to subsequent processes and interactions with adjacent layers creating a strong need for protection and encapsulation with thin inorganic ALD coatings. For example, a 10-nm alumina protection is known to lower the stress, improve thermal conductance, protect from subsequent plasma etching processes, and also improve performance. CNT arrays and graphene composites are also explored to create miniaturized shields that can avoid parasitic coupling and improve RF signal integrity. Recent papers also suggest that graphene composites can have shielding effectiveness beyond that of copper. Used as films or in fence-wall configurations, they can aid in reducing the bulkiness and weight. Examples from ECTC 2022 include metaconductor-based low-loss package-level interconnects, inkjet-printed nano-silver or nano-copper in-package traces, antenna structures with nanomagnetic materials and others. These are briefly described below.

The RF interconnects and components cause considerable conductor losses mainly due to the skin effect that forces high-frequency current to flow through only the outermost layer of a conductor. This reduces the effective cross-section of the conductor and results in higher RF ohmic resistance. One approach to address this issue is to deposit alternate non-ferromagnetic/ferromagnetic superlattice RF conductors, referred to as metaconductors [15,16]. Their low RF resistance have been demonstrated in a planar conductor architecture. A Cu/Co metaconductor based coplanar waveguide (CPW) transmission line structure has shown superior device performance to their monolithic Cu counterpart at 28 GHz, especially, for the mmWave applications,. In order to address the structural discontinuity problem at the edge of the conductor, the paper by Jeon *et. al.* (University of Florida, Gainesville) presented a Cu/Co cylindrical radial superlattice metaconductor bonding wire for millimeter wave applications [16]. Cylindrical radial superlattice (CRS) with Cu/Co is anticipated to be superior to that of Cu/NiFe metaconductors because of higher ferromagnetic resonance (FMR) from Co. A metaconductor coated bonding-wire based airlifted inductor with a one-port feed is designed, fabricated, and characterized. Surface roughness of 30 nm is employed for electrodeposition, which is fully compatible with normal MEMS and CMOS processes and thereby suppresses the roughness effect at high frequencies. At 10-45 GHz, the resistance and Q factor of an inductor composed of a 10 paired Cu/Co CRS metaconductor coated wire with a bonded wire diameter of 25 μm are evaluated, and a 70% resistance reduction and a 56% Q factor enhancement are demonstrated when compared to the solid Cu counterpart. Another paper from University of Florida and Cisco Systems Inc. reported parametric simulation study of a differential stripline with an insertion loss of less than 0.1 dB/mm at 28 GHz based on Copper/Cobalt metaconductor (Cu/Co-MC). Such low loss is hard to achieve using the latest low loss dielectric materials. At 28 GHz, 10 pairs of Cu/Co metaconductor layers exhibit an insertion loss 0.098 dB/mm, while monolithic copper counterparts exhibit an insertion loss 0.142 dB/mm.

Additively-manufactured conductor traces also benefit from advances in nanopackaging. Study on current carrying capacity of inkjet-printed nano-silver interconnect traces on a mesoporous PET substrate is reported by Abbara et al., from SUNY, Binghamton [17]. The low glass transition temperature of the substrate limits current handling, resulting in trace failures. The cross-sectional area and sintering procedure of nanosilver traces play a part in its current handling. The Joule heating effect changes the conductivity of the printed trace. Although the initial resistance of the laser-sintered samples is 2X lower than the oven

sintered samples in general, electrical current sintering can further reduce the resistance of oven-sintered samples. The current-induced sintering in the trace resulted in decreased trace resistance.

Nanomagnetic antennas has always attracted the attention in RF packaging because of its potential for miniaturization and enhanced bandwidth and efficiency. Sturim et al., from Michigan State University reported the development of two electrically tiny wire-folded Spherical Helix Antennas employing $MnFe_2O_4$ nanoparticle thick films [18]. This paper presented an air-filled helix antenna with 16 MHz of bandwidth at 1.108 GHz and 1.82 dBi gain. A magnetically filled helix antenna with the same volume showed enhanced bandwidth and miniaturization by lowering the frequency. This paper demonstrated the utility of magnetic nanocomposites in additive manufacturing.

Nanopackaging for Thermal Management:

Lack of energy-efficient and miniaturized Power Amplifiers in mmWave and THz bands escalates the need for thermal management. In order to address this issue, nanopackaging traditionally has led to key die-attach solutions with nanosilver paste, and recently nanocopper paste. The advent of 2D materials such as graphene and boron nitride nanosheets has further increased the options, as shown by Sun et al. from Georgia Tech [19]. These are briefly reported here. Ultra-large-scale integration of multifunctional high-power-electronic devices place rapidly increasing demands on the heat dissipation capabilities that can no longer be accommodated with current thermal management designs and materials. At last week's ECTC Packaging conference in San Diego, Zinn et al. from Kuprion Inc. presented a novel copper thermal via technology using Kuprion's engineered ActiveCopper [20]. This engineered copper material allows the direct formation and economic integration of large mm-size thermal vias into Printed Circuit Boards (PCBs), ceramic and glass substrates, thus maximizing heat dissipation through such insulating materials. Modeling conducted using ANSYS Icepack and input from measured materials properties provided evidence that such a design can achieve a heat transfer coefficient exceeding 3000 W/cm^2 °K with a bondline thickness of 10 μm and a measured thermal conductivity of up to 394 W/m°K. This ActiveCopper material enables rapid prototyping, is readily integrated into PCB manufacturing and scalable. The material can be applied via direct dispensing or large area-type stencil printing. The ActiveCopper material exhibits multiple unique features: 1) it comes in a paste form that flows easily allowing for rapid filling of holes of any shape, size and thickness; 2) it sinters to bulk Cu in air at normal reflow temperatures of 200 – 235°C but can operate at temperatures exceeding 300°C effectively permitting an unlimited number of subsequent reflow cycles. The material is easily processed using typical hot-pressing conditions as employed in standard FR4 PCB manufacturing. 3) After fusion, the resulting large via has converted into a solid copper coin. No other binders are left behind resulting in great thermal performance. 4) The material is fully RoHS compliant, safe to handle in air and stored at room temperature ready for immediate use. A further key feature is it's easy CTE tailorability over a wide range (3-17 ppm) enabling to match the CTE of Si, SiC and GaN. This new materials system enables many new applications and overcomes the limitations of electroplating and the expensive copper coin approach. One can directly bond and solder to the material; it exhibits exceptional reliability having passed over 4000 thermal shock cycles (5-10 sec air-to-air transition) at -55 to +125 °C. Due to the perfect CTE matching with FR4, no cracking or delamination has been observed. The large thermal via application for PCBs is currently being transitioned into full scale production with a large PCB manufacturer. Development of formulations for the filling of small vias (25-60 micron) in glass substrates are under way and preliminary tests revealed very promising results. In this case, processing is carried out without pressure or vacuum using standard reflow oven curing in a nitrogen atmosphere. Again, the ActiveCopper material has been engineered such that it closely matches the CTE of the respective glass substrates to avoid any thermomechanical stresses for high reliability and long life.

Summary

Nanotechnology will play a key role in realizing future heterogenous integration for all classes of products including high-performance computing, mmWave to THz communications and sensor fusion and networks for health-care, security, automation and control. ECTC 2022 had several papers showing several examples of Nanopackaging to address basic research barriers in the area of hybrid bonding with BEOL geometries for off-chip interconnections, vertical power delivery for low-impedance interconnects from backside power rails to SoC, advanced nanosensors and integration, mmWave components, and thermal management. Although, packaging is today at microscale, these solutions with nanomaterials, nanostructures, nanoscale designs and processes will eventually pave way for future packaging at nanoscale, leading to nanopackaging of devices for true nanoscale heterogeneous integration.

REFERENCES

1. Wei-Lan Chiu, Low-Temperature Wafer-to-Wafer Hybrid Bonding by Nanocrystalline Copper, pp, 679-684, ECTC 2022.
2. Yun Zhang, All Copper Is Not Created Equal — Examples of Grain Engineering In Plating, pp. 851-855, ECTC 2022.
3. Jia-Juen Ong, Fabrication and Reliability Analysis of Quasi-Single Crystalline Cu Joints using Highly <111>-Oriented Nanotwinned Cu, pp. 1206-1210, ECTC 2022.
4. M.L. Huang, Role of (111) nanotwinned Cu on dissolution behavior and interfacial reaction in micro-scale nanotwinned Cu/Sn/Ni interconnects, pp. 883-88, ECTC 2022.
5. Fang, Jun-Peng, Low Temperature Fine-pitch Cu-Cu Bonding Using Au Nanoparticles as Intermediate, pp. 701-706, ECTC 2022.
6. Lothar Dietrich et al., Fabrication and Characterization of Nanoporous Gold (NPG) Interconnects for Wafer Level Packaging, pp. 873-882, ECTC 2022.
7. Hokoon Lim et al., Wireless Nanomembrane Electronics and Soft Packaging Technologies for Noninvasive, Real-Time Monitoring of Muscle Activities, pp. 769-773, ECTC 2022.
8. Blau, R. et al. Intrinsically Stretchable Block Copolymer Based on PEDOT:PSS for Improved Performance in Bioelectronic Applications. ACS Applied Materials & Interfaces 14, 4823-4835, doi:10.1021/acsami.1c18495 (2022).
9. Polat, B. et al. Epidermal Graphene Sensors and Machine Learning for Estimating Swallowed Volume. ACS Applied Nano Materials 4, 8126-8134, doi:10.1021/acsanm.1c01378 (2021).
10. Akeeb Hassan et al., Self-healing of Interconnect Cracks for Reliable and Defect-Free Smart Manufacturing of Flexible Packages, pp. 1556-1561, ECTC 2022.
11. Riyad Al-Haidari et al., Evaluation of an Anisotropic Conductive Epoxy for Interconnecting Highly Stretchable Conductors to Various Surfaces, pp. 1422-1429, ECTC 2022.
12. Anne Jourdain et al., Buried Power Rails and Nano-Scale TSV: Technology Boosters for Backside Power Delivery Network and 3D Heterogeneous Integration, pp. 1531-1538, ECTC 2022.
13. Bo-Zhou Liao et al., Multi-Layer Chips on Wafer Stacking Technologies with Carbon Nano-Tubes as Through-Silicon Vias and it's potential applications for Power-Via technologies, pp. 1811-1817, ECTC 2022.
14. Mohamed Mehdi Jatlaoui et al., , Multi-terminal Ultra-thin 3D Nanoporous Silicon Capacitor Technology for High-Speed Circuits Decoupling, pp. 908-913, ECTC 2022.
15. Hae-in Kim et al., Metaconductor Based Highly Energy Efficient Differential Striplines for 112 Gbps Data Bus with Sub 0.1 dB/mm Package Insertion Loss, pp. 903-907, ECTC 2022.
16. Saeyeong Jeon, et al., Cu/Co Metaconductor Based Highly Energy-Efficient Bonding Wires for next Generation Millimeter wave Electronic Interconnects, pp. 1442-1445, ECTC 2022.
17. El Mehdri Abbara et al., Current Carrying Capacity of Inkjet-Printed Nano-Silver Interconnects on Mesoporous PET Substrate, pp. 794-800, ECTC 2022.
18. Nicholas Sturim et al., Electrically Small Folded Spherical Helix Antennas Utilizing Thick Solution Cast Nanomagnetic Films, pp. 116-121, ECTC 2022.
19. Zhijian Sun et al., Large-Scale Production of Boron Nitride Nanosheets-Based Epoxy Nanocomposites with Ultrahigh Through-Plane Thermal Conductivity for Electronic Encapsulation, pp. 1282-1286, ECTC 2022.
20. Alfred A. Zinn, Large, High Conductivity Direct-Fill Copper Thermal Vias for High Power Devices, pp. 1238-1243. ECTC 2022.

Additively Manufactured Highly Integrated mm-Wave Packaging Structures

Yepu Cui[1], Kexin Hu[2], and Manos M. Tentzeris[3]
School of Electrical and Computer Engineering, Georgia Institute of Technology, USA
[1]yepu.cui@gatech.edu, [2]khu63@gatech.edu, [3]etentzeris@ece.gatech.edu

***Abstract*— Modern 5G, Internet of Things (IoT), and wearable devices require tons of features packed into a small, portable form factor. This brings significant challenges to both the design of the packaging and the manufacturing of the device. This is where additive manufacturing (AM) can play a critical role. AM is a technology which can deposit various of materials in both 2D and 3D manner to realize complex geometries with superior resolution, accuracy, and speed. Compared to traditional subtractive manufacturing methods such as milling and chemical etching, AM techniques only use the minimum amount of materials which can reduce the cost significantly, making it the ideal candidate for future "smart city" that promises to connect billions of devices in all different types of environments.**

AM also enables novel integration of structures that are un-realizable with traditional manufacturing techniques. With AM, fully featured electronic devices can be realized in a customized 3D multi-layer stack within a single package. This paper gives a review of additively manufactured highly integrated packaging structures that operate at 5G mm-wave frequencies.

I. Introduction

With the recent development in 5G and wireless technologies, our society is undergoing what is known as the forth industrial revolution, also known as the digital revolution. The forth industrial revolution highlights the advances in manufacturing technologies with full automation, high resolution, as well as great sustainability. Within this revolution, AM is becoming an innovatory tool for massively on-demand realization of electronic designs such as wireless sensors, antennas, microfluidics, energy harvesters, etc [1]–[4].

The combination of 3D printing and inkjet printing technologies forms the "hybrid printing [5]" technique which has great potential of introducing new and novel "smart" packaging designs that are difficult to implement using traditional technologies. Fig. 1 demonstrates a fully integrated 3D stacked module enabled by the hybrid printing technique. 3D printable low-loss polymer enables the realization of conformal substrates, through-package vias, smart encapsulates, microfluidic channels, as well as dielectric lenses. Inkjet printing technology can deposit conductive materials onto the 3D surfaces directly to realize interconnects, circuits, and EMI shielding layers. By combining various AM technologies, 3D intergrated designs with more complicated structures and functionalities can be realized in mm-wave frequencies for both 5G and IoT modules.

This paper provides a review of additively manufactured highly integrated packing structures that operate at 5G mm-wave frequencies including System on Antenna (SoA) integration, flexible system-on/in-package, as well as printed "smart" mm-wave encapsulants.

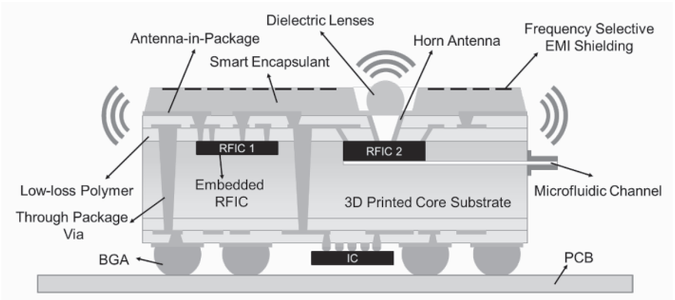


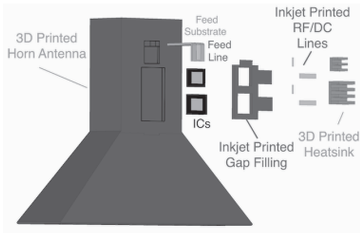
Fig. 1. Schematic of a fully integrated 3D stacked module enabled by 3D printing and inkjet printing techniques [6].

II. System on Antenna Integration

Fig. 2a shows a completed System on Antenna (SoA) design [7] that has a customized 3D printed antenna excited by integrated MMIC and inkjet printed feeding lines. The SoA design is a combination of traditional SoC/SoP and 3D printed antennas, which can provide the high intergration seen in SoC/SoP and high performance on-package antennas in a low-cost fashion. By embedding the ICs and circuits within the antenna, the entire RF system can be integrated into one single structure, eliminating the need for flanges, coax transitions, and cables so that the system size and losses can be reduced dramatically.

The proof-of-concept design of this SoA system is a radar transmitter that can be used for tracking applications. A Ku-band amplifier and a voltage controlled oscillator (VCO) are embedded into the 3D printed horn antenna to provide variable frequency control. The circuit is realized with inkjet printed conductive traces to enable trasmission of Ku-band signals. The full circuit design is shown in Fig. 2b.

The fabrication of this SoA design consists of four critical steps: 1) 3D print the antenna structure with integrated cavity housing for ICs, then metalize the structure. 2) Selectively metalize the microstrip antenna feed. 3) Install ICs, then inkjet print gapfill dielectrics, inkjet print RF and DC interconnects. 4) 3D print the heat sink structure for heat dissipation. The fabricated sample is shown in Fig. 2c and the measurement results are shown in Fig. 2d. The measurement demostrated solid received signals from the SoA with different tuning voltages. This SoA design demonstrates the versatility of AM



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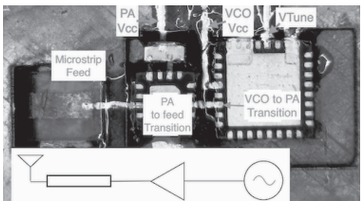

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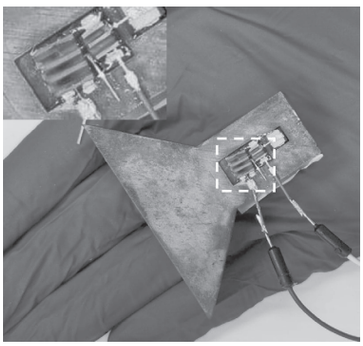

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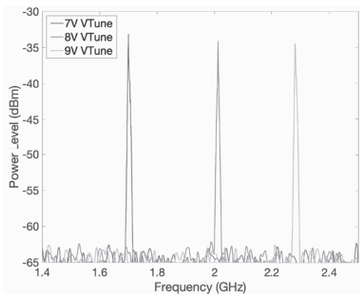


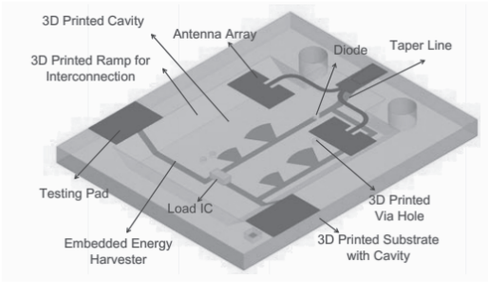
(d)

Fig. 2. (a) Exploded view of the of a SoA proof-of-concept topology, with the various components required. (b) Fully printed SoA with RF and DC inkjet printed lines and equivalent schematic. (c) The top view of the SoA module prototype with enlarged heat sink. (d) Received power level from the SoA, with different tuning voltage demonstrating system level applications [7].

that allows the designer to realize un-conventional geometry as integration layers for RF devices, that can enhance the system performance while reducing the size.

III. Flexible System-on/in-package

With the development of 3D printing technology, flexible materials such as hermo-plastic polyurethane (TPU), polypropylene (PP) for Fused Deposition Modeling (FDM) 3D printers, and Formlabs Flexible 80A, Formlabs Elastic 50A resin for Stereolithography (SLA) 3d printers are now



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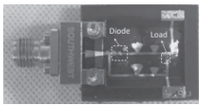

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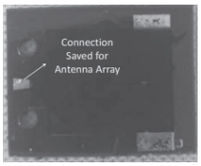

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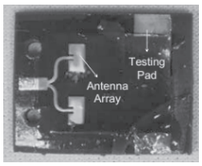


(e)

Fig. 3. (a) Flexible system that is demonstrated layer by layer beginning with (b) encapsulated inkjet printed support circuitry layout with radial stubs (c) integration of rectifying diode and load for measurement (d) encapsulation of integrated circuit and support circuitry (e) SoP antenna used at 26 GHz energy harvesting. [8]

becoming commercially available. When combined with inkjet printing technology, complex system-on/in-package design shown in Fig. 3 with embedded energy harvester, loading circuits, and antenna arrays can be realized in a flexible fashion [8]. This design utilizes non-planar interconnects across integrated circuits of various heights, with non-planar ramps enabling improved performance. The top of the structure contains inkjet printed on-package antenna that convers 5G mm-wave band from 24.4 GHz to 30.1 GHz. The embedded energy harvester eliminates the requirements for external batteries or super capacitors by collecting energy from the nearby 5G base stations. The integration of this full system in a flexible package enables compact electronic devices that can be ideal candidates for the next stage of wearables, where devices are integrated directly into the human body.

IV. Additively Manufactured "Smart" Encapsulants

Conventional IC die encapsulations utilize expoxy molding process that offers limited freedom for system in package integration. Mmwave packaging also requires compact structures with air cavities over the devices to minimize dielectric loading. These processes usually come with high cost and challenges in integration. Recent development on 3D printing technologies has shown the potential in solving packaging problems in a low-profile manner. 3D printer can directly build encapsulations onto front-end circuits with

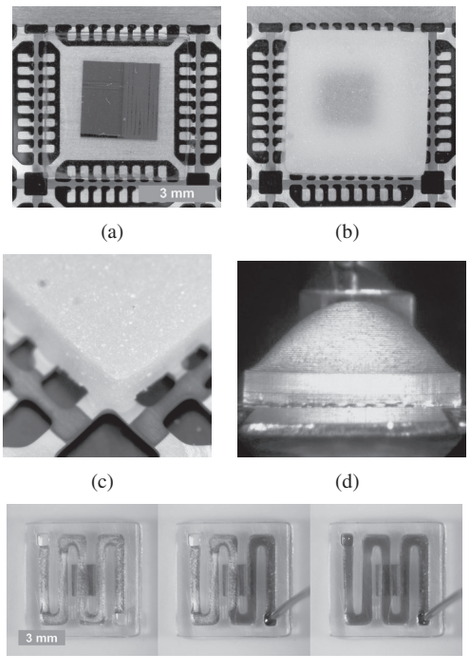


Fig. 4. 3D-printed die encapsulants on a metallic QFN leadframe: Vorex encapsulation (a) top view; (b) perspective view and (c) Porcelite encapsulant perspective view. Vorex encapsulant with (d) dielectric lens and (e) microfluidic network. [10]

customized shapes, spacing and dimensions. SLA printing as a widely accepted and low cost 3D printing technology, provides high resolution and low surface roughness, which also makes SLA printed materials excellent substrates for inkjet printing conductive traces [9].

Fig. 4 shows SLA printed encapsulants using Vorex and Porcelite materials over a 280mm thick silicon die package, that was attached to a metallic QFN by inkjet printed polymers [10]. The Vorex encapsulants including dielectric lens and microfluidic networks are demonstrated in Fig. 4 (d) and (e). A fully additively manufactured MCM module with a "smart" frequency selective surface (FSS) enabled encapsulation is shown in Fig. 5. The FSS encapsulation is only 0.2mm thick and is 1mm higher than the packaged device. It completely covers the circuits and leaves openings for external connections. The FSS pattern consists of 9 circular rings that were inkjet printed with silver nano particle ink to achieve EMI shielding. The measurement results of the integrated MCM with FSS encapsulation show that more than 18dB isolation is added at 24GHz compared to the case of no encapsulation, while the S21 remains the same for both cases. In addition, in this MCM design, inkjet-printed gap-filled interconnects were used, which easily connects the MMICs inside the 3D printed encapsulation to out-of-cavity circuits. Compared with traditional wire-bonding, the inkjet printed interconnects feature a more compact structure with lower parasitic loss and shorter loop length. These interconnects were inkjet printed with multiple layers of SU8 to fill the gaps and build bridges for inkjet printed silver traces. These highly-integrated novel packaging structures prove the on-demand reconfigurable nature of AM techniques for diverse packaging applications.

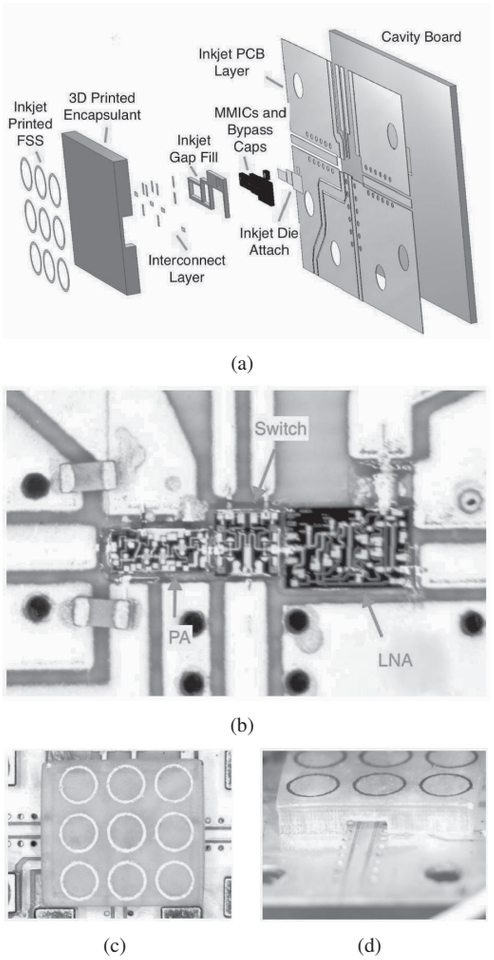


Fig. 5. (a) Exploded view of the complete encapsulated RF front-end MCM with an additively manufactured multilayer structure. (b) Non-encapsulated mm-wave front-end MCM fabricated using inkjet printing (c) 24-GHz FSS inkjet printed on top of the 3-D printed encapsulation. (d) Perspective image showing the cavity and the FSS-enabled "smart" encapsulation of the front-end MCM [11].

V. Conclusion

In this paper, various types of additively manufactured highly integrated packaging structures for 5G mm-wave frequencies are discussed. The capabilities of AM in System on Antenna (SoA) integration, flexible system-on/in-package, as well as printed "smart" mm-wave encapsulates demonstrate novel integration process with high performance and low cost, providing future solutions for 5G and B5G devices. The wide range of potential applications of AM in mm-wave packaging also sets the foundation for wearable biomonitoring, autonomous car implementations and reconfigurable intelligent surfaces up to sub-THz frequencies.

References

[1] K. Schmidt, B. Polzinger, M. Metry, S. Koppe, and A. Zimmermann, "Hybrid additive manufacturing by embedded electrical circuits using 3-d dispensing," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 11, no. 3, pp. 510–521, 2021.

[2] T. M. Hipolito, L. R. Rodrigues, G. C. da Silva, and E. G. del Conte, "Additive manufacturing of microfluidic devices," *IEEE Latin America Transactions*, vol. 14, no. 12, pp. 4652–4656, 2016.

[3] Y. Cui, S. A. Nauroze, R. Bahr, and E. M. Tentzeris, "3d printed one-shot deployable flexible "kirigami" dielectric reflectarray antenna for mm-wave applications," in *2020 IEEE/MTT-S International Microwave Symposium (IMS)*, 2020, pp. 1164–1167.

[4] V. Haseltalab, M. Dolen, U. Yaman, and C. Hoffmann, "Toward a simple design and manufacturing pipeline for additive manufacturing," *IEEE Access*, vol. 9, pp. 107 224–107 234, 2021.

[5] H. Jeong, Y. Cui, M. M. Tentzeris, and S. Lim, "Hybrid (3d and inkjet) printed electromagnetic pressure sensor using metamaterial absorber," *Additive Manufacturing*, vol. 35, p. 101405, 2020. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2214860420307776

[6] X. He, K. Hu, Y. Cui, R. Bahr, B. Tehrani, and M. Tentzeris, "Additively manufactured "smart" rf packaging structures: A quantum leap for on-demand customizable integrated 5g and iot modules," *IEEE Microwave Magazine*, vol. 8, 2022.

[7] X. He, Y. Fang, R. A. Bahr, and M. M. Tentzeris, "Rf systems on antenna (soa): a novel integration approach enabledby additive manufacturing," in *2020 IEEE MTT-S International Microwave Symposium (IMS)*, June 2020.

[8] T. Lin, S. N. Daskalakis, A. Georgiadis, and M. M. Tentzeris, "Achieving fully autonomous system-on-package designs: An embedded-on-package 5g energy harvester within 3d printed multilayer flexible packaging structures," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019, pp. 1375–1378.

[9] B. K. Tehrani, R. A. Bahr, W. Su, B. S. Cook, and M. M. Tentzeris, "E-band characterization of 3d-printed dielectrics for fully-printed millimeter-wave wireless system packaging," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*, June 2017, pp. 1756–1759.

[10] B. Tehrani, R. Bahr, D. Revier, B. Cook, and M. Tentzeris, "The principles of "smart" encapsulation: Using additive printing technology for the realization of intelligent application-specific packages for iot, 5g, and automotive radar applications," in *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)*, May 2018, pp. 111–117.

[11] X. He, B. K. Tehrani, R. Bahr, W. Su, and M. M. Tentzeris, "Additively manufactured mm-wave multichip modules with fully printed "smart" encapsulation structures," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 7, pp. 2716–2724, 2020.

Universal Chiplet Interconnect Express (UCIe)®: An open standard for developing a successful chiplet ecosystem

Dr. Debendra Das Sharma

Intel Senior Fellow, Co-GM Memory and I/O Technologies, Data Center and AI Group, Intel Corporation, Santa Clara, CA 95052, USA
Chair and Co-Founder of UCIe Consortium
debendra.das.sharma@intel.com

I. Introduction

Universal Chiplet Interconnect Express (UCIe)® [1] is an open industry standard interconnect, offering high-bandwidth, low-latency, power-efficient, and cost-effective on-package connectivity between chiplets. It addresses the compute, memory, storage, and connectivity needs across the entire compute continuum, spanning cloud, edge, enterprise, 5G, automotive, high-performance computing, and hand-held segments. UCIe offers a plug-and-play interconnect at the package level, enabling a designer to package chiplets from different sources, including different fabs, using a wide range of packaging technologies.

II. Motivation for On-Package Integration of Chiplets

Gordon Moore predicted the "Day of Reckoning" in his seminal paper where he posited "Moore's law" [1]: *"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."* We are past that inflection point. On-package integration of multiple dies has been widely deployed in mainstream volume CPUs and GP-GPUs [3].

There are many drivers for on-package chiplets. As die sizes keep increasing to meet the growing processing demand, they are exceeding the reticle limit and facing yield challenges in the advanced process nodes. Smaller chiplets connected on package helps designers overcome these challenges.

Lowering the overall portfolio cost with a time to market advantage is a compelling driver for deploying chiplets. For example, the compute cores shown in Figure 1 can be implemented in an advanced process node to deliver leadership power-efficient performance whereas the memory and I/O controller functionality may be reused from a design already deployed in an established process node. Such partitioning also results in smaller dies which results in better yield. It also mitigates IP porting costs which are increasing significantly for the advanced process nodes (Figure 2).

Another value add of chiplets is the ability to offer bespoke solutions. For example, one can choose different numbers of compute, memory, and I/O, and accelerator chiplets depending on the need of the segment. One does not need to do a different die design for different segments, lowering the product cost.

UCIe comprehends these usage models across market segments and is designed to transform the industry.

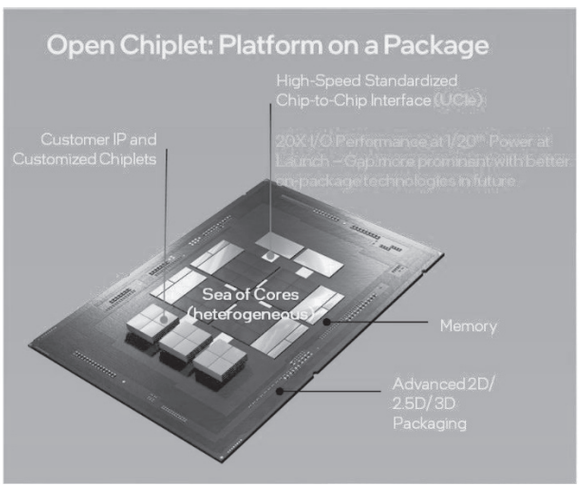


Figure 1: UCIe-based Open Chiplet Ecosystem: Platform on a Package

III. Considerations for an Ubiquitous Industry Standard

Figure 3 represents the necessary ingredients for a standard to be widely deployed, based on our experience in driving successful industry standards such as Peripheral Component Interconnect Express (PCIe)® and Computer Express Link (CXL)®.

An open industry standards body defining a specification is a critical component for wider deployment. Any company can join UCIe and member companies drive its evolution. Thus, companies can invest in the technology without worrying about the viability of the technology, like PCIe and CXL. Compelling key performance indicators (KPIs) catering to a wide range of usages is essential. It is also important to have a complete specification that comprehends all the layers of the stack for ensuring interoperability. As we will see later, UCIe meets these requirements. On-package integration of chiplets has

matured commercially across different manufacturing, assembly, and test companies. This maturity removes another obstacle for adoption.

UCIe is the result of industry leaders with expertise in chiplet integration working together to develop a common standard so that multiple chiplets from different sources can interoperate seamlessly. This will drive a thriving open chiplet ecosystem.

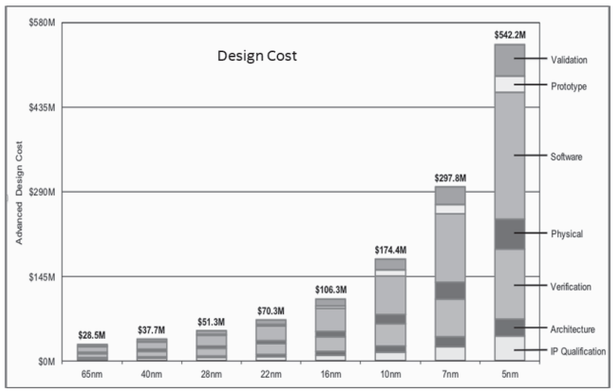


Figure 2: Design cost across different process nodes (Source: IBS, as cited in IEEE Heterogeneous Integration Roadmap)

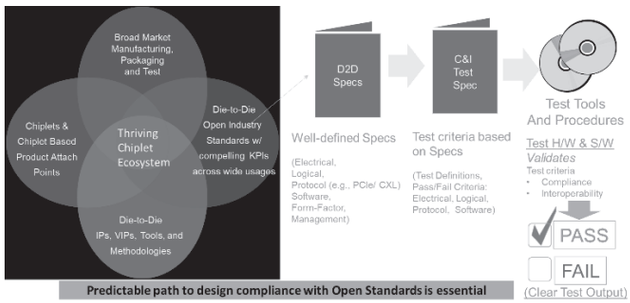


Figure 3: Ingredients of a successful and broad interoperable chiplet ecosystem

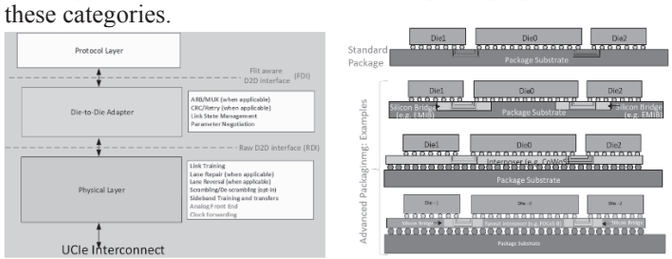
IV. Usage Models and KPIs targeted by UCIe 1.0 Specification

UCIe is a well-specified, layered protocol (Figure 4a). The physical layer is responsible for the electrical signaling, clocking, link training, sideband, etc. The Die-to-Die adapter provides the link state management and parameter negotiation for the chiplets. It optionally guarantees reliable delivery of data through its cyclic redundancy check (CRC) and link level retry mechanism. When multiple protocols are supported, it also defines the underlying arbitration mechanism. A 256-byte FLIT (flow control unit) defines the underlying transfer mechanism when the adapter is responsible for reliable transfer.

UCIe maps PCIe and CXL protocols natively [4] as those are widely deployed at the board level across all segments of compute. This is done to ensure seamless interoperability by leveraging the existing ecosystem where board components can be brought on-package. With PCIe and CXL, SoC construction, link management, and security solutions deployed in today's platform can be seamlessly transported to UCIe.

The usage models addressed by UCIe are comprehensive: data transfer using direct memory access, software discovery, error handling, etc., are addressed through PCIe/ CXL.io; the memory use cases are handled through CXL.Mem; and caching requirements for applications such as accelerators are addressed with CXL.cache. UCIe also defines a "streaming protocol" which can be used to map any other protocol such as a proprietary symmetric cache coherency protocol (e.g., Ultra Path Interconnect). Going forward, the UCIe consortium may innovate on protocols to cover new usage models or enhance existing ones.

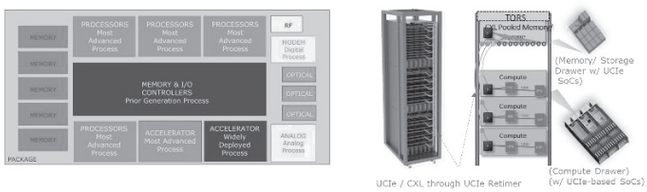
UCIe 1.0 supports two types of packaging, as shown in Figure 4b. The standard package (2D) is used for cost-effective performance. The advanced packaging is used for power-efficient performance. There are multiple commercially available options, some of which are shown in the diagram. UCIe specification embraces all types of packaging choices in these categories.



(a. Layering with UCIe) (b. Packaging Options: 2D and 2.5D)

Figure 4: UCIe : Layering Approach and different packaging choices

UCIe supports two broad usage models. The first is package level integration to deliver power-efficient and cost-effective performance, as shown in Figure 5a. Components attached at the board level such as memory, accelerators, networking devices, modem, etc. can be integrated at the package level with applicability from hand-held to high-end servers with dies from multiple sources connected through different packaging options even on the same package. The second is to provide off-package connecvity using different type of media (e.g., optical, electrical cable) using UCIe Retimers to transport the underlying protocols (e.g., PCIe, CXL) at the rack or even the pod level for enabling resource pooling, resource sharing, and even message passing using load-store semantics beyond the node level to the rack/ pod level to derive better power-efficient and cost-effective performance at the edge and data centers.



(a: Package level Integration) (b: Rack/ Pod level connectivity with UCIe Retimers)

Figure 5: Usage Models supported by UCIe: on-package integration as well as off-package connectivity with different media (e.g., optics, mmWave, electrical cable)

UCIe supports different data rates, widths, bump-pitches, and channel reach to ensure the widest interoperability feasible, as detailed in Table 1. It defines a sideband interface for ease of design and validation. The unit of construction of the interconnect is a cluster which comprises of N single-ended, unidirectional, full-duplex Data Lanes (N = 16 for standard package and 64 for advanced package), one single-ended Lane for Valid, one lane for tracking, a differential forwarded clock per direction, and 2 lanes per direction for sideband (single-ended, one 800 MHz clock and one data). The advanced package supports spare lanes to handle faulty lanes (including clock, valid, sideband, etc.,) whereas the standard package supports width degradation to handle failures. Multiple clusters can be aggregated to deliver more performance per Link, as shown in **Error! Reference source not found.**.

Table 1 summarizes the key metrics for both the packaging options. A die with the standard package design is expected to interoperate with any other design on the standard package. Similarly, a die with the advanced package design will interoperate with any other die designed for the advanced package, even within the wide range of bump pitch from 25u to 55u. It should be noted that the KPI table conservatively estimates performance for the most widely deployed bump pitch today. For example, 45µm bump pitch is used for advanced packaging. The bandwidth density will go up by up to 3.24X if we go with a denser bump pitch of 25µm. Even at 45µm, the bandwidth density of 1300+ GBytes/s /mm or mm^2 (both for linear as well as area) is about 20X of what we can achieve with the most efficient PCIe SERDES. Similarly, PCIe PHY have a power efficiency of ~10pJ/b today which can be lowered by up to 20X with the UCIe based designs due to their shorter channel reach. UCIe also enables for a linear power-bandwidth consumption curve with very fast entry and exit times (sub-ns vs multiple micro-seconds for SERDES based designs) while saving 85+% power. Thus, in addition to being really low power, it also is very effective in power savings, offering compelling power-efficient ultra-high performance. What is important is as the technology advances, these savings would be even more significant. UCIe 1.0 has been defined to meet the projected needs of a wide range of challenging applications through almost the end of this decade.

Table 1: UCIe 1.0 Characteristics and Key Metrics

Characteristics / KPIs	Standard Package	Advanced Package	Comments
Characteristics			
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G d
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across no
Channel Reach (mm)	<= 25	<=2	
Target for Key Metrics			
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u for AP; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm^2)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ CXi Flit Mod

V. Conclusions

The industry needs an open chiplet ecosystem that will unleash innovations across the compute continuum. UCIe 1.0 offers compelling power-efficient and cost-effective performance. The fact that it is an open standard with a plug-and-play model, modeled after several successful standards, and launched by key industry leaders will ensure its wide-spread adoption. We foresee the next generation of innovations will happen at the chiplet level allowing an ensemble of chiplets offering different capabilities for the customer to choose from that best addresses their application requirements.

In the future, we expect the consortium to drive even more power-efficient and cost-effective solutions as bump pitches continue to shrink and 3D integration becomes mainstream. Those may require wider links running slower and get closer to on-die connectivity from a latency, bandwidth, and power-efficiency point of view. Advances in packaging and semiconductor manufacturing technologies will revolutionize the compute landscape in the coming decades. UCIe is well poised to enable innovations in the ecosystem to take full advantage of these technological advances as they unfold.

VI. References

1. D. Das Sharma, "Universal Chiplet Interconnect express (UCIe)®: Building an open chiplet ecosystem", White paper published by UCIe Consortium, Mar 2, 2022

2. Moore, Gordon, "Cramming more components onto integrated circuits", Electronics, Volume 38, Number 8, April 19, 1965

3. A. Biswas, "Sapphire Rapids," *2021 IEEE Hot Chips 33 Symposium (HCS)*, 2021, pp. 1-22, doi: 10.1109/HCS52781.2021.9566865

4. "Universal Chiplet Interconnect Express (UCIe) Specification Rev 1.0", Feb 17, 2022, www.uciexpress.org

Application of Artificial Neural Network Surrogate Models for Efficient Signal Integrity Analysis in Emerging Graphene-Based Interconnects

Surila Guglani, Sourajeet Roy, *Senior Member, IEEE*

Department of Electronics and Communications Engineering, Indian Institute of Technology Roorkee, Roorkee,

***Abstract* — With advancing technology nodes, conventional copper on-chip interconnects are becoming more susceptible to different scattering mechanisms such as sidewall scattering, surface roughness scattering and grain boundary scattering. These scattering mechanisms increase the per-unit-length resistance of the interconnects, thereby leading to increased signal attenuation, latency, and power losses. In order to address these limitations of conventional copper interconnects, more advanced interconnect technologies such as carbon nanotubes and hybrid copper-graphene interconnects are currently being investigated. These newer technologies exploit the enhanced electrical and material properties of novel 2D materials such as graphene to improve the overall conductive properties of the interconnects. However, in order to model the electrical properties of graphene-based interconnects, highly complicated equivalent circuit models are required, the solution of which are extremely time consuming. One approach to mitigate the high computational costs of modeling such novel interconnects is by using artificial neural network models. In this article, we review the current state-of-the-art in artificial neural networks to efficiently model the transient responses of the aforementioned emerging graphene-based interconnects.**

***Index Terms* — Artificial neural networks (ANNs), design space exploration, copper-graphene interconnects, transient response, signal integrity analysis.**

I. Introduction

With the sustained device scaling below the 22-nanometer mark, on-chip copper interconnects are becoming highly vulnerable to various scattering mechanisms such as sidewall and top/bottom surface scattering, surface roughness scattering, and grain boundary scattering [1]. These scattering mechanisms collectively decrease the mean free path of electrons travelling in the copper conductors. This, in turn, significantly increases the per-unit-length (p. u. l.) resistance of the interconnects beyond their nominal bulk value. The increased p. u. l. resistance results in increased signal attenuation, greater signal propagation delay, and increased power losses [1]-[3]. Moreover, with the decrease in transistor feature sizes, the roughness of the copper conductors become more pronounced. This increase in surface roughness leads to greater effective surface area between the conductors themselves and between the conductor and ground, which in turn results in increased parasitic capacitances. The increase in the parasitic capacitance result in greater crosstalk noise and even larger signal propagation delays [3]-[5]. Therefore, copper on-chip interconnects are nearing their performance and reliability limits within the 22nm technology node.

In order to address the above limitations of copper on-chip interconnects, investigations into newer 2D materials such as graphene are currently underway [5], [6]. In particular, the following interconnect technologies based on graphene have been suggested in the literature [6].

(i) Carbon nanotubes (CNTs): Carbon nanotubes can be of two kinds – single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs). SWCNTs comprise of a single graphene sheet rolled up as shown in Fig. 1(a) [7] while MWCNTs consist of multiple graphene sheets rolled up as shown in Fig. 1(b) [7]. Of these, currently MWCNTs are preferred because not only can they carry higher current through the multiple graphene sheets but their growth process is also easier to control [7]. Moreover, statistically speaking, only a third of SWCNT shells in a bundle exhibits metallic conductor properties due to their chirality while the rest exhibit semiconductor properties [7]. This is in contrast to MWCNTs where due to the increasing diameters of the outer shells, almost all shells exhibit metallic conduction even if they are of semiconductor chirality [7].

Both SWCNTs and MWCNTs exploit the significantly higher mean free path of graphene compared to copper at room temperatures [8]. This ensures that CNT interconnects offer much smaller scattering resistance than their conventional copper counterparts. Moreover, MWCNTs also possess much higher current carrying capacity, higher thermal conductivity, and higher mechanical strength than copper interconnects [7]-[9]. As a result, MWCNTs can support extremely high signal speeds (in the range of THz as opposed to GHz), exhibit much smaller propagation delay (in the order of picoseconds instead of nanoseconds), and are far less susceptible to thermal and structural breakdown compared to conventional copper interconnects [9].

(ii) Graphene Nanoribbons (GNRs): Graphene nanoribbons consist of either single or multiple ultra-thin layers of graphene conductors stacked vertically [10]. Figure 1(c) illustrates the vertical stacking of multiple graphene layers to form multilayered graphene nanoribbon (MLGNR) interconnects. MLGNR interconnects, by virtue of having multiple graphene layers has far higher conductivity than single layer graphene nanoribbon interconnects. The MLGNR interconnects can be of the top contact variety (i.e., the MLGNR is connected to the electrode through a metal contact present on the top graphene layer only) or of the side contact variety (i.e., the MLGNR is connected to the electrode through a metal contact deposited over the near and far-end

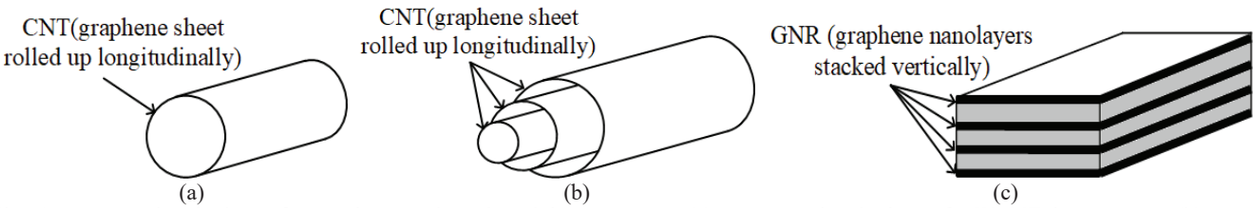


Fig. 1 Cross-sectional view of emerging graphene-based interconnects. (a) Cross-sectional view of SWCNT interconnect (b) Cross-sectional view of MWCNT interconnects (c) Cross-sectional view of MLGNR interconnects

sides of the entire stack). In these interconnects, once again, the lower scattering resistance, the higher thermal conductivity, higher current carrying capacity, and higher mechanical strength of graphene compared to copper is exploited to ensure better electrical performance [10]-[12]. Once possible drawback of MLGNRs is the possibility of inter-sheet electron conduction (i.e., current conduction in the transverse direction) that can reduce the overall current conduction along the length of the conductor (i.e., in the longitudinal direction). To mitigate this issue, intercalation doping is used to improve the Fermi level of the MLGNRs and thus, their overall conductivity.

(iii) Copper-Graphene Hybrid Interconnects: Another issue with conventional copper on-chip interconnects is the diffusion of copper ions from the conductor into the dielectric layer. This increases the dielectric conductivity and leakage losses while introducing discontinuities into the interconnects [13]. As a remedy for the diffusion of copper ions, a barrier layer of tantalum (Ta) or tantalum nitride (TaN) is generally placed around the copper conductor [13]. However, explorations into alterative barrier layer materials have led to the use of graphene nanoribbons as barrier layers around the copper interconnects [14]. Due to the lower scattering resistance of graphene compared to copper, the graphene barrier layers possess better conductive properties than the copper conductor. The presence of these barrier layers significantly lowers the equivalent resistance of the conductor plus the barrier layers [15]. Moreover, graphene barrier layers being ultra-thin, they can stop diffusion of copper ions into the dielectric without significantly reducing the effective cross-sectional area (i.e., the conductance) of the interconnect. Finally, graphene barrier layers possess good thermal stability at very high temperatures.

II. Modeling of Emerging Graphene-Based Interconnects

Despite the many advantages of graphene-based interconnects, all of these emerging interconnects are highly sensitive to fabrication process variations and manufacturing tolerances [16]. Therefore, thorough and detailed design space exploration, design optimization, and variability analysis of such interconnects are required as a precursor to their fabrication. Typically, such analyses of interconnects are performed using thousands of repeated SPICE simulations of the interconnects [16]. The key problem with the SPICE simulations is that the equivalent circuit models of MWCNT, MLGNR, and copper-graphene hybrid interconnects are highly complicated and cumbersome, thus making even a solitary SPICE simulation computationally prohibitive, let alone thousands of simulations. In the following subsections, the details regarding the circuit models of different emerging interconnects are discussed.

A. Equivalent Circuit for MWCNT and MLGNR Interconnects

The MWCNT and MLGNR interconnects are longitudinally divided into small sections where each section is represented using equivalent lumped resistance-inductance-conductance-capacitance (RLGC) circuit elements as shown in Fig. 2. It is noted from Fig. 2 that the equivalent circuit models of these interconnects consist of individual RLGC models of each conducting shell or nanoribbon making up a conductor which are then coupled together using parasitic circuit elements (e.g., the tunneling conductances, quantum capacitances, and inter-shell capacitances) [7], [17]. Therefore, for realistic MWCNT and MLGNR interconnects consisting of a large number of conducting shells or nanoribbons, the overall equivalent circuits are usually massive. These massive equivalent circuits are directly represented in SPICE using a massive coupled modified nodal analysis (MNA) system of equations. This massive MNA system of equations is then directly solved in SPICE to derive the transient response of the near and far-ends of the interconnects - in other words, the signal integrity quantities of the interconnects are probed in SPICE. Unfortunately, the solution of these massive coupled system of MNA equations require massive computational time and memory costs.

B. Equivalent Circuit for Hybrid Copper-Graphene Interconnects

Hybrid copper-graphene interconnects include a combination of the electrical properties of both copper and graphene. The effective electrical characteristics of each hybrid conductor can be expressed using the Telegrapher's partial differential equations and the effective p. u. l. parameters [18]. Importantly, the effective p. u. l. parameters of such heterogeneous interconnects are extracted from a quasi-TEM approximation of the interconnect structure,

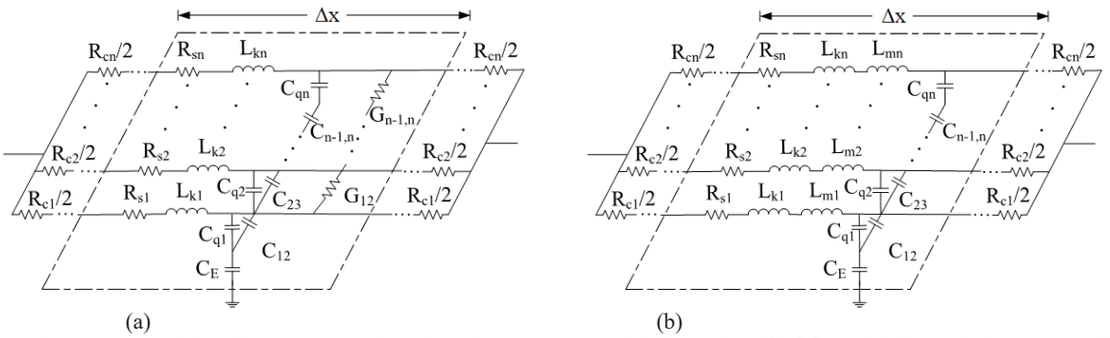


Fig. 2 Equivalent circuit models of emerging graphene-based interconnects. (a) Equivalent RLGC model for each Δx section of MWCNT interconnects (b) Equivalent RLGC model for each Δx section of MLGNR interconnects

usually using full-wave electromagnetic (EM) solvers. For example, a quasi-static 2D EM solver based on the finite element method (FEM) technique is used to calculate the p. u. l. capacitance parameters of the interconnects while a quasi-static 3D EM solver using the method of moments (MoM) technique is used to calculate the p. u. l. inductance parameters [19]. Once, the p. u. l. parameters are extracted, multiconductor transmission line (MTL) models can be used to represent the hybrid interconnects in a SPICE framework. These MTL models can be directly solved in SPICE to probe the transient response of the network. Unfortunately, for hybrid interconnects, the very first step of extracting the p. u. l. parameters using full-wave EM techniques is extremely time consuming [20], [21]. Thus, even for hybrid copper-graphene interconnects, performing SPICE-based design space exploration and variability analysis of these interconnects still remains a major computational challenge.

III. Application of Artificial Neural Networks for Signal Integrity Analysis

A. History of Application of ANNs to Interconnect Modeling

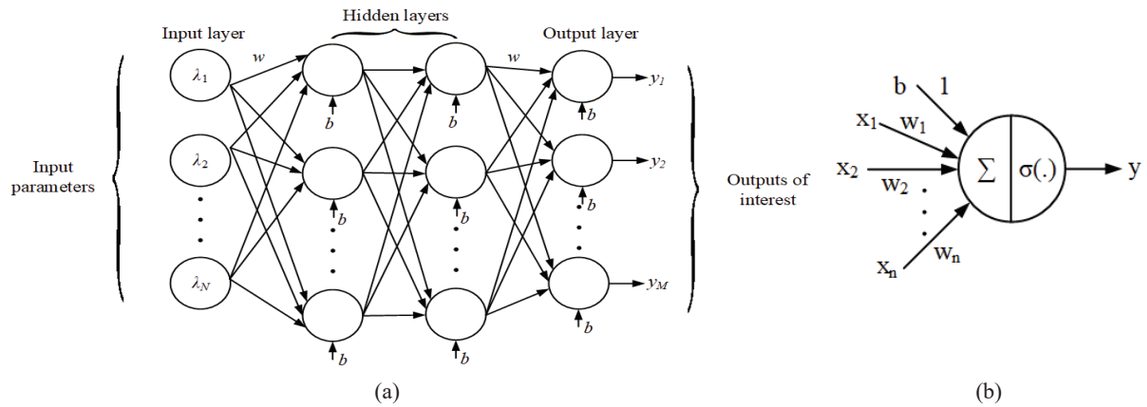
One of the most effective ways to reduce the computational cost of modeling, simulating, and analyzing high-speed interconnects is by using surrogate models. Surrogate models or metamodels are closed-form mathematical expressions that are trained to emulate the input-output relationship of a system under test [22]. Once trained, the metamodels act as analytic functions that are far more numerically efficient to solve compared to simulating the system under test based on the fundamental governing physics equations as done in conventional EM and circuit solvers (e.g., SPICE). These metamodels can be stored and repeatedly used to probe the output results for different values of the input parameters. Hence, their advantage over conventional physics-based solvers is even more profound where the system under test needs to be simulated repeatedly (e.g., in design explorations, parametric sweeps, or Monte Carlo bases statistical analysis).

Recently, machine learning (ML) techniques have garnered significant interest for their ability to construct metamodels that can emulate highly nonlinear input-output relationships [22], [23]. There currently are a variety of machine learning techniques available such as such as artificial neural networks (ANNs), support vector machines (SVMs), and Gaussian processes (GPs) [24], [25]. All of these techniques have already been applied to a variety of modeling and simulation problems within the general field of electronic design automation as well as the more specific field of electronic packaging and interconnect modeling [26]-[29].

Of the various ML techniques, ANNs have had a rich history of being used to model the performance of a variety of interconnect structures including but not limited to conventional copper interconnects [20], [21]. Indeed, ANN metamodels have already been reported for extracting the p. u. l. parameters of copper interconnects as analytic functions of the geometrical, physical, and material parameters of the interconnect structures [26], [27]. These metamodels being closed-form in nature, they can analytically predict the p. u. l. parameters of the interconnects for any arbitrary values of the geometry and layout at a fraction of the time and memory costs required by full-wave EM solvers [20], [21]. Similarly, in the works of [30], recurrent neural networks (RNNs) predicting the transient response of copper interconnects as analytic functions of the geometrical, physical, and material parameters of the interconnects have also been developed. In these works, it is possible to analytically predict the transient response and from them, directly extract the signal integrity quantities of interest while avoiding solving a large system of MNA coupled equations in SPICE at high time costs. In the following section, we will look at how ANNs can be adapted for modeling and simulating the transient response of emerging graphene interconnects.

B. ANNs for Emerging MWCNT and MLGNR Interconnects

The SPICE simulation of MWCNT and MLGNR interconnects involve solving a massive system of coupled MNA equations corresponding to the large RLGC circuit models of Fig. 2. The outputs of interest of such SPICE



(a) (b)

Fig. 3 (a) Basic MLP architecture of ANNs (b) Single neuron from the MLP architecture

simulations are the transient near-end and far-end responses of the interconnects. From the transient responses, signal integrity (SI) quantities such as 50% signal delay, peak crosstalk, eye height and eye width are extracted. Note that the values of all of these SI quantities will change as the values of the geometrical, material, and physical parameters of the interconnects change. Therefore, ANNs can be used to emulate the relationship between the geometrical, physical, and material parameters of the interconnects (inputs) and the corresponding values of the SI quantities (outputs).

In order to emulate the above input-output relationships, the architecture of ANNs take the form of multilayer perceptrons (MLPs) as shown in Fig. 3(a). In this architecture, the first layer on the left-hand side is called the input layer. This input layer accepts the normalized values of the geometrical, material, and physical parameters of the interconnects. These values are then processed and propagated through multiple layers of neurons referred to as the hidden layers (see Fig. 3(a)). Finally, the outputs of the hidden layers are again processed and propagated through the rightmost layer (i.e., the output layer) to yield the values of the SI quantities.

The power of ANNs arises from the nonlinear processing ability of each individual neuron in the MLP architecture [26], [28]. To better explain this, an arbitrary neuron from the MLP architecture is showed in detail in Fig. 3(b). The input to the neuron is the linear combination of the outputs of the previous layer with an added bias term. This linear combination term is then passed through a nonlinear activation function. This processing of the linear combination term through the activation function allows the ANN to be able to emulate highly complex nonlinear input-output relationships. Common activation functions include the hyperbolic tangent function, sigmoid function, arctangent function besides possible user defined functions [26]. The output of the ANNs depend on the values of the linear weights and bias terms used in each neuron. Therefore, the values of these weights and bias terms are tuned such that the error between the values of the SI quantities predicted by the ANN and the true values obtained from SPICE simulations are minimized over the entire input parameter space. This task of tuning the ANN weights and bias terms is referred to as the training of the ANN. The training of the ANN can be performed using well-known optimization algorithms (e.g., stochastic gradient descent and Levenberg-Marquardt with back-propagation [26], [28].

It is observed that in order to train the ANN, the true values of the SI quantities of the MWCNT or MLGNR interconnects have to be first extracted from repeated SPICE simulations. These true values are necessary to calculate the error loss term of the ANN which is to be minimized. The cost of the required repeated SPICE simulations of the interconnects will be typically high. However, this task needs to be done only once – in effect, the associated time cost is a one-time cost. Once the ANN has been trained, the input-output relationship modeled by the ANN will allow us to directly (i.e., analytically) predict the values of the SI quantities for any arbitrary values of the geometrical, material, and physical parameters of the interconnects at negligible computational time and memory costs compared to SPICE simulations.

C. ANNs for Hybrid Copper-Graphene Interconnects

For hybrid copper-graphene interconnects, the main computational effort is in extracting the p. u. l. parameters of these heterogeneous structures using full-wave EM solvers. Here, ANNs of the MLP architecture can be used to reduce this computational effort. For this purpose, the inputs of the ANNs will remain the same as before – the normalized values of the geometrical, material, and physical parameters of the interconnects. However, the outputs will now change to the p. u. l. resistance, inductance, conductance, and capacitance parameters of the interconnects including all mutual inductance terms and coupling capacitance terms. As in the case of MWCNT and MLGNR interconnects, the ANNs can be trained in a similar manner with the exception being that the error function that is to be minimized will now be the error between the p. u. l. parameter values predicted by the

ANN and the true values extracted from full-wave EM solvers spanning the entire input parameter space [20], [21]. Therefore, repeated simulations of the full-wave EM solver will be required to extract the true values of the p. u. l. parameters when calculating the error function. Just as before, this will be a one-time cost.

Now, once the ANN has been trained to accurately emulate the relationship between the geometrical, material, and physical parameters of the interconnects and the corresponding p. u. l. parameters, it will facilitate the repeated yet extremely fast prediction of the p. u. l. parameters followed by SPICE simulation of the MTL model of the hybrid interconnects during design space explorations, iterative design optimization, and Monte Carlo based statistical analysis. Importantly, during such analysis, the time-consuming simulations of the structure using full-wave EM solvers will be avoided entirely. One disadvantage of the above approach is that while the need for using the full-wave EM solvers will be eliminated, we will still need to perform the repeated SPICE simulations of the MTL models of the interconnects. This disadvantage can be eliminated if the ANN is modified to directly emulate the transient response of the interconnects instead of the intermediate p. u. l. parameters. This is possible if the MLP architecture is replaced by a recurrent neural network (RNN).

V. Conclusion

As new interconnect technologies such as those based on graphene (e.g., MWCNT, MLGNR, and hybrid copper-graphene interconnects) emerge, the SPICE-based transient analysis of such interconnects will be significantly more computationally intensive than for conventional copper interconnects. This is because the emerging interconnects possess significantly more complicated structures involving multiple conducting shells and nanoribbons not seen in conventional copper interconnects. In such scenarios, machine learning techniques in general and ANNs in particular have the capacity of emulating the nonlinear relationships between the geometrical, material, and physical parameters of the interconnects and its transient responses. These ANNs can be used as analytic functional maps to precisely predict the transient responses of the emerging interconnects for any arbitrary values of the geometrical, material, and physical parameters without resorting to time consuming SPICE or full-wave EM simulations. As a result, ANNs will enable the extremely fast design space exploration, optimization, and statistical analysis of the interconnects at a small fraction of the expected time costs.

References

[1] J. A. Davis et al., "Interconnect limits on gigascale integration (GSI) in the 21st century," in *Proc. IEEE*, vol. 89, no. 3, pp. 305-324, March 2001.

[2] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, "Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller," *J. Appl. Phys*., vol. 97, no. 2, pp. 023706-1–023706-7, 2005.

[3] International Technology Roadmap for Semiconductors, 2015. [Online]. Available: http://www.itrs2.net/itrs-reports.html

[4] N. Srivastava and K. Banerjee, "Interconnect challenges for nanoscale electronic circuits," *TMS J. Mater.*, vol. 56, no. 10, pp. 30-31, Oct. 2004.

[5] K. Banerjee and N. Srivastava, "Are carbon nanotubes the future of VLSI interconnections?," *2006 43rd ACM/IEEE Des. Autom. Conf.*, San Francisco, California, 2006, pp. 809-814.

[6] H. Li, C. Xu, N. Srivastava and K. Banerjee, "Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1799-1821, Sept. 2009.

[7] M. Tang and J. Mao, "Modeling and Fast Simulation of Multiwalled Carbon Nanotube Interconnects," *IEEE Trans. Electromag. Compatibility*, vol. 57, no. 2, pp. 232-240, April 2015.

[8] A. Todri-Sanial, J. Dijon, and A. Maffucci (editors), *Carbon Nanotubes for Interconnects*. Switzerland: Springer International, 2017.

[9] A. Naeemi, R. Sarvari, and J. D. Meindl, "Performance comparison between carbon nanotube and copper interconnects for gigascale integration (GSI)," *IEEE Electron Device Letters*, vol. 26, no. 2, pp. 84–86, Feb. 2005.

[10] C. Xu, H. Li and K. Banerjee, "Modeling, Analysis, and Design of Graphene Nano-Ribbon Interconnects," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp. 1567-1578, Aug. 2009.

[11] A. Naeemi and J. D. Meindl, "Conductance Modeling for Graphene Nanoribbon (GNR) Interconnects," *IEEE Electron Device Letters*, vol. 28, no. 5, pp. 428-431, May 2007.

[12] A. Naeemi and J. D. Meindl, "Compact Physics-Based Circuit Models for Graphene Nanoribbon Interconnects," *IEEE Trans. Electron Devices*, vol. 56, no. 9, pp. 1822-1833, Sept. 2009.

[13] C.-K. Hu et al., "Future on-chip interconnect metallization and electromigration," in *Proc. IRPS*, pp. 4F.1-1-4F.1-6, Mar. 2018.

[14] A. Singh, T. R. Prabhu, A. R. Sanjay and V. Koti, "An overview of processing and properties of CU/CNT nano composites," in *Mater. Today Proc.*, vol. 4, no. 2, pp. 3872-3881, 2017.

[15] R. M. Sundaram, A. Sekiguchi, M. Sekiya, T. Yamada and K. Hata, "Copper/carbon nanotube composites: Research trends and outlook," in *Roy. Soc. Open Sci.*, vol. 5, no. 11, Nov. 2018.

[16] A. Nieuwoudt and Y. Massoud, "On the Optimal Design, Performance, and Reliability of Future Carbon Nanotube-Based Interconnect Solutions," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2097-2110, Aug. 2008.

[17] M. Kaur, N. Gupta and A. K. Singh, "Performance Analysis of Multilayer Graphene Nanoribbon Based Interconnects," *2017 IEEE MTT-S Int. Microw. RF Conf. (IMaRC)*, 2017, pp. 1-5.

[18] C. R. Paul, *Analysis of Multiconductor Transmission Line*. New York: Wiley, 1994

[19] *ANSYS Q3D Extractor*, 2020, [online] Available: http://www.ansys.com/products/electronics/ansys-q3d-extractor.

[20] R. Kumar et al., "Knowledge-Based Neural Networks for Fast Design Space Exploration of Hybrid Copper-Graphene On-Chip Interconnect Networks," *IEEE Trans. Electromagn. Compatibility*, vol. 64, no. 1, pp. 182-195, Feb. 2022.

[21] S. Kushwaha, A. Attar, R. Trinchero, F. Canavero, R. Sharma and S. Roy, "Fast Extraction of Per-Unit-Length Parameters of Hybrid Copper-Graphene Interconnects via Generalized Knowledge Based Machine Learning," *2021 IEEE 30th Conf. on Elect. Perform. Electron. Packag. Syst. (EPEPS)*, 2021, pp. 1-3.

[22] M. Swaminathan, H. K. Torun, H. Yu, J. A. Hejase and W. D. Becker, "Demystifying machine learning for signal and power integrity problems in packaging," *IEEE Trans. Comp., Packag. and Manuf. Technol.*, vol. 10, no. 8, pp. 1276-1295, Aug. 2020.
[23] H. M. Torun and M. Swaminathan, "High-dimensional global optimization method for high-frequency electronic design," *IEEE Trans. Microwave Theory Tech.*, vol. 67, no. 6, pp. 2128-2142, Jun. 2019.
[24] R. Trinchero, P. Manfredi, I. S. Stievano and F. G. Canavero, "Machine learning for the performance assessment of high-speed links," *IEEE Trans. Electromagn. Compatibility*, vol. 60, no. 6, pp. 1627-1634, Dec. 2018.
[25] V. Vapnik, *Statistical Learning Theory*, Hoboken, NJ, USA:Wiley, 1998.
[26] Q.-J. Zhang and K. C. Gupta, *Neural Networks for RF and Microwave Design*, Norwood, MA, USA: Artech House, 2000.
[27] A. Veluswami, M. S. Nakhla and Q.-J. Zhang, "The application of neural networks to EM based simulation and optimization of interconnects in high-speed VLSI circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 45, no. 5, pp. 712-723, May 1997.
[28] Q.-J. Zhang, K. C. Gupta and V. K. Devabhaktuni, "Artificial neural networks for RF and microwave design-from theory to practice," *IEEE Trans. Microwave Theory Tech.*, vol. 51, no. 4, pp. 1339-1350, Apr. 2003.
[29] P. Watson and K. C. Gupta, "EM-ANN models for microstrip vias and interconnects in dataset circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 12, pp. 2495-2503, Dec. 1996.
[30] Y. Fang, M. C. E. Yagoub, F. Wang and Q.-J. Zhang, "A new macromodeling approach for nonlinear microwave circuits based on recurrent neural networks," *IEEE Trans. Microwave Theory Tech.*, vol. 48, no. 12, pp. 2335-2344, Dec. 2000.

Making the Digital Twin work for Mission Critical Electronics

Adwait Inamdar[1], Przemyslaw Gromala[2], Willem van Driel[1], GuoQi Zhang[1]
[1]Delft University of Technology, The Netherlands
[2]Robert Bosch GmbH, Reutlingen, Germany

Introduction

Digital Twin has become a commonly used phrase in the context of products, processes, businesses, and more. It was first introduced in 2003 by Dr Michael Grieves, but the term was first defined in the *NASA Modelling, Simulation, Information Technology & Processing Roadmap* in 2010 (revised in 2012). Thus, the concept primarily evolved in the context of aerospace and manufacturing applications and was later embraced by many other industries such as healthcare. Among the newer technologies, it currently lies on the peak of the expectation curve according to a report by Gartner in 2018. A recreated chart of the hype cycle, highlighting a few other related emerging technologies, is presented in Figure 1.

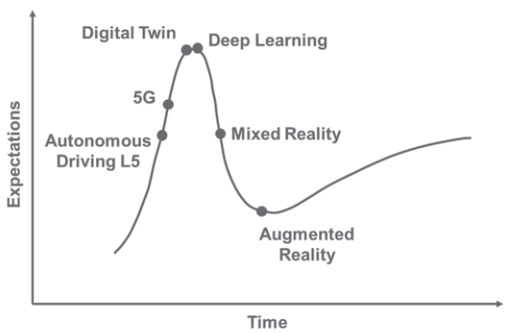


Figure 1: Hype cycle for emerging technologies by Gartner (recreated)

The primary reason behind the adoption of Digital Twin technology is digitalization of industries, which has been accelerated by the newly emerging information technologies (IT) enabling incorporation of more and more electronics such as sensors into the conventional products and systems. A good example of this is the automotive industry, which is progressing towards developing a framework for fully electric, connected, and automated (ECA) vehicles. Every step towards higher level of automation requires additional electronic systems and their integration into various functions of an automobile. Considering exposure to harsh environments, electronics are a crucial component of an automobile with respect to its functionality, cost, and overall safety.

Overall, adoption of electronics is growing at a fast pace. Application fields like intelligent manufacturing, autonomous driving, smart city, and smart services are built around connectivity and artificial intelligence (AI), and thus, require mission critical electronics (MCE) on a large scale. Therefore, reliability of electronic products and their subsystems has become highly critical. In this scenario, performance and lifetime on demand become essential, and Digital Twin presents itself as a key enabler for providing it.

What is a Digital Twin?

Digital Twin is a continuously updated virtual representation of an object, system, or process which replicates all phases in the lifecycle of its physical counterpart. The definition sounds like a virtual model of a system, but it is actually much more than that, virtual model being just one facet of it.

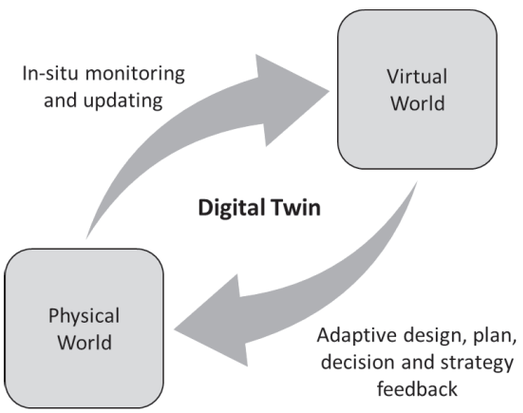


Figure 2: Structure of a Digital Twin system

Figure 2 shows schematically the structure of a Digital Twin system. It consists of three parts – the physical entity, its virtual representation

(model), and the connectivity between these 2 islands for data and information exchange.

The physical entity can be any object, system, or process. It can be implemented on different scales – product, machines and tools, processes, a control-volume, or even a business. In the context of microelectronic systems, product-specific implementation is the most relevant.

Connectivity between the physical entity and its virtual representation is what sets a Digital Twin system apart from just a model. The connections facilitate exchange of data, which enables continuous update of the model rather than remaining static. Similarly, the results generated from the updated model can be used as feedback for improving the physical product. Thus, a bilateral connectivity is the key to build an effective Digital Twin system. The connections can be categorized into three types based on their levels of complexity –

(a) Weak connection: this utilizes connection in only one direction, i.e., from product to model, with no closed loop. Thus, modelling serves as a supporting tool, and it can be mainly used for virtual prototyping, and product/process design.

(b) Cloud connection: this allows real-time monitoring of product, data filtering and transmission. A cloud-based platform is utilized to process the collected data using complicated simulation models. This data can be then utilized for product or process improvement with a closed-loop connectivity. A caveat of this implementation is that the closed loop is external to the product. But the advantage is the capability to run bigger and complex models on an external computational node.

(c) Embedded connection: an embedded connection allows the model to run locally. It also incorporates real-time monitoring and data collection but processes it on the edge. This saves the cost and energy of transmitting data to an external server, and thus, is more efficient. In this way, an integrated close-loop control and decision-making can be achieved. Only shortcoming of this approach is the limited computational power at the edge, e.g., of a microcontroller. Therefore, only simpler, and computationally lighter models such as compact models or meta-models can be used.

Each of these above three approaches is suitable for different kind of applications and use cases.

Digital Twin for Microelectronics

Different stages in the lifecycle of an electronic product are: (1) product design, (2) material selection and characterization, (3) production, (4) usage, service, maintenance, and repair, (5) recycle. Figure 3 (first appeared in *Heterogeneous Integration Roadmap 2021*) elaborates on its wider landscape, where each stage requires its virtual representation. Thus,

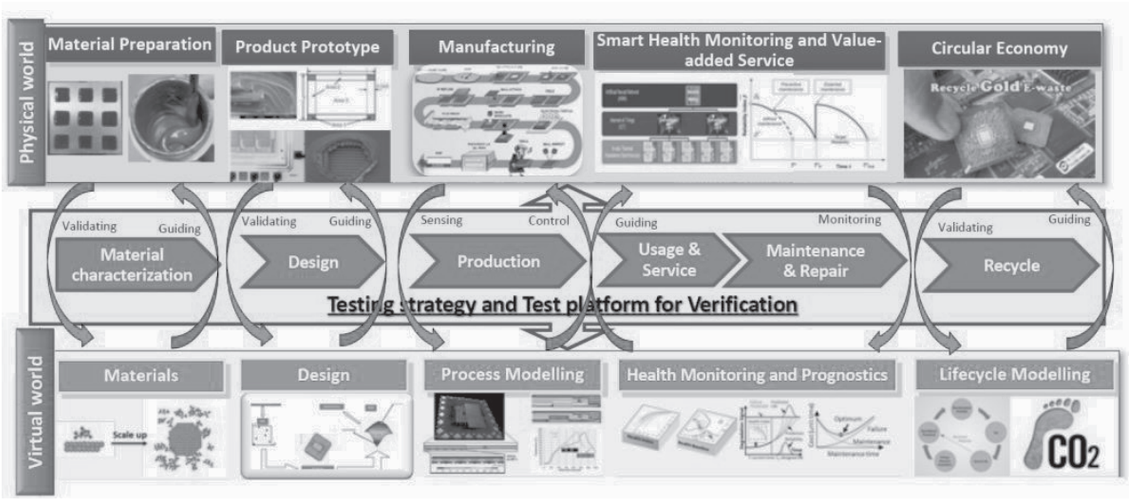


Figure 3: Landscape of product lifecycle and Digital Twin implementation

Digital Twin is multi-layered and multi-scale in nature. The goal is to have an end-to-end Digital Twin implementation for all the stages of product lifecycle, but the complexities involved to achieve it are not addressed by the current state of the art. However, each one of the stages can have its individual Digital Twin implementation.

As an example, consider the stage 4 – usage and service. The primary goal of the Digital Twin of this stage is to establish individual per-product in-situ health monitoring for failure detection and lifetime prognosis. A logical workflow to achieve that is indicated in the flowchart in Figure 4.

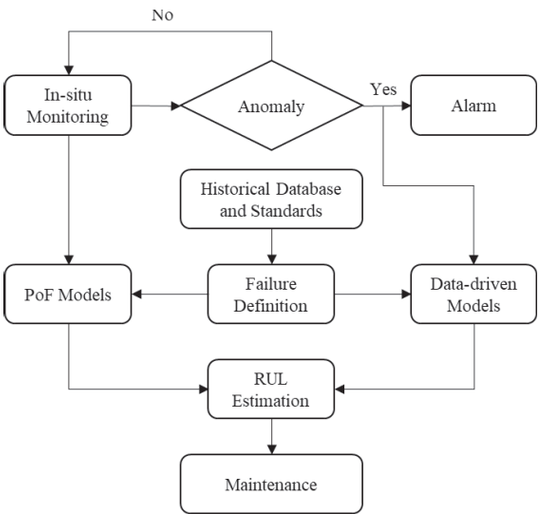


Figure 4: Health Monitoring and RUL Prognosis

In-situ monitoring of products is achieved using advanced sensors. The collected data is used for anomaly detection on the edge. Anomalies are reported, and otherwise, data is utilized for data-driven algorithm for remaining useful life (RUL) estimation, which can either be on the cloud (bigger and complex models) or on the edge (compact/meta models).

Simultaneously, the sensor data is utilized to identify current state of degradation based on the total exposure to harsh environmental conditions and using material degradation models. Accordingly, the physics-of-failure based (e.g., finite element) model of the product is updated, and possible failure modes and resulting RUL is estimated based on the multi-scale/multi-physics simulations, historic database, and standards. The simulations run mostly on an external computing node.

In this way, edge + cloud computing can be utilized for a Digital Twin implementation for predicting RUL. Based on the estimation, a condition-based maintenance can be suggested, which forms a closed loop of connectivity between physical and virtual world.

This implementation has the potential to facilitate individual monitoring of every single product from a batch, while they are in-use. With the combination of edge and cloud computing per-product health monitoring and failure prognostics can be achieved. This would result in better insights about product degradation, and eventually, failure risk mitigation.

Challenges and Roadmap

One of the primary challenges is to develop proper definition, boundaries, and standards around the concept of Digital Twin. The challenges related to the hardware aspect, i.e. the physical twin, involve developing advanced, low cost, and reliable sensors for in-situ monitoring, and embedding these sensors in products to make the system capable of self-monitoring.

The Digital Twin needs to have accurate and efficient multi-scale multi-physics simulation models, which consider non-linearity as well as time and temperature dependency. Some of the key milestones in the context of failure criteria are – definition of accurate failure threshold and multi-failure modes interaction; while for the modelling aspect, they are – simulation-driven design and optimization, accurate compact models, automation for model generation, and transition from a deterministic to a probabilistic /stochastic simulation methodology.

The connectivity aspect needs to solve the challenges with cloud platform and wireless connection, low cost and reliable real-time monitoring, smart sensing and IoT, computational power at the edge, big-data management – collection, storage, smart filtering, processing, and lastly, a closed loop control algorithm.

The roadmap for solving the above challenges is laid out for next 5-10 years, and the key goals to achieve can be simplified as the following 6 points: smart in-situ sensing and transmission, edge computing capable hardware, accurate compact/meta-models embedded in a dedicated highly reliable Digital Twin chip, robust multi-scale multi-physics (nonlinear, dynamic, probabilistic) simulation models, robust data-driven models, and lifetime (RUL) on demand.

prediction of anomaly and failure. This purely data-driven ML-based approach is still a black-box implementation and thus, is difficult to completely rely on.

Digital Twin proposes a combined approach, integrating physics-of-failure (PoF) based models with ML and data-driven models. This ensures that the simulation model of the product is continuously updated for its current degraded state using in-situ data and ageing models.

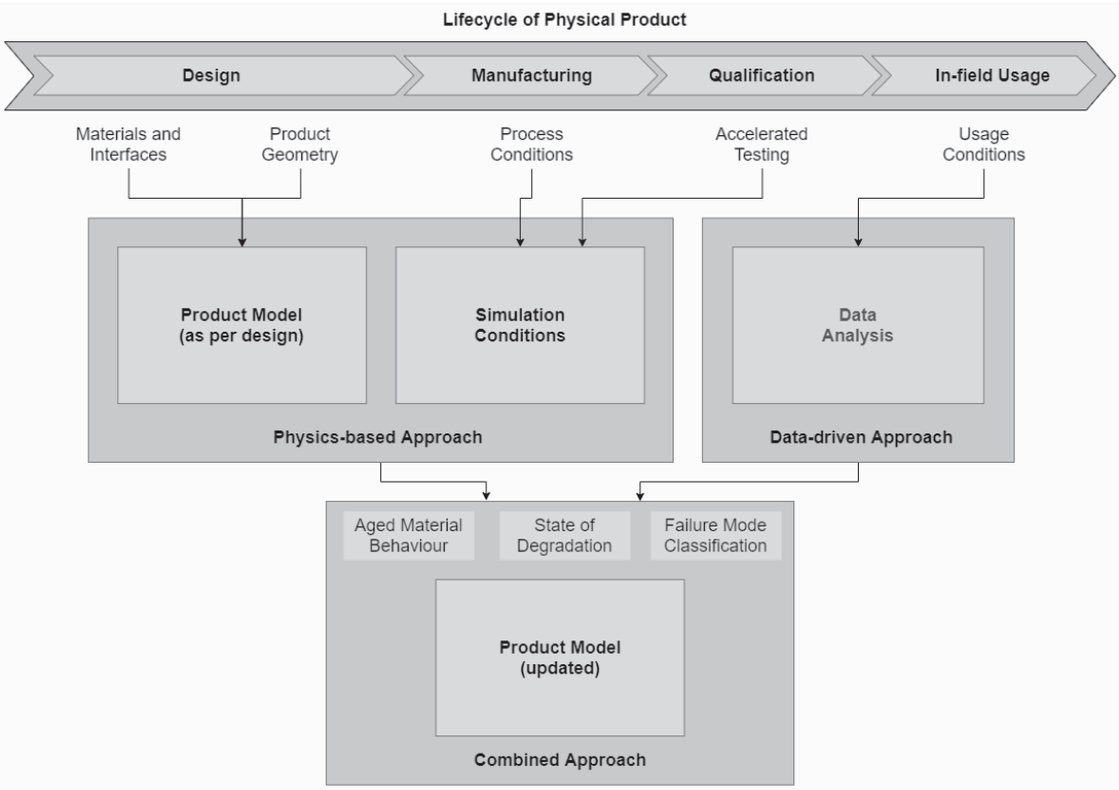


Figure 5: Overview of product-specific Digital Twin Implementation

An overview of how a product-specific Digital Twin system would work is indicated in Figure 5. It shows how the current physics-based modelling approach is limited to consideration of product model as per the original design. It does not get updated for its degradation due to exposure to operating conditions. Thus, the simulations of all later stages do not consider the changes in product due to ageing, making the 'simulation conditions' block completely separated from the product model.

On the other hand is the data-driven approach. It monitors operating conditions through sensors and uses machine learning (ML) for

This allows consideration of 'aged material behaviour', making the virtual representation of the product more realistic. Thus, the simulations are also closer to reality, giving better results and predictions.

In summary, the Digital Twin implementation utilizes best of both approaches. It enables the ability of system optimization, monitoring, diagnostics, and prognostics using integration of AI, machine learning, and big data analytics with the traditional PoF based methods. It serves as a powerful tool for scheduling strategic maintenance by predicting failures and estimating lifetime of electronic components.

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Session	Chair	Affiliation
S2: IVR for Computers and Servers	Siddarth Ravichandran	Chipletz
S3: Multiphysics Design & Tools	Rajen Murugan	Texas Instruments
S4: Additive Manufacturing	Peter Friedrichs	Infineon
S5: Manufacturing Technologies	Jason Rouse	Corning
S7: Materials I Interconnects & Lead Attachments	Andy Mackie	Indium Corporation
S8: Materials II Substrates & Encapsulants	Ninad Shahane	Texas Instruments
S9: High Power Module Integration	Cyril Buttay	Laboratoire Ampère, Lyon
S11: Thermal Management and Reliability	Patrick McCluskey	University of Maryland
S12: Passive Component Integration	John Bultitude	KEMET Corporation
S13: Low Power & Telemetry	Shubhendu Bhardwaj	Florida International University
S14: Tour of FIU Labs	Markondeyaraj Pulugurtha	Florida International University

Plenary Speakers

Dr Michael Guyenot, Bosch, "Highly integrated low inductance SiC power modules."

Professor Fred C. Lee, Virginia Tech, USA, "PCB based Integrated Magnetics."

Dr. Brandon Passmore, Wolfspeed, "Finite-Element Predictive Modeling for Power Modules."

Professor Katsuaki Suganuma, University of Osaka, Japan "Superior heat dissipation by low-pressure Ag sinter joining and real-time AI lifetime prediction for SiC power module."

Dr. Mahadevan Iyer, **Amkor**, "Emerging Power electronics packaging and system integration for automotive applications"

Dr. Deepak Divan, Georgia Tech, "Soft-switching topologies for automotive and aircraft"

In addition, the conference features **keynote talks** from:

Dr. Michael Hill (Intel, IVR)
Dr. Minjie Chen (Princeton University, IVR and Vertical Power Delivery)
Dr. Madhavan Swaminthan (Georgia Tech - PRC, Machine Learning-based Optimization)
Dr. Rajen Murugan (Texas Instruments, Multiphysics Modeling)
Dr. Brij Singh (John Deere, Power Module Manufacturing Advances)
Dr. Patrick McCluskey (Univ. Maryland, Thermal management and reliability)
Dr. Jaim Nulman (Nano Dimension, Additive Manufacturing)
Dr. Osama Mohammad (FIU, Advanced Topologies)
Dr. Matt Kelly (IPC, Power Module Manufacturing Advances)
Dr. Thomas Foulkes (Pacergy, 3D Printed PCBs)
Dr. Srikrishna Bhogaraju (Technical University of Ingolstadt, Cu sintering interconnect analysis)
Dr. Habib Mustain (Heraeus, Power Interconnects)
Dr. Matt Wilkowski (Enachip, Wafer-Integrated Inductors)
Dr. Mike Hayes (Tyndall National Institute, Power Harvesting for IoT)
Dr. G. Q. (Virginia Tech., Nonlinear Resistive Field-Grading in Medium-Voltage Power Modules)

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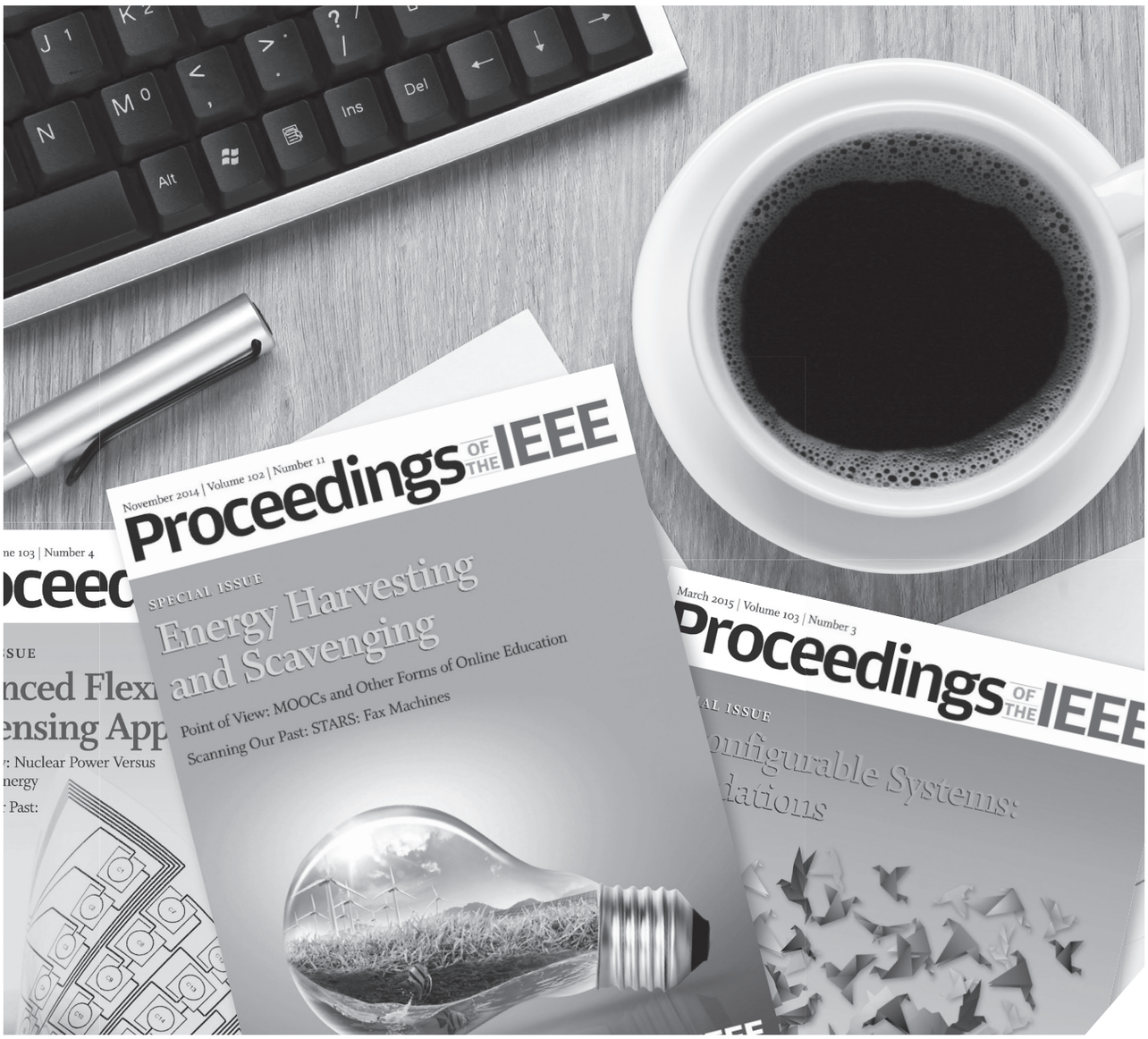

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