Components, Packaging, and Manufacturing Technology Society Newsletter

THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

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President's Column....

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2014–2015 CPMT President
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Welcome to a new CPMT newsletter! I hope you all are getting a great start to 2014. CPMT has certainly hit the ground running with a full slate of upcoming conferences, workshops, and webinars. It is my honor to write to you as the new CPMT President. For the next two years, I will have the privilege of serving you and the broader CPMT community. We have a very dedicated and talented leadership team of CPMT officers working together with many volunteers towards the multifaceted activities of the Society:

Vice President, Technology: Steve Bezuk
Vice President, Conferences: Chris Bailey
Vice President, Publications: R. Wayne Johnson
Vice President, Education: Jean Trewhella
Vice President, Finance: Thomas G. Reynolds III
Sr. Past President: Rolf Aschenbrenner
Jr. Past President: S.W. Ricky Lee
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Program Director, Student Programs: Kwang-Lung Lin
Program Director, Industry Programs: William T. Chen
Program Director, Region 8 Programs: Toni Mattila
Program Director, Region 10 Programs: Hirofumi Nakajima

Looking ahead, I am excited about the tremendous opportunities for CPMT to continue to grow and thrive. With the support of the CPMT officers and Board of Governors, we shall continue the growth and impact of CPMT by focusing on **long term strategies** as well as **improved services and increased value** to CPMT members. As our industry and Society are going through a major transformation, CPMT will increase **membership services globally** and extend our reach to **diverse experiences and backgrounds**. CPMT will also engage and influence emerging and **disruptive technologies through collaboration** with other societies and industries. In my next message, I will update you with more details on the execution plan for the next two years.

I would also like to take this opportunity to express my sincerest appreciation to, Ricky Lee, who served as CPMT President from 2012 to 2013. Under his leadership, CPMT continued to grow through a platform of **Connecting Peers, Mentoring Talents**. Truly this is what our Society is all about.

Finally, your support is essential to CPMT's future success. I highly value your opinions and ideas, and welcome your feedback on how CPMT can better serve you and our community. Please do not hesitate to write to me at jiexue@ieee.org. l look forward to hearing from you and meeting you in future CPMT events.

NEWSLETTER SUBMISSION DEADLINES:

1 February 2014 for Spring issue
1 May 2014 for Summer issue
1 August 2014 for Fall issue
1 November 2014 for Winter issue

Submit all material to nsltr-input@cpmt.org

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2015 term-end: Regions 1-6,7,9—Phil Garrou, Patrick Thompson; Region 8—Karlheinz Bock; Region 10—Kuo-Ning Chiang, Charles W. Lee, Daniel Lu

2016 term-end: Regions 1-6,7,9—Li Li, Ning-Cheng Lee, James E. Morris, Jeffrey C. Suhling; Region 8—Toni Mattila, Gilles Poupon

CPMT Society Newsletter

Editor-in-Chief: Kitty Pearsall kitty.pearsall@gmail.com

CPMT Archival Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:
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Tolga Tekin

3D/TSV:
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Region 10 Programs: Hirofumi Nakajima, hirofumi1703nakajima@gf6.so-net.ne.jp

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Long Range/Strategic Planning: Rolf Aschenbrenner, Rolf.Aschenbrenner@izm.fraunhofer.de
Nominations: S.W. Ricky Lee, rickylee@ieee.org

Distinguished Lecturers

Program Director: Jean Trewhella, jeanmh@us.ibm.com

Lecturers: Albert F. Puttlitz, Ph.D., Avram Bar-Cohen, Ph.D., H. Anthony Chan, Ph.D., Rajen Chanchani, Ph.D., William T. Chen, Ph.D., Badih El-Kareh, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., George G. Harman, Ph.D., R. Wayne Johnson, Ph.D., George A. Katopis, Ph.D., John H. Lau, Ph.D., Michael Lebby, Ph.D, Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., T. Paul Parker, Michael Pecht, Ph.D., Karl J. Puttlitz, Ph.D., Bahgat Sammakia, Ph.D., Dongkai Shangguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Yong-Khim Swee, Yutaka Tsukada, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Ralph W. Wyndrum Jr., Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branch Chapters

Refer to cpmt.ieee.org for CPMT Society Chapters and Student Branch Chapters list

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CPMT Society News....

Message from the Past President

S.W. Ricky Lee

People usually said: "I cannot believe how time flies……" when they stepped down from their offices. Although this is such a stereotype, I still have to say it because that is the true feeling. Indeed many things happened to CPMT in the past two years during my term as the Society President. With the help from numerous colleagues, most of whom are CPMT officials and BoG members, we were able to achieve the following:

- Revamp of society website and introduction of "Member Only" webpage.
- Completion of IEEE Technical Activities Five-Year Society Review.
- Improvement of DL program.
- Re-org of Technical Committees and offering of webinar series.
- Early election of Society President.
- Revision of Society Constitution and Bylaws.

In addition, there were many regional activities around the world that contributed to the growth of CPMT. I really have to thank those colleagues who dedicated themselves to making CPMT a better technical society. Please pardon me for not being able to list all their names due to the limitation of space. But people do know who you are and what you contributed. From the bottom of my heart, I thank you!

As you may know, becoming the President of CPMT means at least six years of commitment. I will continue to serve as the Junior Past President for two years, followed by two more years as the Senior Past President. I have very high confidence in the new CPMT official team and will do my best to help them to improve our Society. I look forward to meeting with you again in some of CPMT events in the near future.

Avram Bar-Cohen Receives 2014 IEEE Components, Packaging and Manufacturing Technology Award

Avram Bar-Cohen
Distinguished University Professor
of Mechanical Engineering
University of Maryland,
College Park, USA

"For contributions through leadership, education, and advocacy to thermal design, modeling, and analysis of electronic components, and for original research on heat transfer and liquid-phase cooling."

The IEEE Components, Packaging and Manufacturing Technology Award, sponsored by the IEEE Components,

Packaging and Manufacturing Technology Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

The 2014 Award will be presented to Avram Bar-Cohen at the 64th Electronic Components and Technology Conference (ECTC), May 2014.

Avram Bar-Cohen has defined and guided the emergence of thermal packaging as a critical engineering domain, addressing the consequences of heat generation within ever-shrinking electronic components. He has laid the scientific foundations for the thermal management of electronic components with seminal research on air-cooled heat sinks and liquid cooling of logic and radio-frequency devices. Engineered thermal management devices and heat flow paths are necessitated by the consequences of heat generation within electronic components, as uncontrolled temperatures can cause degradation in performance and reliability of solid-state devices. Dr. Bar-Cohen's work has formed the basis of thermal courses taught today and has driven advances in applications ranging from consumer electronics to super-computing platforms. He is also leading the way in the emerging area of embedded microfluidic cooling techniques.

An IEEE Fellow, Dr. Bar-Cohen is a Distinguished University Professor of Mechanical Engineering at the University of Maryland, College Park.

Avram Bar-Cohen joins the following past recipients of this Award.

2013 – John H. Lau

"For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging."

2012 – Mauro J Walker

"For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations."

2011 – Rao R. Tummala

"For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging."

2010 – Herbert Reichl

"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

2009 – George G. Harman

"For achievements in wire bonding technologies."

2008 – Karl Puttlitz Sr. and Paul A. Totta

"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages."

2007 – Dimitry Grabbe

"For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

2006 – C. P. Wong

"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005 – Yutaka Tsukada

"For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004 – John W. Balde

"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www.ieee.org/awards

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CPMT Society Officers and Program Directors For 2014–2015

The CPMT Society Board of Governors appointed its Officers and Program Directors for the two-year term of 1 January 2014 through 31 December 2015. The following individuals were appointed:

Vice President, Technology

STEVE J. BEZUK (M'90) is Senior Director of IC Package Engineering at Qualcomm. Steve's group is responsible for current and next generation packaging technologies for all of Qualcomm's products. Prior to joining Qualcomm Steve was with Kyocera, Unisys, Sperry-Univac and RCA's Sarnoff Research Center. Steve has worked and managed groups in a variety of areas, including of amorphous silicon research, CMOS, Bipolar and GaAs IC process development, Laser enhanced materials processing, and wirebond, TAB, Flip Chip, MEMS, and TSV packaging. Steve has authored and presented papers and keynote addresses at a variety of international conferences.

Steve has also been very active in the IEEE CPMT for over 20 years. He participated at the local chapter level in San Diego from 1988 to 1992, organizing and presenting at chapter events. Steve joined committees for the ECTC (Electronic Components Technology Conference) starting in 1992 and helped start and establish the interactive sessions (poster sessions) as an important addition to the conference. Steve was the General Chair for the 2004 ECTC conference and is the currently Publications Chair. Steve has also served as a member of the conference Steering Committee (formerly the Governing Council) since 2004. He was also a member of the team that led the acquisition of ECTC from its co-sponsor. Steve has served as a member of the CPMT Board of Governors and is in his third term.

In addition, Steve has been a strong and active supporter of education throughout his career, working with high schools, universities and consortia. He also has coordinated programs with the University of Minnesota, University of California at San Diego, the SRC, and MCC. Steve is a member of the Industry Advisory Board for the San Diego State University Mechanical Engineering Department and past chair.

Steve has a B.S. in Chemistry from the University of Pittsburgh and a Ph.D. in Chemistry from the University of Minnesota.

Vice President, Publications

R. WAYNE JOHNSON (S'77, M'79, S'80, M'82, S'85, M'87, SM'94, F'04) is a Professor and Chair of Electrical and Computer Engineering at Tennessee Tech University. Research efforts are focused on materials, processing, and reliability for electronics and for extreme environment electronics. Current research projects span the temperature range for 50 mK to +773 K. Prior to joining Tennessee Tech, he was at Auburn University for 25 years, where he established teaching and research laboratories for advanced packaging and electronics assembly. He is a CPMT Distinguished Lecturer on Extreme Environment Electronics. He has published and presented numerous papers at workshops and conferences and in technical journals. He was a co-author of the 2012 Best Paper of the Transaction on Components, Packaging and Electronics Manufacturing, Packaging Technologies Section, a co-author of the 2010 ECTC Best Paper of Conference and co-faculty advisor for the 2009 ECTC Intel Best Student Paper winner. He has also co-edited one IEEE book on MCM technology and written book chapters in the areas of silicon MCM

technology, MCM assembly, automotive MCMs (IEEE Press), flip chip assembly and high temperature packaging (IEEE Press). Wayne was elected a Fellow of IEEE in 2004 for "his contributions to electronics that must operate in harsh environments." Dr. Johnson received the B.E. and M.Sc. degrees in 1979 and 1982 from Vanderbilt University, Nashville, TN, and the Ph.D. degree in 1987 from Auburn University, Auburn, AL, all in electrical engineering. Wayne is the current Vice President of Publications for the IEEE CPMT Society and serves as the Chair of the Publications Committee. He is a Co-Editor-in-Chief (Manufacturing Technology Section) and Managing Editor of the IEEE Transactions on Components, Packaging and Manufacturing Technology. He is also a Fellow of the International Microelectronics and Packaging Society (IMAPS), and a member the Surface Mount Technology Association (SMTA) and IPC.

Vice President, Conferences

CHRIS BAILEY (A'01, M'03, SM'05) is Professor of Computational Mechanics and Reliability at the University of Greenwich, London, United Kingdom. I received my PhD in Computational Modelling from Thames Polytechnic in 1988, and an MBA in Technology Management from the Open University in 1996. Before joining Greenwich in 1991, I worked for three years at Carnegie Mellon University (USA) as a research fellow in materials engineering.

One of my main achievements with regards to CPMT was helping to establish the Region 8 flagship conference ESTC (Electronics System-integration Technology Conference). I was the Programme Chair for the first conference held in Dresden, and the General Chair for the 2008 conference in London. I am also a regular attendee and committee member of CPMT conferences such as ECTC and EPTC as well as conferences such as Eurosime (Europe), ICEPT (China), and IMPACT (Taiwan). In 2014 I will be organising the Therminic Conference in Greenwich, London. I have also worked closely with others in Europe to help promote closer co-operation between CPMT and IMAPS for the benefit of the whole community.

Since 2010 I have had the pleasure of serving you as a member of the CPMT Board of Governors. During my first two terms on the BoG I have taken on the role of Strategic Director for Student Programs with the aim of supporting students involved in CPMT activities worldwide. Particular achievements include arranging financial support for student attendees at the International Spring Seminar on Electronics Technology (ISSE) as well as promoting student membership at events such as ECTC, EPTC and ESTC.

My research has resulted in over 250 publications. I am currently an Associate Editor for the CPMT Transactions and have been a guest editor on the journal of Soldering and Surface Mount Technology. I am also a committee member of the Innovative Electronics Manufacturing Research Centre (IeMRC) in the UK and have participated in a number of UK Government sponsored overseas missions to promote collaboration and review electronic packaging technologies. Recently I became a member of the working group writing a new IEEE standard for Prognostics and Health Management for Electronic Systems.

Vice President, Education

JEAN M. TREWHELLA (M'06) Recently Ms. Trewhella has moved back to her roots and is spearheading IBM's optical interconnect initiative including SiPhotonics in STG. Prior to this she spent 5 years as Director of IBM Packaging Research and Development Center high performance first level packaging technology with responsibility for both organic and ceramic packaging as well as 3D initiative.

Ms. Trewhella received her B.S. in Physics from Antioch College (1987) and her M.S. in Applied Physics from Columbia University (1992). She joined the T.J. Watson Research Center, IBM, in 1988 where her work included polymer optical waveguides fabrication, electrical modeling, and opto-mechanical package design for data communication systems. In 2000 she created the High Speed Electrical and Optical Packaging Group in IBM Research directing work in electrical link signal integrity, advanced 1st and 2nd level packaging, and low cost high speed opto-mechanical packaging. She received an Outstanding Technical Achievement Award for her work on 10Gbps Ethernet Transceiver Development in 2003. In 2005 she drove IBM wide team of engineers and scientists to highlight key disruptive technologies in Technology, Application-Optimized Systems, and Services 2.0. From 2006–2008 she was responsible for the Electronic Packaging Integration Group in IBM STG where her team developed the power5 and z10 system hardware.

Ms. Trewhella was on the Strategic Advisory Board for NSF STC—Materials & Devices for Information Technology Research 2004–2008, she served as the General Chair of the 60th ECTC and is currently a member at large of the CPMT Board of Governors. She has authored numerous papers and holds over 20 US patent

Vice President, Finance

THOMAS G. REYNOLDS III (M'92, SM '04) Dr. Reynolds received his PHD from Brown University in 1972 where he worked on synthetic inorganic chemistry of electronic materials. His MS (1966) and BS (1964) were from the University of Virginia in Materials Science and Mechanical Engineering respectively. Tom has worked in the field of electronic ceramic materials and other advanced technologies for more than 35 years.

Retiring in 2003, from 1992 Tom was the Director of Technology at Murata Electronics N.A., Inc. He has worked in the areas of leading edge designs in decoupling capacitors, hard disk drive activation, LTCC modules, and integrated passive components. He has acted as liaison between American designs and Asian development activities, as well as in merger and acquisition analysis. Prior to joining Murata, Dr. Reynolds worked for Philips Electronics for 18 years in both the US and Europe, developing processes and methods for electronic (dielectric) ceramics, and from 1968 to 1973 he was staff scientist at Texas Instruments.

Tom has been involved with CPMT and ECTC (Electronic Components Technology Conference) for more than 19 years. He was General Chair for ECTC in 2000 and was active for several years following this as Finance Chairman. He is also a Senior Member of IEEE. Tom has been a member of the CPMT Board of

Governors since 2004 and VP of Finance since 2006. In addition he is currently serving as Treasurer of the ECTC.

Additional activities and responsibilities include Treasurer of the Ft Walton Sail & Power Squadron of the United States Power Squadron and he was Commodore of the Ft Walton Yacht Club in 2006. Tom also served on the Board and the Finance Committee of that Club from 2007–2010. Tom is also a Founding Member of the Florida Commodores Association—an association of more than 250 with the goal of fostering communication, guidance and mentoring of past present and future leaders. Tom is also a member of the Institute for Senior Professionals (North West Florida State College), an association of business, professional, medical and military professionals to advise and serve the local community based on their experience and expertise.

Program Director, Membership Programs

PATRICK THOMPSON (M'87, SM'92) earned his BS, MS and PhD degrees in Chemical Engineering at the University of Missouri-Rolla. He has more than 25 years of experience in advanced packaging research, development and transfer to manufacturing, contributing to technologies ranging from flip chip fabrication and packaging, flip chip on board and chip scale packages, to multichip packaging, MEMS, optoelectronic packaging, and high performance portable packaging. He has led teams at Bell Labs, AMI Semiconductors, and Motorola (now Freescale). Since 2001, he has been a Senior Member of the Technical Staff at Texas Instruments, where he currently leads fine pitch Cu pillar interconnect and TSV packaging technology development.

Pat is active in industry-consortia and industry-university partnerships, including mentoring SRC custom projects and PhD students.

Pat has five patents and over two dozen publications. He has presented packaging tutorials and given invited talks at leading packaging conferences. He is a member of the Electronic Components and Packaging Technology Conference technical program committee, where he has held multiple positions, including General Chair of the 2006 ECTC, and is now the Financial Chair. He has served at both the local and Society level of the CPMT holding positions including Member-at-Large of the Board of Governors, Administrative Vice President, and Technical Vice President of the CPMT.

Pat has applied his interest in professional education and training and industry-academia interactions in CPMT as a member, and current chair of the Awards Committee. He instituted the CPMT Student Travel Award, and leads the search for and recognition of outstanding packaging professionals through the CPMT major awards. He is also a member of the ECTC Advisory Committee and the CPMT Field Award search team.

Program Director, Chapter Programs

KITTY PEARSALL (A'84, M'01, SM'02) Kitty Pearsall received the BS degree in Metallurgical Engineering in May 1971 from the University of Texas at El Paso. In 1972 she joined IBM as a Materials Engineer. In 1976 she left IBM on an educational leave of absence. During this absence, Kitty received the MS and PhD degree in Mechanical Engineering, Materials Option from the University of Texas at Austin in May 1979 and May 1983 respectively. From 1983 to 2013 Kitty served as an IBM technical resource in materials/package engineering in manufacturing, procurement and development environments. Twelve of these years were spent in technical management focusing on the qualification of various commodities.

In 2005 Kitty was appointed an IBM Distinguished Engineer (DE) and was elected into the IBM Academy of Technology. As a DE in the Integrated Supply Chain Kitty serves as a process consultant and subject matter expert working on strategic initiatives impacting qualification and end quality of procured commodities. She is engaged with WW teams implementing these cross-brand, cross commodity processes/products. As a technical executive in IBM Kitty is passionate about the development of the ISC technical pipeline and was awarded the Women in Technology Fran E. Allan Mentoring Award (2006) in recognition of her people development both in and outside of IBM.

Kitty has been a licensed Professional Engineer in the State of Texas since 1993. She is the holder of 2 US patents, 7 patent pending and several disclosures that have contributed to the IBM patent portfolio. She has numerous internal publications as well as 19 external publications in IEEE conferences and journals. Kitty was recognized as a 2007 recipient of the Cockrell Engineering Distinguished Engineering Graduate by University of Texas Austin. In 2008 she was inducted into the University of Texas Mechanical Engineering Department Academy of Distinguished Alumni.

Kitty is an active member in IEEE and CPMT. She holds memberships in TMS, American Society of Metals and CPMT. Kitty has been a member of the ECTC Manufacturing Technology Committee since 1993 and has been on the Professional Development Course (PDC) Committee since 2006. Since 2008 Kitty assumed the Chair position of the PDC.

During Kitty's tenure on the CPMT Board of Governors she has served as a Member at Large, the Strategic Awards Director, and currently as VP of Education. If reelected she plans to continue this and will focus on increased recognition of contributions to the CPMT Society in emerging Geos, and technical development of the CPMT women membership.

Program Director, Awards Programs

ERIC PERFECTO (M'95, SM'01) has 28 years of experience at IBM working in the development of advanced packages for high-end systems. He holds an M.S. in Chemical Engineering from the University of Illinois and an M.S. in Operations Research from Union College.

Until 2000, Eric worked on the development and implementation of multi-level thin films on ceramic substrates, leading projects in photolithography, chemical etching, photosensitive polyimide, pattern electroplating and bonding metallurgies for C4 joining, wire-bonding and LGA. Later, he led the development of the thin film transfer technology including the joining materials and processes. He is currently the C4 Development Chief Technologist responsible for UBM and Pb-free solder implementation and yields improvements for server, ASICs and 3D applications. His technical interests include chip-package interaction, electromigration, 3D interconnect, and design for manufacturing.

An author of more than 50 technical papers, Eric received two Best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CPMT Trans. on Adv. Packaging. He holds over 35 US patents and has been honored with two IBM Outstanding Technical Achievement Awards: one for the development and implementation of Cu-Polyimide structures, and the other for the development and implementation of 150 um pitch C4 technology.

Eric served as the 57th ECTC General Chair in Reno, the 55th ECTC Program Chair, the ECTC Materials and Processes Subcommittee Chair ('02–'03), and is currently the ECTC Publicity chair. He has achieved senior member status from IEEE, IMAPS and Society of Plastic Engineers, and is a member of the Society of Hispanic Engineers. Current volunteer activities include chairing the mentoring committee of the IBM East Fishkill Technical Vitality Council, and frequently serves as a judge at the Dutchess County Science Fair, NY.

Eric is currently an elected member of the Board of Governors of the CPMT where he serves as the Program Director, Awards Programs. He is an Associate Editor for the CPMT Transactions.

Program Director, Student Programs

KWANG-LUNG LIN (M'98, SM'05, F'11) is Distinguished Professor in the Department of Materials Science and Engineering (MSE), National Cheng Kung University (NCKU), Taiwan. He received Ph.D. degree in Metallurgy from the Department of Materials Science and Engineering of Pennsylvania State University in 1984. He has been with NCKU since 1985 after one year postdoctor research at Ames Lab (DOE)—Iowa State University. He was the Department Head of the MSE-NCKU (1991~1994), the Director of the Precious Instrument Center of NCKU (1998~2001), the Deputy Director and then the Director of the Institute of Micro-Nano Technology of NCKU (2002~2004), the Coordinator of the Metal and Ceramic Program of the National Science Council (NSC) of Taiwan (2001~2004), the Director General of the Department of International Cooperation of NSC (2005~2007), the Director of Nano Powder and Thin Film Technology Center and the Deputy Executive Director of ITRI South —ITRI (2009~2010), Technology Consultant of ASE, Inc (2011~). He has served in several international academic society committees including the Strategic Award Committee—IEEEE CPMT (2007~present), Board of Governor—IEEE CPMT (2007~present), Board Committee Member—IEEE CPMT (Taipei Chapter), Regional Director—Region 10 IEEE CPMT (2012~present), Electronic Packaging and Interconnection Materials Committee of TMS. He has aggressively served in organizing/co-organizing international academic symposia, as program committee, or as session chairman in the areas of surface modification, electronic packaging and Pb-free solder. The international symposia he has been involved include ECTC, EMAP, IMPACT, Pb-free Solder Symposium and Workshop of TMS, Advanced Electronic Packaging Materials—MRS, ISMEN (Int Symposium of Materials for Enabling Nano-device), IUMRS-ICA.

Professor Lin's interest of research include flip chip technology, solder bumping, Pb-free solders, interfacial material interaction, electromigration of solder, phase transformation under current stressing. Part of most important research achievements is the successful development of a new Sn-Zn series solder as well as the understanding of the solid/liquid solder interaction mechanism and interfacial behavior, phase transformation of solder under current stressing. Professor Lin has been author/co-author of more than 175 international journal refereed papers and given more than 60 presentations in international academic conferences. He has been awarded 16 patents from USA, Japan, and Taiwan in flip chip, solder bumping, and Pb-free solders. He has also received Best Paper Award—Silver Medal (American Electroplating and Surface Finishing Society, 1997), Distinguished Research Award (NSC, 1997, 1999), Outstanding Engineering Professor Award (Chinese Engineering Society-Taiwan, 1997), C. T. Ho Distinguished Award (2006). He has been serving as referee for a number of international academic journals as well as project reviewers of the funding agencies of several countries. He is currently the editor-in-chief of Materials Chemistry and Physics (Elsevier publisher, IF 2.353).

He has also been serving as consultant to major electronic packaging industries in Taiwan. A great number of Ph.D. and MS graduates from his group are serving in major semiconductor foundry/electronic packaging/optoelectronic/solar cell/advanced materials industries in Taiwan. He also helped the major packaging industries in Taiwan on establishing the first flip chip solder bump manufacturing line, gold bumping manufacturing line by providing engineer training and technical consultation at the first place.

Program Director, Industry Programs

WILLIAM T. CHEN (M'92, SM'03, F'06) received his engineering education at University of London (B.Sc), Brown University (M.Sc) and Cornell University (PhD). He joined IBM Corporation at Endicott New York in 1963.

At IBM he worked in a broad range of IBM microelectronic packaging products. He received IBM Division President Award for his leadership and innovation in Predictive Modelling on IBM products. He was elected to the IBM Academy of Technology for his contributions to IBM Products and Packaging Technologies. He retired from IBM in 1997. He joined the Institute of Materials Research and Engineering (IMRE) in Singapore, to initiate research in microelectronic packaging materials and processes. He was appointed to the position Director of the Institute (IMRE) steering the growth in people, funding and research facilities and research direction for IMRE to become the leading materials science and engineering research center in the ASEAN region. In 2001 he joined ASE Group, where he holds the position of ASE Fellow and Senior Technical Advisor. In this assignment he has responsibilities for guidance to technology strategic directions for ASE Group.

He is Senior Past President of the IEEE/CPMT Society. He is the Co-Chair of the ITRS Assembly and Packaging Roadmap Technical Working Group. He is chair of the Semicon West Packaging Committee. He has been elected to a member of the iNEMI Board. He is a member of the Technology Committee of GSA.

He has been elected to Fellow of IEEE and Fellow of ASME. He has served as an Associate Editor of ASME Journal of Electronic Packaging, and IEEE/CPMT Transactions.

Program Director, Region 8 Programs

TONI MATTILA (M'08) is a research scientist and docent at Aalto University in Helsinki, Finland where he leads a research team that focuses on the reliability of electronic devices. He received his Ph.D. degree in electrical engineering in 2005 and an M.Sc. degree in materials science and engineering in 1999 from the Helsinki University of Technology (HUT). Since 1996, he has been working with electronics production technologies and reliability of electronic devices both in industrial and academic settings. Before joining HUT in 1999 he worked in Tellabs and Nokia.

Toni's research has focused on electronics production technologies, soldering in electronics, failure mechanisms of electronic assemblies, MEMS technologies, and the development of improved methods for reliability assessment and lifetime prediction. Within the framework of his research Toni has been working in close co-operation with international electronics industry, research institutions and universities. His research has so far resulted in over fifty publications in scientific and technical journals and conferences. In addition, Toni has authored seven book chapters, held several professional tutorials during conferences and been a frequent speaker at conferences, seminars and technology fairs. He is also a frequent reviewer in several scientific journals, including CPMT Transactions.

Since 2008, Toni has been Chairman of the CPMT Finland Chapter. During this time he has, together with other board members, developed and revitalized local activities. More than 100 people attend seminars and events organized by the CPMT Finland chapter annually. He has also established firm connections between the CPMT chapters in Scandinavia. Toni is currently an elected member of the Board of Governors of the CPMT.

Toni also works actively in the IEEE Finland Section, where he has been a member of the executive committee since 2008, and served in various positions. Other IEEE activities include, for example, a membership of technical committees for all three Electronics System Integration Technology Conferences (ESTC). In the past he has also acted in several other positions of trust. For example, he has been the chairman of a housing association for ten years.

Program Director, Region 10 Programs

HIROFUMI NAKAJIMA (M'06, SM'11) received his Bachelor's and Master's degree of Electric Engineering from Shinshu University, Japan in 1976 and 1978, respectively. He joined NEC Corp. in 1978 and started his career on semiconductor packaging technology. His working fields in his younger days included development of in-line snap-cure die-bond process and its material, chip-on-board packaging, Cu wire bonding, and commercializing stacked memory packages. He was transferred to NEC Electronics Inc. in Roseville, California in 1988, where he managed the assembly engineering group. After a 5-year work in U.S., he returned to NEC Corp. in Japan, where he directed the packaging department in developing BGA, CSP, and single-point TAB bonding. In 2002 his responsibility shifted from the management of hands-on technical development to strategic planning of technical development including benchmarking and the future trend. He joined the committee member of IEEE VLSI Package Workshop in Japan in 2003, and then enrolled into IEEE CPMT Society in 2005. His work area expanded to the activity of industry cooperation, including international technology roadmap of semiconductors (ITRS), standardization activity, and Semi Japan. He served as the program chair of IEEE VLSI Package Workshop in Japan in 2008 and refurbished it as IEEE CPMT Symposium Japan (ICSJ), where he served as the executive chair in 2010. He had kept working for Renesas Electronics Co. after the merger between the semiconductor division of NEC Co. and Renesas Technology in 2010 until his resignation in September 2013.

His strength is comprehensive understanding of package technology based on the details of element technologies, which has helped leading packaging working group of Jisso roadmap activity in Japan, as well as contributing to the assembly and packaging technology working group of International Technology Roadmap for Semiconductors (ITRS).

His insight in package technology development can be proved by the fact that Japan's most eminent media, Nikkei, has published his article on package overview and trend in "Nikkei Semiconductor Technology Almanac" and hosted his one-day seminar of packaging technology for four years consecutively. He has contributed to many international conferences as a panelist or an invited speaker, such as at ECTC 2006, ECTC2008, International Workshop on Microelectronics Assembling & Packaging & Reverse Trade Show (MAP 2008), EPTC 2008, ICEP 2009, Semicon West 2009, IMPACT 2009, IMPACT 2010, IMPACT 2011, and EMAP 2012. He published 13 papers and five books and delivered 19 presentations in the past eight years, as well as owns 10 patents.

He is a senior member of IEEE and has served many roles in international societies including the executive chair of ICSJ; the chair of assembly and manufacturing technology program subcommittee, ECTC 2011; a program committee member of EMAP, IMPACT, ECTC, and ESTC; chair of Semi Japan program committee in 2010 and 2011; and a member of ITRS. He is also the secretary of SC47A, IEC (standardization on integrated circuit, International Electrotechnical Commission) and an expert of SC47D, IEC (standardization on semiconductor packaging) and won the Chairman's award of IEC Activities Promotion Committee of Japan in Oct. 2011 and IEC 1906 Award in Oct. 2013.

Newly-Elected and Appointed Members of the CPMT Society Board of Governors

In late 2013, CPMT Society members elected new Members-at-Large to the CPMT Board of Governors for the three-year term of 1 January 2014 through 31 December 2016.

Regions 1–6, 7, 9

NING-CHENG LEE (M '02) Ning-Cheng Lee is the Vice President of Technology of Indium Corporation of America. He has been with Indium since 1986. Prior to joining Indium, he was with Wright Patterson Air Force Base Materials Laboratory (1981–1982), Morton Chemical (1982–1984), and SCM (1984–1986). He has more than 20 years of experience in the development of fluxes and solder materials for SMT industries. In addition, he also has very extensive experience in the development of polymeric packaging materials. His current research interests cover advanced materials for interconnects and packaging for electronics and optoelectronics applications, with emphasis on both high performance and low cost of ownership.

He received his PhD in polymer science on structure-property relationships from University of Akron in 1981. Prior to Akron period, he has studied organic chemistry at Rutgers University in 1976. He received a BS in chemistry from National Taiwan University in 1973.

Ning-Cheng is the author of "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies" by Newnes, and co-author of "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials" by McGraw-Hill. He is also the author of book chapters for several lead-free soldering books. He received 1991 award from SMT Magazine and 1993 and 2001 awards from SMTA for best proceedings papers of SMI or SMTA international conferences, and 2008 award from IPC for Honorable Mention Paper—USA Award of APEX conference. He was honored as 2002 Member of Distinction from SMTA, 2003 Lead Free Co-Operation Award from Soldertec, 2006 Exceptional Technical Achievement Award from CPMT, 2007 Distinguished Lecturer from CPMT, 2009 Distinguished Author from SMTA, and 2010 Electronics Manufacturing Technology Award from CPMT. He served on the board of governors for CPMT, serves on the SMTA board of directors. Among other editorial responsibilities, he serves as editorial advisory board of Soldering and Surface Mount Technology, Global SMT & Packaging and as associate editor for IEEE Transactions on Electronics Packaging Manufacturing. He has numerous publications and frequently gives presentations, invited to seminars, keynote speeches and short courses worldwide on those subjects at international conferences and symposiums.

LI LI (M'01, SM'09) is a Distinguished Engineer at Cisco Systems, Inc. where he leads an initiative on 3D IC integration and advanced packaging development. He has been with Cisco for about 10 years and has 18 years industry experience in IC packaging design, technology development and qualification.

He led the Cisco semiconductor packaging technology team from 2007 to 2009 focusing on high performance package development and qualification for ASIC, PLD, MPU and Memory components supporting all Cisco product families including the industry leading CRS and Nexus routing and switching products. He was promoted to a Cisco Distinguished Engineer in 2008 for his outstanding contributions in advanced technology and supply chain development.

Dr. Li began his career at IBM as an Advisory Engineer. He was part of the team who developed the industry first Flip Chip Plastic Ball Grid Array (FC-BGA) for fast SRAM applications. He led a cross-functional team to develop an optoelectronics package for Philips Electronics' Liquid Crystal on Silicon (LCOS) devices before joining Cisco System.

He is the author of several book chapters and has over 50 technical papers in the field of microelectronics packaging and currently holds 9 US patents. His technical interests include design and manufacturing of advanced packaging and interconnect products, device and package level reliability analysis, 2.5D / 3D IC integration, and System-in-Package.

Dr. Li is a Senior Member of IEEE. He currently co-chairs the Interconnections Committee for the IEEE Electronic Component Technology Conference (ECTC) and has been a member of the ECTC Program Committee since 2007. He represents Cisco on the JEDEC JC-14 and JC-42 committees and is a member of the Board of Directors at HDP User Group International, Inc. (HDPUG), an industry consortium dedicated to high-density electronic packaging. He is also active in the Assembly and Packaging Working Group for International Technology Roadmap for Semiconductors (ITRS) and 3D IC Working Group at Global Semiconductor Alliance (GSA). He volunteers to non-profit organizations in the Bay Area including Habitat for Humanity and Resource Area for Teaching (RAFT).

He received his M.S. and Ph.D. degrees in Mechanical Science and Engineering from the University of Illinois at Urbana-Champaign.

JAMES MORRIS (S'69, M'70, SM'82, F'00) Jim is a Professor of Electrical & Computer Engineering at Portland State University, Oregon, and Professor Emeritus at the State University of New York at Binghamton. His B.Sc. and 1st Class Honors M.Sc. degrees in Physics are from the University of Auckland, New Zealand, and his Ph.D. in Electrical Engineering is from the University of Saskatchewan, Canada. He has served as Department Chair at both Binghamton and Portland, and was the founding Director of Binghamton's Institute for Research in Electronics Packaging. Jim has also held faculty positions at Saskatchewan, Victoria University of Wellington (NZ), and South Dakota School of Mines & Technology, with visiting/sabbatical positions at Loughborough University of Technology, Chemnitz University of Technology, University of Maryland (in CALCE), University of Bordeaux, University of Greenwich, Chalmers University of Technology, Dresden University of Technology, University of Canterbury (NZ), and Helsinki University of Technology (as Nokia-Fulbright Fellow), with honorary appointments at Shanghai University and Shanghai Jiao Tong University. Other positions have included Senior Technician

and Post-Doctoral Fellow at the U of S, brief periods with Delphi Engineering (NZ) and IBM-Endicott, and industrial consulting.

Jim was CPMT Treasurer from 1991 until 1997, an elected BoG member in 1996–1998, and Vice-President for Conferences from 1998 until 2003. As Treasurer, he put the Society on the solid financial foundation which has endured since, and as VP-Conferences oversaw the significant expansion of CPMT conferences outside the USA. He is an IEEE Fellow and CPMT Distinguished Lecturer, won the CPMT David Feldman Outstanding Contribution Award in 2005, and co-chairs the CPMT Nanotechnology Technical Committee. He is an Associate-Editor of the IEEE Transactions on CPMT and has been General Chair of three CPMT-sponsored conferences, Treasurer or Technical Chair of others, and serves on several CPMT conference committees, including the ECTC Interconnections Program Committee, (having previously been a member of the Materials & Processing, Emerging Technologies, and Education committees, chairing two.) As the CPMT Society representative on the IEEE Nanotechnology Council (NTC), he has instituted a regular Nanopackaging column in the IEEE Nanotechnology magazine, established the NTC Nanopackaging Technical Committee, (which also acts as a program committee for annual IEEE NANO conferences,) was the 2010–2013 NTC Awards Chair, chaired the IEEE NANO 2011 conference in Portland, and now serves as the NTC Vice-President for Conferences. He co-founded the Oregon CPMT Chapter in 2002, and currently sits on the joint CAS/CPMT Chapter executive committee. He also belongs to the American Society for Engineering Education and IMAPS, and chairs the Oregon Chapter of the IEEE Education Society, which he co-founded in 2005. This year he is Program Chair of the 1st IEEE Conference on Technologies for Sustainability (SusTech 2013) in Portland.

His research activities are focused on electrically conductive adhesives and the electrical conduction mechanisms in discontinuous thin metal films, with applications to nanopackaging and single-electron transistor nanoelectronics, but with continuing projects in device modeling and sensors too. He is also actively involved in the promotion of international educational exchanges, and in Internet education. He has edited four books on electronics packaging, including "Nanopackaging: Nanotechnologies and Electronics Packaging," which has just been published in Chinese, and co-authored a fifth. This year, he also has had two co-edited books on nanodevices published.

JEFFREY C. SUHLING (A'94, M'01) received a B.S. degree in Applied Mathematics and Physics, and M.S. and Ph.D. degrees in Engineering Mechanics from the University of Wisconsin, Madison, WI. He joined faculty of the Department of Mechanical Engineering at Auburn University in 1985, where he currently holds the rank of Quina Distinguished Professor. Dr. Suhling co-established the NSF Center for Advanced Vehicle and Extreme Environment Electronics (CAVE3) in 1998, and served as Center Director from 2002– 2008. CAVE3 is a government and industry sponsored research center involving over 20 member companies, 15 faculty, and 35 graduate students that specializes in reliability of electronic packaging in harsh environments. In 2008, he was appointed Department Chair of the Department of Mechanical Engineering, which is the largest program at the University with over 1000 undergraduate students and 150 graduate students. He was selected "Outstanding Mechanical Engineering Faculty Member" by the undergraduate students during 1990, received the College of Engineering Birdsong Superior Teaching Award in 1994, and received the College of Engineering Senior Research Award in 2001. He has advised 75 graduate students at Auburn University, including 27 Ph.D. students and 48 M.S. students.

Dr. Suhling has been an active researcher in electronic packaging for over 25 years. His general areas of interest are in the mechanics and reliability of packaging. Specializations include silicon sensors for packaging stress and temperature measurements, stress effects in silicon devices, test chips, mechanical characterization of packaging materials including solders and polymers, solder joint reliability and aging effects, and finite element modeling. He has authored or co-authored over 375 technical publications, including 6 books and book chapters, 55 journal articles, and 325 conference proceedings papers. Six of his conference papers have been selected as the Best of Conference. These include Best Session Paper Awards at the 2005 and 2010 ECTC Conferences, as well as Best Paper Awards at the 1998 and 2002 IMAPS Annual Conferences, 2008 SMTA International, and 2013 InterPACK Conference. In addition, he and his co-authors have received Best Poster awards at the InterPACK 2007, InterPACK 2009, and InterPACK 2013 conferences.

Dr. Suhling is a member of IEEE/CPMT, ASME, IMAPS, and SMTA. In IEEE, he has served on the ECTC Applied Reliability program committee for the past 10 years. He was appointed to the ECTC Professional Development Course (PDC) program committee in 2006, and has served as Assistant Chair from 2008–Present. He has also been active in the IEEE/CPMT ITHERM Conference series, serving on the program committee for over 10 years. In ASME, Dr. Suhling served as Chair of the Electrical and Electronic Packaging Division (EPPD) during 2002–2003, and was on the EPPD Executive Committee from 1998–2003. Dr. Suhling was the Technical Program Chair of the InterPACK '07 Conference, and General Chair of the InterPACK '09 Conference. He was elected a Fellow of ASME in 2009, and was recognized with the ASME-EPPD Mechanics Award for outstanding contributions to electronic packaging research.

Region 8

TONI MATTILA (M'08) is a Senior Director at the investment promotion agency Invest in Finland (IIF), where he is responsible for R&D investments in the field of electronics and ICT. He is also a docent (Adjunct Professor) of Aalto University, Finland. He received his Ph.D. degree in electrical engineering in 2005 and the M.Sc. degree in materials science and engineering in 1999 from the Helsinki University of Technology (HUT). Since 1996, he has been working with electronics production technologies and reliability of electronic devices both in industrial and academic settings.

Before joining IIF in 2013, Toni worked for 14 years with electronics production technologies, soldering in electronics, failure mechanisms of electronic assemblies, and the development of improved methods for reliability assessment and lifetime

prediction at HUT and Aalto University. Within the framework of his research Toni worked in close co-operation with international electronics industry, research institutions and universities. His research has so far resulted in over 50 publications in scientific and technical journals and conferences. In addition, Toni has authored six book chapters, held several professional tutorials at conferences and been a frequent speaker at conferences, seminars and technology fairs. He is also a frequent reviewer in several scientific journals, including CPMT Transactions.

Since 2011, Toni has served as a Member to the CPMT Society Board of Governors and now he is running for his second term. During this time he has also acted as Strategic Regional Director for Europe (Region 8) and established firm contacts with the local CPMT chapters in the region. He is also a member to the society Awards Committee. From 2007 to 2011 Toni was also the Chairman of the CPMT Finland Chapter. During this term he revitalized and developed the local chapter activities together with his board members so that more than 100 people annually attended the seminars and events organized by the CPMT Finland chapter. Toni has also been actively involved with the IEEE Finland Section, where he served as a member of the executive committee from 2008 to 2011, and the secretary of the section in 2010–2011.

Toni's other IEEE activities include a membership of technical committees of all three major CPMT conferences: the Electronics System Integration Technology Conferences (ESTC), the Electronic Components and Technology Conference (ECTC), and the Electronics Packaging Technology Conference (EPTC). Toni is also the executive chair of the forthcoming ESTC conference to be held in Helsinki, Finland in September of 2014. In the past he has also acted in several other positions of trust: for example, he has been the chairman and a member of housing associations for almost 15 years, and he also acted as a treasurer of a student union during his student years.

GILLES POUPON (M'05, SM'10) Gilles Poupon received his formal education at University of Grenoble (France) and Conservatoire National des Arts et Métiers in Paris. He received his M.S. in Electrochemistry in 1985. He joined CEA-LETI, Grenoble, France, in 1987. Since 2004, Gilles was Director of Strategic Programs on Advanced Packaging at CEA-LETI. Subsequently, he became the Manager of the High Density Interconnection and Packaging Laboratory at LETI. He has an extensive experience in technologies relating to micro-systems packaging, 3D integration and silicon interposers. He worked on specific technologies based on wafer level packaging, eWLP, fine pitch & high density interconnections, TSV processes, micro-cooling (silicon heat pipes).

Gilles Poupon has been active in electronic packaging since 2001. He is Senior Member of IEEE (SM'10), Chair of Interconnection committee for ECTC conference in 2013 and Chair of IEEE-CPMT French chapter. He has worked in establishing the IEEE workshops in France and he has been active on the technical committees for ESTC in Europe. Additionally, Gilles is the Technical Director of the French chapter of IMAPS since 2006 and involved in the technical committee of IMAPS European events. He is the Technical Chair of conference EMPC 2013 in Grenoble. Gilles Poupon is a Scientific Advisor of EURIPIDES (European cluster on packaging) and committee member of Smart System Integration Conference (from EPOSS network in Europe). He is also a member of ITRS Assembly & Packaging Technical Working Group. He has published two books (Hermes Science; 2008 and 2011) on advanced packaging and new processes for interconnections. He has authored several chapters of books and co-authored and authored over 50 proceedings papers and journal papers. He has more than 10 patents in the field of advanced packaging, micro systems technologies and 3D integration.

Additionally, the following individuals were appointed to fill in-term vacancies as Members-at-Large:

Regions 1–6, 7, 9

PHILIP GARROU (M'88, SM'92, F'00) consults in the areas of thin film technology, IC packaging and interconnect, microelectronic materials and 3D IC integration for startups and fortune 500 companies. From 2002 – 2004 he was Global Director of Technology and New Business Development for Dow Chemicals Advanced Electronic Materials business. From 1997 – 2002 he was General Manager of Dows BCB dielectric business.

Dr. Garrou is a fellow of both IEEE and IMAPS and has served as President of the IEEE Components, Packaging and Manufacturing Technology Society, CPMT (2004–2005) and IMAPS (1998). Dr. Garrou has been Associate Editor of IEEE Transactions on Components and Packaging. He is currently Contributing Editor and blogger ("Insights from the Leading Edge") for Solid State Technology. He has authored / co-authored > 100 technical publications. He edited and authored the Multichip Module Handbook-for McGraw Hill in 1998 and the Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuitsfor Wiley-VCH, (Vol 1&2) 2008; (Vol 3) 2014.

In 1994 he won the Milton Kiver Award for Excellence in Electronic Packaging and Production for the commercial introduction of CycloteneÔ Advanced Electronics Resins.

Region 8

KARLHEINZ BOCK (M'96) is since 2008 a Professor of Polytronic Microsystems at the faculty of Communication and Electronics Engineering at the University of Berlin. He earned his Diploma on electrical and communication engineering from the University of Saarland, Saarbrücken, Germany in 1986. He worked as a materials scientist and as a systems analyst and consultant before he joined the University of Darmstadt, Darmstadt, Germany in 1989 where in 1994 he received his Dr.-Ing. (Ph.D.) for RF microelectronics. In 2012 he received the Doctor honoris causa of the Polytechnical University of Bukarest in Romania for his work on Polytronics.

Since 2001 he is employed as head of the Polytronic and Multifunctional Systems department at the Fraunhofer Institution for Modular Solid State Technologies in Munich working on advanced technology topics amongst them, thin silicon; thinning, dicing and handling and reliability of components; self-assembly of Si dies and other electronic components; super capacitances (super-Cap);

foil and flexible electronics; organic electronics and sensors; 3D multifunctional and hetero-systems integration & packaging; MEMS acceleration sensors; medical electronics; implantable devices; biosensors with an annual research project volume of several Mio. €.

Karlheinz Bock has secured over € 50 Mio research funding and has been awarded more than 20 patents, and has published over 220 papers. He has given more than 50 invited presentations at universities, research institutions and international conferences and received the "Japan Society for Promotion of Science (JSPS) Award" in 1994 for his PhD thesis. He co-authored 14 best paper awards amongst them the "He Bong Kim Award 2004" at CSMANTECH as well as at SPIE 2012, San Diego, USA and at MES 2012, Osaka Japan. Over the years he has been engaged in developing the technological community of 3D systems hetero-integration and packaging and organic and flexible electronics serving on many technical organizations and conferences. Amongst them he served on the emerging technology committee of the IEEE ECTC conference since 2008 as "Emerging Technologies" sub-committee member and vice chair (2011) and chair (2012). He also served on the ESTC 2012 technical program committee; since 2010 a jury member of the AMA Sensor Innovation Award in Germany and since 2012 as member of the AMA research council; since 2010 as conference co-chair for integrated smart systems ISS at Plastic Electronics in Dresden. Since 2013 he serves as the chair of the international advisor committee of the International Student Professional Contest "Interconnection technologies in Electronics" TIE in Romania. He has been active in different roles as committee member of IEDM since 2008 and in 2012 he served as the European arrangements chair of IEDM. He is active in the Board of Editors of the Micro-and Nanotechnology Journal of Bentham Science Publishers.

To see the full list of CPMT Society Board of Governors members, go to http://cpmt.ieee.org/board-of-governors.html

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Congratulations to IEEE Fellows Class of 2014

Listed below are new IEEE Fellows who are members of the CPMT Society.

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

This year marks the 50th Fellows Class. Over the last fifty years, IEEE has elevated roughly 10,000 members to this honor.

Sheng Liu (China)
For leadership in engineering development of LED packaging.

Bahgat Sammakia (US)
For contributions to thermal management applications in electronic systems.

Peter Sandborn (US)
For contributions to the analysis of cost and life-cycle of electronic systems.

Guoqi Zhang (The Netherlands)
For contributions to heterogeneous micro/nano electronics packaging, system integration and reliability.

Brice Achkir (US)
For contributions to diagnostics of physical layer design in gigabit digital transmission systems.

Daniel Radack (US)
For leadership in microwave and millimeter-wave integrated circuit technologies and packaging techniques.

Bjorn Gustavsen (Norway)
For contributions to frequency-domain modeling techniques.

IEEE Launches New Fellows Directory

IEEE has launched a redesigned Fellows Directory. It is the most comprehensive online search and networking tool available to members. If you need to complete an IEEE Fellow Nomination, gather information for a region, section, or society, it's now easy to accomplish.

The information in the directory can be accessed by six categories: alphabetical by last name, year elevated, gender, IEEE region, IEEE society, and deceased. Within these categories, members can search, sort, or run a filter. For example, a report can be compiled on all Fellows within a specific region elevated in a particular year. The directory allows members to view the profiles of Fellows plus the ability to network with the Fellows. If you are not an IEEE member, you will have limited access to certain information.

Check it out today. The directory works on handheld devices and computers. To access the directory, go to www.ieee.org/fellows, then click the Fellow Directory icon.

New IEEE CPMT Senior Members

The members listed below were elevated to the grade of Senior Member between July and November 2013.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

Michael Caggiano	Richard Joyce	Sakethraman Mahalingam	Ramesh Ramadoss	Daquan Yu
Louis Hart	Detlef Krabe	Michael Osterman	Jean Trewhella	Li-Rong Zheng

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CPMT Webinars

CPMT Webinars allow you to attend lectures on the latest technology development topics within the CPMT Society's scope, presented live, by experts in our field. They typically run from one to one and one half hours, with time allowed for questions and answers.

The webinars are made available as a no-cost benefit for CPMT Members.

Most webinars are recorded. Recordings of and/or presentations from past Webinars can be accessed by CPMT Members in the CPMT Webinar Archive on the CPMT website: http://cpmt.ieee.org/cpmt-webinar-archive.html.

Topics of past webinars include:

- 3D Printing: From Prototype to Production
- Nanomaterials for Printed Electronics
- Thermo-Mechanical and Mechanical Reliability of Electronics
- Platform Independent Photonic Design Tools and Concepts
- Sub-Terahertz Photonics for Ultra-Wideband Wireless Communications
- HELIOS Results/Achievements
- Active plasmonics co-integrated with Si-photonics and electronics for on-chip interconnects
- Advanced Packaging for High Power LEDs
- Electro-optical Printed Circuit Board and Interconnect Technologies and their Application to Data Center and HPC Systems

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More Value for your CPMT Membership

CPMT Members have access to technical content from a variety of sources—available free of charge—as a membership benefit. The CPMT website has a Members Only area with content that includes selected presentations from regional conferences, Chapter workshops, seminars and meetings; recordings and presentation files of past CPMT Webinars; and special offers.

To access Members Only content, go to http://cpmt.ieee.org/members-only.html and log in using your IEEE Web Account.

Publication News....

Have You Read Them? The Most Downloaded CPMT Transactions Papers

What might you be missing in the CPMT literature? Following is a list of most downloaded papers in Fourth Quarter 2013. CPMT members and subscribers can access these and other papers in IEEE Xplore.

"High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)," Joohee Kim; Jun So Pak; Jonghyun Cho; Eakhwan Song; Jeonghyeon Cho; Heegon Kim; Taigon Song; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Min-Suk Suh; Kwang-Yoo Byun; Joungho Kim, *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, Volume: 1, Issue: 2, Digital Object Identifier: 10.1109/TCPMT.2010.2101890, Page(s): 181–195, Feb 2011

Abstract: We propose a high-frequency scalable electrical model of a through silicon via (TSV). The proposed model includes not only the TSV, but also the bump and the redistribution layer (RDL), which are additional components when using TSVs for 3-D integrated circuit (IC) design. The proposed model is developed with analytic *RLGC* equations derived from the physical configuration. Each analytic equation is proposed as a function of design parameters of the TSV, bump, and RDL, and is therefore, scalable. The scalability of the proposed model is verified by simulation from the 3-D field solver with parameter variations, such as TSV diameter, pitch between TSVs, and TSV height. The proposed model is experimentally validated through measurements up to 20 GHz with fabricated test vehicles of a TSV channel, which includes TSVs, bumps, and RDLs. Based on the proposed scalable model, we analyze the electrical behaviors of a TSV channel with design parameter variations in the frequency domain. According to the frequency-domain analysis, the capacitive effect of a TSV is dominant under 2 GHz. On the other hand, as frequency increases over 2 GHz, the inductive effect from the RDLs becomes significant. The frequency dependent loss of a TSV channel, which is capacitive and resistive, is also analyzed in the time domain by eye-diagram measurements. Due to the frequency dependent loss, the voltage and timing margins decrease as the data rate increases.

URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5739019&isnumber=5739011

"Through-Silicon-Via-Based Decoupling Capacitor Stacked Chip in 3-D-ICs," Eunseok Song; Kyoungchoul Koo; Jun So Pak; Joungho Kim, *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* Volume: 3, Issue: 9, Digital Object Identifier: 10.1109/TCPMT.2013.2257928, Page(s): 1467–1480, Sep 2013

Abstract: In this paper, a new decoupling capacitor stacked chip (DCSC) based on extra decoupling capacitors and through-silicon-vias (TSVs) is proposed to overcome the narrow-bandwidth limitation of the conventional decoupling capacitor solutions in three-dimensional-integrated circuits (3-D-ICs), as exhibited by expensive on-chip metal-oxide-semiconductor (MOS) decoupling capacitors and inductive off-chip discrete decoupling capacitors. In particular, in comparison to the on-chip decoupling solutions, such as MOS, metal-insulator-metal and deep trench capacitors, the proposed TSV-based DCSC represents several advantages, such as small leakage currents, large capacitances ranging from tens of nF to a few µF, low equivalent series inductance (ESL) with tens of pH, and high flexibility in TSV arrangements. The proposed TSV-based DCSC can be applied by mounting decoupling capacitors, such as Si-based MOS capacitors and discrete capacitors, on the backside of a chip and connecting the capacitors to the on-chip power delivery network (PDN) through TSVs. To demonstrate the performance of the proposed DCSC structure, a segmentation method was applied to compare the PDN impedance (Z11) of the TSV-based DCSC with those of the well-known conventional decoupling capacitor methods. The TSV-based DCSC was found to exhibit the advantages of both low on-chip level ESL (under several tens of pH) and high off-chip level capacitance (up to several µF). Additionally, the PDN impedance properties of the TSV-based DCSC were analyzed with respect to the variations in the number of power/ground TSV pairs, on-chip PDN size, and capacitance values of the stacked off-chip discrete decoupling capacitors using the segmentation method.

URL: http://ieeexplore.ieee.org/xpl/login.jsp?tp=arnumber=6549141

"Broadband and High-Efficiency Power Amplifier That Integrates CMOS and IPD Technology," Hwann-Kaeo Chiou; Hua-Yen Chung; Yuan-Chia Hsu; Da-Chiang Chang; Ying-Zong Juang, *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, Volume: 3, Issue: 9, Digital Object Identifier: 10.1109/TCPMT.2013.2266119, Page(s): 1489–1497, Sept 2013

Abstract: This paper presents a broadband and high-efficiency integrated CMOS-integrated passive device (IPD) power amplifier (PA) with heterogeneous integration of active devices that are fabricated using 0.18 µm CMOS technology and passive components that are fabricated using IPD technology. The passive components that are fabricated using IPD technology have the advantages of high-Q, low-loss performance, and low cost. By replacing the conventional series resonant output matching network of class-E PA with a broadband Ruthroff-type transmission line transformer (TLT), the proposed PA exhibits broadband characteristics. It performs efficiently owing to the benefits of the low-loss TLT and the switching mode operation of the class-E PA. The measurements demonstrate an output power of more than 25.64 dBm and a power-added efficiency (PAE) of more than 40.2% over the bandwidth from 2 to 3 GHz. The peak output power and PAE are 26.18 dBm and 47.4%, respectively.

URL: http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=6573340

"Low-Loss Broadband Package Platform With Surface Passivation and TSV for Wafer-Level Packaging of RF-MEMS Devices," Bangtao Chen; Sekhar, V.N.; Cheng Jin; Ying Ying Lim; Toh, J.S.; Fernando, S.; Sharma, J., *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* Volume: 3, Issue: 9, Digital Object Identifier: 10.1109/TCPMT.2013.2263932, Page(s): 1443–1452, Sept 2013

Abstract: Packaging of radio frequency (RF) microelectromechanical system (MEMS) devices requires a good electrical performance, and thus requires the parasitic effects of packaging to be minimal. This paper presents the design, fabrication, and characterization of improved low-loss wafer-level packaging (WLP) platform with through-silicon-via (TSV) interposer for RF-MEMS packaging. The insertion loss because of parasitic effects is reduced using optimized grounding configuration and surface passivation. The coplanar waveguide (CPW) test vehicle, high-frequency antenna, RF tuner, and film bulk acoustic resonator (FBAR) filter are fabricated and characterized using the developed WLP platform with TSV. To determine the RF performance of the package, the CPW transmission lines are fabricated on high-resistivity Si substrates, and the grounding configuration is optimized. The fabrication of the RF-MEMS WLP involves the process of a TSV cap wafer and CPW transmission lines or RF MEMS on the substrate wafer. TSV cap process includes TSV etching, void-free TSV plating, and redistribution layer postprocess on thin TSV wafer. The electrical characterization of the fabricated devices is performed. The optimized model has a wide bandwidth of 26.5 GHz and a packaging loss of 0.1 dB at 10 GHz. This implies that the effect of packaging on the performance of RF device is expected to be minor. The developed WLP platform is used for the 94-GHz antenna, RF tuner, and FBAR filter packaging and the characterization of RF-MEMS devices is presented.

URL: http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=6545340

"Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring," Jonghyun Cho; Eakhwan Song; Kihyun Yoon; Jun So Pak; Joohee Kim; Woojin Lee; Taigon Song; Kiyeong Kim; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Minsuk Suh; Kwangyoo Byun; Joungho Kim, *Components, Packaging and Manufacturing Technology, IEEE Transactions on*, Volume: 1, Issue: 2, Digital Object Identifier: 10.1109/TCPMT.2010.2101892, Page(s): 220–233, Feb 2011

Abstract: In three-dimensional integrated circuit (3D-IC) systems that use through-silicon via (TSV) technology, a significant design consideration is the coupling noise to or from a TSV. It is important to estimate the TSV noise transfer function and manage the noise-tolerance budget in the design of a reliable 3D-IC system. In this paper, a TSV noise coupling model is proposed based on a three-dimensional transmission line matrix method (3D-TLM). Using the proposed TSV noise coupling model, the noise transfer functions from TSV to TSV and TSV to the active circuit can be precisely estimated in complicated 3D structures, including TSVs, active circuits, and shielding structures such as guard rings. To validate the proposed model, a test vehicle was fabricated using the Hynix via-last TSV process. The proposed model was successfully verified by frequency- and time-domain measurements. Additionally, a noise isolation technique in 3D-IC using a guard ring structure is proposed. The proposed noise isolation technique was also experimentally demonstrated; it provided –17 dB and –10 dB of noise isolation between the TSV and an active circuit at 100 MHz and 1 GHz, respectively.

URL: http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=5739017&isnumber=5739011

Book Review

Encyclopedia Of Thermal Packaging
Set 1: Thermal Packaging Techniques (A 6–Volume Set)
Avram Bar-Cohen (University of Maryland, USA), Editor

Reviewed by: Daniel N. Donahoe, Ph.D., P.E.
1000 kilometers® IEEE CPMT Member
Licensed Professional Engineer—Arizona, California, Utah
Certified Reliability Engineer

This is a review of the first six-volume set of the planned four multi-volume sets which will compose the comprehensive, seminal multi-set *Encyclopedia of Thermal Packaging*. published by World Scientific Publishing Company The first six volumes are appropriately titled *Thermal Packaging Techniques* and were assembled by Editor-in-Chief Avram Bar-Cohen (Avi). His expertise was introduced to practicing engineers, certainly to myself, by his 1983 book co-authored with the late Alan Kraus focused on practical applications of heat transfer engineering. That book was titled *Thermal Analysis and Control of Electronic Equipment*.

Often great accomplishment springs from great mentorship. Avi began his career at MIT under Dr. Arthur E. Bergles; Dr Bergles was granted the ASME Medal, the highest ASME award granted for eminently distinguished engineering achievement. Allan Kraus was likewise honored with an ASME award in his name, The Allan Kraus Thermal Management Medal to recognize individuals who have demonstrated outstanding achievements in thermal management of electronic systems and their commitment to the field of thermal science and engineering. I have likewise benefited from Avi's gracious advice. It is my pleasure to review his new encyclopedia.

In this first set of his encyclopedia, Avi has selected six "building block" topics. These topics range from topics of current research, concepts not yet productized, to current challenges in advancing latest technologies, to practical thermal engineering. The volume authors are themselves noted experts in each topic. In this spirit of celebrated experts, the encyclopedia introduction is authored by Dr. Wataru Nakayama.

Two volumes describe the fundamentals of electronics cooling. Volume 2 covers the classic approach to electronics cooling that remains the linchpin of electronics cooling, the "cold plate". It is authored by Allan Kraus who died in 2012. Avi begins the volume with his moving eulogy for his old friend, Allan, delivered in the Spring of 2012 at Allan's funeral in Cleveland. Volume 6 further expands on the fundamentals of electronics cooling design by addressing experimental design. Readers from industry will appreciate that thermal design and required agency compliance of products is rooted in measurement. The author is Professor Gary Solenbrekken from the University of Missouri.

Three volumes focus on an approaches to the thermal power barrier threatening to constrain the advancement of the integrated circuit (~100 Watts per square centimeter) along past evolutionary performance trajectories. In Volume 1 that approach is the microchannel as first describe by Tuckerman and Pease in 1981. Volume 1 describes the state of the art based on the work by Professor Suresh Garimella and his students at Purdue University. His coauthor is Dr. Tannaz Harrirchian currently with Intel. As the volume reveals, this approach remains an active research topic. Volume 3 continues to address these thermal limits but by using an older technology, direct immersion in dielectric liquids. The text of volume 3 covers stacked ICs, the latest embodiment of the early "cordwood" approach to packaging. Professor Bar-Cohen coauthored this volume with Dr. Karl Geisler from 3M Corporation, the primary manufacturer of dielectric fluids. The text includes a useful one-stop compilation of dielectric fluid properties. Volume 4, reviews another standard approach that can be applied to high power ICs or to cold plates, the thermoelectric module. Appropriately, my own first engineering assignment at Lockheed was a thermoelectric cold plate. This volume reviews significant advancements and the current state of the art in thermoelectric coolers, especially for applications to IC hot spots. The authors are Professor Bao Yang and Dr. Peng Wang from the University of Maryland.

Volume 5 is dedicated to an exciting and current design application, solid state lighting (SSL). SSL promises to replace other forms of lighting in buildings and in vehicles by offering superior lifetimes, much better efficacy (lumens per watt) with less environmental impact due to both dramatic reduction in energy consumption and less polluting raw materials. However, major technical hurdles remain; the cost of these devices remains high. In the short term, these implementation are packaging and thermal hurdles. In the long run, there are in device physics and packaging research challenges. The chapter on OLED challenges addresses such challenges. Appropriately, one author is from academia and three are from industry. These authors are Professor Mehmet from Ozyegin Univeristy and Dr. Anat Setlur, and Dr. Joseph Shinag and Standon Weaver from General Electric. As expected due to the device physics challenges, the GE team is interdisciplinary.

Reading this encyclopedia brings back fond memories of my days as an undergraduate reading about applications of the thermal sciences in the volumes of Advances in Heat Transfer and in the ASHRAE Handbooks. The field of electronics still offers engineering and scientific challenges for those of us who share the passion for pursuit of electronics technology, especially those thermal challenges presented by electronics. Therefore, engineers and scientists performing R&D tasks involving electronics packaging and system integration, as well as engineers in industry, researchers in academia or students, should not be without this unique Encyclopedia, including the current Set 1, as well as subsequent Sets 2-4. This exceptionally helpful engineering tool is offered in both print and electronic versions, the latter available for licensing from the World Scientific Publishing Company.

IEEE Xplore® Table of Contents Alert

Any technologist – **member or non-member** – is welcome to receive alerts when upcoming issues of our CPMT *Transactions* are posted to the IEEE's Xplore database and all the papers are available for downloading. This is a handy way to scan the issue's Table of Contents and quickly learn about novel approaches to packaging, modeling, reliability, materials, assembly and other topics.

The website link is:ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

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Transactions on Components, Packaging and Manufacturing Technology
Transactions on Semiconductor Manufacturing

Conference News....

2014 International Conference on Electronic Packaging Technology

12~15, August, 2014, Chengdu China

Call for Papers

The 15th International Conference on Electronic Packaging Technology (ICEPT 2014) will be held in **Chengdu, China, from August 12 to 15, 2014**. The ICEPT 2014 is organized by Electronic Manufacturing and Packaging Technology Society (EMPT) of Chinese Institute of Electronics (CIE) and co-organized by University of Electronic Science and Technology of China. As one of the most famous international conferences on electronic packaging technology, the conference has received strong support from IEEE CPMT and active involvement from IMAPS and iNEMI, and was highly appreciated by CIE and China Association for Science and Technology (CAST).

ICEPT 2014 is a four-day event, featuring technical sessions, invited talks, professional development courses, exhibition, and social networking activities. It aims to cover the latest technological developments in electronic packaging, manufacturing and packaging equipment, and provide opportunities to explore the trends of research and development, as well as business in China. .

CONFERENCE THEMES

- **Advanced Packaging:** BGA, CSP, flip ship; COB WLP, POP/PIP; TSV, 3D integration; high density substrate; and other advanced packaging and integration technologies.
- **System Integration:** 3D integration by TSV, SIP, Test methodologies for 3D packaging and system level packaging.
- **Packaging Materials & Processes:** Green materials, nano-materials, and other novel materials for packaging performance enhancement and cost reduction; various new packaging/assembly processes.
- **Packaging Design and Modeling:** Novel packaging/assembly designs; methodologies for modeling, simulation and validation of electrical, thermal, optical and mechanical performance of various electronics packages; multi-scale and multi-physics modeling, process simulation.
- **Inter-connection technologies:** High density inter-connection technologies; advanced bonding technologies; substrate solution for 3D packaging; non-conventional inter-connection technologies.
- **Advanced Manufacturing Technologies and Packaging Equipment:** Packaging/assembly equipment (wafer thinning); test technologies; technologies for manufacturability and yield improvement, cost reduction and service performance improvement.
- **Quality & Reliability:** Quality monitoring and evaluation; methodologies for accelerated reliability data collection and analysis, reliability modeling and life prediction, failure analysis and non-destructive diagnose.
- **Solid State Lighting Packaging & Integration:** Methodologies for design, manufacturing and test of high power LED module; LED packaging/integration technologies and their applications in LCD, micro-projector, in-door lighting, street lamp, etc.
- **Microwave and Power electronics Packaging:** Components and modules for RF/mmW/THz systems; power devices; microwave device packaging; power electronics packaging; automobile electronics packaging.
- **Emerging Technologies:** MEMS, NEMS, and MOEMS; optoelectronics packaging; medical electronic device packaging; wearable/flexible electronics packing; sensors, actuators, nano-devices, etc.

IMPORTANT DATES

- **April 21, 2014** — **Deadline for Submission of Abstract**
- **May 12, 2014** — **Notification of Acceptance**
- **June 30, 2013** — **Deadline for Submission of Manuscript**

SUBMISSION OF ABSTRACT

Abstracts are solicited to describe original and unpublished work. The abstract should be approx. 500 words and contains a clear statement of the background, methodology, results, conclusions, and important references of the work. All abstracts and papers must be in English and should be submitted through https://www.easychair.org/conferences/?conf=icept2014.

The template for abstract submission can be downloaded at the conference website http://www.icept.org. Selected papers will be recommended for publication in IEEE/CPMT journals.

BEST CONFERENCE PAPERS AND BEST STUDENT PAPERS

The conference proceeding is an official IEEE publication. Best Conference and Student Papers will be selected and awarded at the conference.

CALL FOR PROFESSIONAL DEVELOPMENT COURSES

The conference program includes professional development courses (PDC), and the leading experts in the field may e-mail to icept2014@163.com for details.

CALL FOR EXHIBITION/SPONSORSHIP

A tabletop exhibition featuring suppliers of materials, equipment, components, software, manufacturers, and service providers of the electronics packaging and related industries will be held during the conference. Potential exhibitors and sponsors may e-mail to icept2014@163.com for details.

General Chair: Prof. Keyun BI

Technical Chairs: Prof. Bangchao Yang, Prof. Bo Zhang

Conference Website: http://www.icept.org

Conference E-mail: icept2014@163.com

ABOUT Chengdu

Chengdu, located in southwest People's Republic of China, is the capital of Sichuan province and a sub-provincial city. Chengdu is also one of the most important economic centers, transportation and communication hubs in Southwestern China. According to the 2007 Public Appraisal for Best Chinese Cities for Investment, Chengdu was chosen as one of the top ten cities to invest in out of a total of 280 urban centers in China.

More than four thousand years ago, the prehistorical Bronze Age culture of Jinsha established itself in this region. The fertile Chengdu Plain, on which Chengdu is located, is called Tian fu zhi guo in Chinese, which literally means "the country of heaven", or more often seen translated as "the Land of Abundance". It was recently named China's 4th-most livable city by China Daily.

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iMPACT International Microsystems, Packaging, Assembly and Circuits Technology conference

EMAP 2014 16th International Conference on Electronic Materials and packaging

IMPACT-EMAP 2014

Call for Papers

Consumer Electronics Association (CEA) identifies the five tech trends for 2014: the Internet of Things (IoT), driverless cars, digital health care, robotics and content curation. The research report shows their potential to enrich our lives, and in some cases, massively change them. To reflect the cutting-edges technology development, the theme of IMPACT-EMAP 2014 highlights "Challenge for Change-Shaping the Future" and will arrange keynote speeches, invited talks, industrial sessions and outstanding paper presentations. The IMPACT Conference is the largest gathering of packaging and PCB professionals in Taiwan, attracting over 3,600 attendees in accumulated total over the past few years.

This year, the 9th IMPACT (International Microsystems, Packaging, Assembly, Circuits Technology) Conference will be held in conjunction with the 16th EMAP (International Conference on Electronics Materials and Packaging) which just rotates to Taipei. IMPACT Conference keeps collaborating with International organizations such as ICEP from Japan and iNEMI from U.S.A. The IMPACT Conference is an amazing convergence of microsystems knowledge and community via bridging the industries and academia. IMPACT is committed to helping you fulfill your increasingly demanding role in the R&D department, and providing more contents relevant to your needs and goals than ever before!

Call for Paper

Conference: IMPACT-EMAP 2014 (The 9th IMPACT and 16th EMAP Joint Conference) **Exhibition:** TPCA Show 2014

Theme: Challenge for Change-Shaping the Future

Date: Oct 22 (Wed)-24(Fri), 2014 **Venue**: Taipei Nangang Exhibition Center

On-line Submission: www.impact.org.tw

SCOPE OF PAPER SOLICITED

IMPACT

Packaging	PCB
P1 -Advanced Packaging Technologies	B1. Green Materials and Process
P2. Green Packaging	B2. Test, Quality, Inspection and Reliability Technology
P3-3D Integration	B3. HDI and Embedded Technology
P4-LED & Optoelectronics Packaging	B4. Electro Deposition and Electrochemical Processing Technology
P5-Interconnections & Nanotechnology	B5. Advanced and Emerging Technology
P6-Modeling, Simulation & Design	B6. Mechatronics and Automation
P7-Thermal Management	B7. Marketing & Management
P8- Advanced Sensor & Microsystems Technology (MST)	
P9-Advanced Materials, Automatic Process & Assembly	
P10-Emerging Systems Packaging Technologies	

EMAP

Materials and Packaging	
M1. Materials and Processing	M2. Passive and Active Components
M3. Optoelectronics / Photonics	M4. Sensor, Actuator, and Transducer Technologies
M5. Advanced Packaging	M6. Thru Silicon Via (TSV) Technology
M7. Interconnection Technologies	M8. System-in-Package (SiP) and 3D Stacked Die Packaging
M9. Electrical Modeling, Characterization, and Signal Integrity	M10. Thermal-Mechanical Modeling and Characterization
M11. Quality and Reliability	M12. Packaging Technologies for High Brightness LEDs
M13. Flexible Electronics	M14. Others

* Papers relevant with the above scopes are encouraged to submit but NOT limited to.* Conference authority keeps the right to final session arrangement.

Abstract Submission Deadline	June 15, 2014	400-500 words Submit on-line through conference website
Abstract Acceptance Notification	July 14, 2014	Notice sent via email
Online Registration Opens	July 28, 2014	
Advance Program Online	August 11, 2014	Advanced program announcement
Full Paper Submission (Camera-ready Version)	August 15, 2014	4 pages including figures and tables Submit on-line through conference website and copyright forms due

* Authors of accepted papers including oral presentation and posters should register before the deadline; please be noted that un-registered (paid) papers will be removed from the symposium program. * The secretariat keeps the right to modify the agenda.

Technical Program Chair: Hsiang-Chen Hsu, PH.D. 徐祥禎, Tel: +886-7-6577711 #3201, Email: liaison@isu.edu.tw

Secretariat: Taiwan Printed Circuit Association (TPCA), Tel: +886-3-3815659 #405 Sylvia 楊庭芳, Email: service@impact.org.tw

23rd IEEE International Conference on

Electrical Performance of Electronic Packaging and Systems

EPEPS 2014

October 26-29, Portland, OR, USA

Call for Papers

EPEPS is the premier international conference on advanced and emerging issues in electrical modeling, measurement, analysis, synthesis and design of electronic interconnections, packages and systems. It also focuses on new methodologies and CAD/design techniques for evaluating and ensuring signal, power and thermal integrity in high-speed designs. EPEPS is jointly sponsored by the IEEE Components, Packaging and Manufacturing Technology Society and IEEE Microwave Theory and Techniques Society. Authors are invited to submit papers describing **new technical contributions related to the broad area of electrical performance of high-performance interconnect systems**, covering:

1) **Emerging and advanced issues**
2) **New design techniques and innovative architectures**
3) **Novel CAD concepts, methodologies and algorithms for modeling, simulation and optimization**

with emphasis on:

- System-level, board-level and on-chip interconnects
- High-speed channels, links, backplanes, serial and parallel interconnects, SerDes
- Low power mobile and personal applications
- Multiconductor transmission lines
- Memory and DDR interfaces
- Jitter and noise management
- Signal and thermal integrity
- Power integrity and power distribution networks
- Electronic packages and microsystems
- 3D interconnects, 3D packages, TSVs and MCMs
- Nano interconnects and nano structures
- RF/microwave packaging structures, RFICs, mixed signal modules and wireless switches
- Package/chip co-design
- Electromagnetic (EM) and EM interference modeling, simulation algorithms, tools and flows
- Macromodeling and model order reduction as it applies to electrical analysis
- Advanced and parallel CAD techniques for signal, power and thermal integrity analysis
- Measurement and data analysis techniques for system-level and on-chip structures.

Submission Deadline: **June 16, 2014 8pm, PST**

Submission Format: **2 column, 4 page pdf format only.**

Information for authors can be found at www.epeps.org. Submitted manuscripts should be camera ready and compliant with the general standards of the IEEE, including appropriate referencing. Noncompliant manuscripts will not be considered for review.

Location: Portland, OR

Tutorials: EPEPS offers tutorials on state-of-the-art topics during the conference.

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2014 ASTR Workshop
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Submit Papers to the 2014 Accelerated Stress Testing & Reliability (ASTR) Workshop

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- Integration of design modeling, analysis and accelerated testing: the intelligent approach to reliability
- Accelerated testing within a lean culture: Focusing test effort
- Accelerated-testing of complex, safety-critical systems: Quantifying assurance
- Accelerated testing for aging systems: Extending End-of-Life

Please provide abstracts of no more than 300 words, describing your work, its value, context and relevance to the ASTR theme and topics. Abstracts must be in WORD format with the following naming convention:

- Abstract-Last Name-Shortened Title-ASTR2014 (dash between each section)
- 75 character limit for total filename

Date	Milestone
4/30/14	**Abstracts due**
5/15/14	**Notification to speakers of provisional acceptance**
5/30/14	**Upload abstracts to website**
6/30/14	**Draft presentations due**
7/30/14	**Early registration deadline**
8/01/14	**Presenter's registration due date**
8/15/14	**Final presentations due**

IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 8 - 11, 2014, in San Diego, CA, USA http://www.swtest.org/index.html

The Semiconductor Wafer Test Workshop is the only IEEE Components, Packaging, Manufacturing Technology (CPMT) Society event that focuses on all the aspects associated with microelectronic wafer and die level testing.

The conference has a mixture of manufacturer and vendor presentations. It is not a sales show, nor an academic or theoretical conference. It is a probe technology forum where attendees come to learn about recent developments in the industry and exchange ideas. There is a relaxed atmosphere with social activities and plenty of time for informal discussion and networking.

The two and one half-day event starts Sunday afternoon with registration, a reception, a buffet dinner, and a panel discussion. The conference adjourns on Wednesday at noon, in time to get most participants back to work by Thursday morning. SWTW has grown to almost 500 attendees with more international visitors each year.

William R. Mann Memorial Student Fund

Sponsored by the family and friends of William R. Mann and administered by the IEEE Computer and Components, Packaging, & Manufacturing Technology Societies, the **William R. Mann Memorial Student Travel Grant** program awards travel grants to undergraduate or graduate students attending an accredited university or college who will attend, present a paper or participate at either the IEEE International Test Conference or the IEEE Semiconductor Wafer Test Workshop (one grant each per year). Please contact SW Test General Chair for more information.

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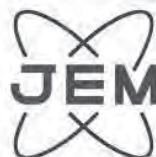

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EPTC 2014
16th Electronics Packaging Technology Conference
3 – 5 December, Marina Bay Sands, Singapore

CALL FOR PAPERS

ABOUT EPTC

The 16th Electronics Packaging Technology Conference (EPTC 2014) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society.
EPTC 2014 will feature technical sessions, short courses/forums, an exhibition, social and networking activities. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.
Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new development in the following categories:

- **Advanced Packaging:** Flip-chip and wire-bond packaging, embedded passives and actives on substrates, 3D System in Packaging, etc.
- **TSV/Wafer Level Packaging:** Wafer level packaging, embedded chip packaging, 2.5D/3D integration, TSV, Silicon interposer, RDL, bumping technologies, etc.
- **Interconnection Technologies:** Wire-bond technology, Flip-chip technology, solder alternatives (ICP, ACP, ACF, NCP), die attachment (Pb-free), etc.
- **Emerging Technologies:** Packaging technologies for MEMS, biomedical, optoelectronics, photovoltaic, printed electronics, wearable electronics, Photonics, LED, etc.
- **Materials & Processes:** Materials and processes for traditional and advanced microelectronic systems, MEMS, solar, green and biomedical packaging.
- **Electrical Modeling & Simulations:** Power plane modeling, signal integrity analysis of substrate/package.
- **Mechanical Modeling & Simulations:** Thermo-mechanical, moisture, fracture, fatigue, vibration, and drop impact modeling, Chip-package interaction, etc.
- **Thermal Characterization & Cooling Solutions:** Thermal modeling and simulation, component and system level thermal management and characterization
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IMPORTANT DATES

Online abstract submission start	1st April 2014
Closing of abstract submission	30th May 2014
Notification of acceptance	29th July 2014
Submission of manuscript	22nd September 2014

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited to describe original and unpublished work. The abstract should be at least 500 words and it must clearly state the purpose, methodology, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well. Authors can choose between oral or poster presentation. Accepted papers have to be registered and presented (oral & poster) in the conference by the authors, then will be published in IEEE Xplore.
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Location: Belgium
Dates: April 7–9, 2014

Name: 2014 IEEE 18th Workshop on Signal and Power Integrity (SPI)
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Name: 2014 25th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)
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