Components, Packaging, and Manufacturing Technology Society Newsletter

The Global Society for Microelectronics Systems Packaging

Vol. 28 No. 1, March 2005 (ISSN 1077-2999)

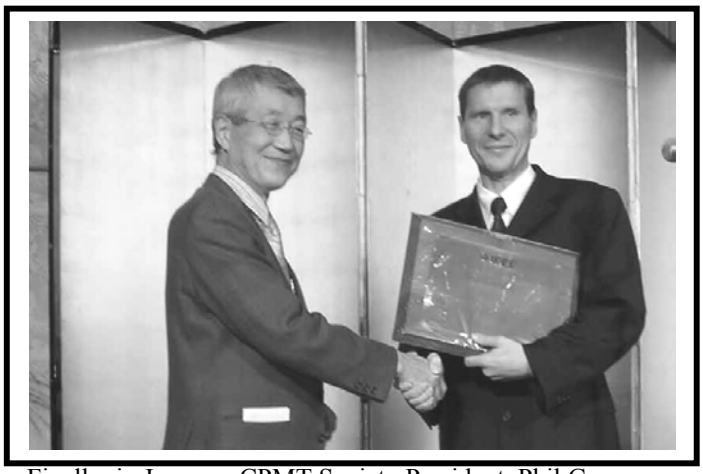
www.cpmt.org
www.ewh.ieee.org/soc/cpmt/newsletter

Special Recognition to Some Very Important International Volunteer Leaders - President's Report

The CPMT Society has been graced over the years with many dedicated volunteers from all corners of the globe. To recognize the efforts of these individuals, the Society recently presented "Presidents Awards" to thank several of these volunteers who have contributed their time and energy to advance the Microelectronics Industry and our Society's mission.

During the 7th VLSI Packaging Workshop, held in Japan last December, Rolf Aschenbrenner, Technical Vice President of the CPMT Society presented George Harman, NIST and IEEE Fellow, a certificate of recognition for "… a lifetime of contributions to the electronics industry and the CPMT Society". George (SM'75-F'82), who worked his entire career at NIST(NBS), received the B.S. degree in l physics from the VPI and his M.S. in physics from University of Maryland. He has published over 60 papers, two books on wire bonding, eight book chapters, and has four patents. George has received many awards from the IEEE, IMAPS, DVS, SME, and NIST. He is a Fellow Emeritus of the National Institute of Standards and Technology, and has been a Research Fellow at the University of Reading, UK. He chaired the IEEE CPMT Fellows committee for 15 years. He is on the ITRS Roadmap Committee for Assembly and Packaging. Currently he serves as a National and International consultant in the field of wire bonding and electronic packaging.

Rolf also presented Kanji Otsuka , Meisei University with a lifetime contribution commendation to recognize "… his many contributions to CPMT Society activities in the Far East region, especially the founding of the VLSI packaging workshop". Professor Otsuka, (F'98) received his PhD in Materials Science from Tokyo Institute of Technology. He worked for Hitachi Ltd. From 1959 to 1992 in semiconductor group and then the computer group, in charge of materials and package design and development for semiconductors and computers. Since 1992, he has been a professor of Electronics and Computer Science at Meisei University.. He has been the Dean of Faculty of Informatics from 2001 to now. He has been involved with many IEEE/CPMT activities, especially the VLSI Packaging Workshop in Japan of which he was the founder.



Finally, in January, CPMT Society President, Phil Garrou, presented Herbert Reichl of Fraunhofer IZM (Germany), 2003 IEEE Fellow, with recognition of his lifetime of technical achievement in microelectronics as "…a scholar, mentor and global leader" . . Prof. H. Reichl studied Electrical Engineering at the Technical University Munich and received his Doctor Degrees in 1974. He was a scientific assistant at Fraunhofer

(continued on page 3)

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Next News Deadline: March 5, 2005

Members-only Web:
UserName: xxxx (don't tell non-members)
Password: xxxxxxxxx (starting April 30)
current/old codes: xxxx xxxxxx

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TC-GEMP (21) Green Electronics Manufacturing and Packaging, Hansjoerg Griese, Email: griese@izm.fhg.de
TC-NANO Nano Packaging -- Rao Tummala, Georgia Tech, rao.tummala@ee.gatech.edu

****IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 park Avenue, 17th Floor, New York, NY 10016-5997. 41.00 per member per year (included in Society fee) for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. periodicals postage paid at New Your,, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved, copyright(c) 2005 by the CPMT Society of IEEE. Authors and Artists given full permission for further use of their contributions. For circulation information call IEEE customer Service 908 981 1393, or FAX 9667.

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Institute IFT and became head of the department "Semiconductor Technologies" and later head of the department "Sensor and Application Techniques". In 1981 he became a professor at the Technical College Munich.

Since 1987 he is professor for Packaging and Interconnection Technologies at the Technical University Berlin and head of the Research Center Microperipherics. Since 1993 he is also head of the Fraunhofer IZM Berlin. In 1996 he further became Head of the Board of Directors of the Fraunhofer Group Microelectronics.

Prof. Reichl has written and co-authored 6 books and more than 500 articles. Prof. Reichl holds more than 50 patents, mainly in the field of packaging and interconnection technologies. He is also editor or scientific supervisor of several technical journals. In 2000 he was honored with the "Bundesverdienstkreuz" of the Federal Republic of Germany.
Congratulations to these 3 honorees who have made great advances in our field and have served CPMT well.

--submitted by Phil Garrou, President CPMT Society

NOTICE TO CPMT SOCIETY MEMBERS

AMENDMENTS TO SOCIETY CONSTITUTION AND BYLAWS

At its November 2004 meeting, the CPMT Board of Governors (BoG) approved amendments to its Constitution and Bylaws. The amendments have also been approved by the IEEE Board of Directors and the IEEE Technical Activities Board, as required.

The first amendment, affecting both the Constitution and Bylaws, relates to the officer positions on the BoG. The second amendment, affecting only the Bylaws, relates to the election of BoG Members-at-Large.

In order for the amendment to the Constitution to take effect, it must be published in the Society TRANSACTIONS or Newsletter, or otherwise publicized by direct mailing to the membership with notice that they go into effect unless 40 or more Society members object in writing within 30 days. If such objections are received, a copy of the proposed amendment shall be mailed with a ballot to all members of the Society at least 30 days before the date appointed for return of the ballots, and the ballots shall carry a statement of the time limit for their return to the IEEE office. Approval of the amendment by at least two-thirds of the ballots legally cast shall be necessary for its enactment.

In order for the amendments to the Bylaws to take effect, they must be published in the Society TRANSACTIONS or Newsletter for information only.

The amendments are summarized below. Any CPMT member wishing to file an objection to Amendment 1-- BoG Officer Positions, should contact the CPMT Executive Office by e-mail, fax or mail by no later than 25 April 2005. Please include your name and contact information, your IEEE member number, and the reason for your objection.

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Amendment 1 - Board of Governors Officer Positions
(Amendment to Constitution and Bylaws)
Background and Rationale:

Several changes have taken place over the past few years that have changed the way the Board of Governors and Society Officers operate.

Key among these changes is the opening of the Society Executive Office. The Executive Office has taken over some functions and responsibilities previously handled by Officers and other volunteers. As a result, the following changes will be implemented to reflect the current operational mode:
Secretary: "responsible for keeping the records of the BoG in the areas commonly ascribed to its function (prepare and distribute reports, notices, or such documents as may be required by the President and BoG.)"
Executive Office performs these functions. Change: Eliminate position.
Treasurer: "responsible for keeping the records of the BoG in the areas commonly ascribed to its function (prepare and distribute reports, notices, or such documents as may be required by the President and BoG."
Executive Office performs most of these traditional functions. Change: Elevate position to Vice President, Finance to reflect focus on strategic responsibilities as opposed to operational functions.

Another key change in Society operations is the establishment several years ago of Strategic Program Directors in a number of key areas such as Membership, Chapters, International Relations and Awards. As a result, the following change will be implemented to reflect the current operational mode:
Vice President, Administrative: "responsible for providing the direction and coordination of the administrative activities of the Society, including the Membership, Publicity, Chapter Development, Nominations, Awards and Fellows, International Relations, the Constitution and Bylaws Committee Chairs, and the IEEE and TAB representatives.
Strategic Program Directors are responsible for a number of these areas and function at a high level. Direction and coordina

tion of the group of activities is not an operational necessity. Change: Eliminate position.

Finally, the contract with a professional marketing and communications company to provide marketing, public relations and communications services, under the leadership of the Strategic Program Director, Marketing, provides an important function in the Society. As a result, the following change is proposed:
Director, Technical Marketing: "shall contribute to areas of technical marketing development pertaining to CPMT Membership, Conferences and Publications…"

This position has not been active for over eight years. Its functions can be handled best by marketing professionals, under the guidance of Society volunteers. This model is currently in place through the Strategic Program Director, Marketing working with a professional marketing and communications company. Change: Eliminate position.

The Strategic Director positions and the Society Executive Office will be documented in the Bylaws.

Amendment 2 - Election of Board of Governors Members-at-Large (Amendment to Bylaws only)

Background:

To further the CPMT Society's globalization efforts, it is proposed that changes be made to the Board of Governors to ensure that it truly reflects and represents the Society's global membership.

Governance is an important and highly visible indicator of the nature of the organization. Although progress has been made in this area - there are more Members-at-Large (5) from outside the US now than in past years and, for the first time, two Officers from outside the US - the perception of the Society by those outside the US continues to be that it is a US organization with a global membership.

Proportional representation for Member-at-Large positions based on IEEE Regional location of Society members will be implemented according to the following procedures:

1. Determining Proportions

Annually, in spring, using IEEE Region definitions, and Society membership statistics as of 31 December of the preceding year, an analysis will be made of the proportion of Society members in each of the following Regions/grouping of Regions:

1-6 (US)
7 (Canada)
8 (Europe, Africa, Middle East)
9 (Central and South America)
10 (Asia, Pacific)

Any Region/grouping of Regions determined to have at least 10% of CPMT members will have the proportional number of Member-at-Large positions designated to it for representation on the Board

2. Constructing Slate of Candidates:

The slate of candidates for each year's election will be constructed to ensure that the resulting total of newly elected Members-at-Large plus continuing Members-at-Large has the proper proportion of representatives from each Region/grouping of Regions.

Candidates to represent each Regions/grouping of Regions will be selected from among members of the respective Regions/grouping of Regions, by a process to be defined by the Nominating Committee in consultation with the Society President. The process will ensure that input is provided by Society volunteers in the respective Regions/grouping of Regions.

3. Voting Procedures:

Society members in each Region/grouping of Regions with designated positions will vote for their Region/grouping of Regions' respective positions only. That is, members in Region 8 will vote for Members-at-Large for Region 8 only.
Society members in Regions without designated positions will vote with the Region/grouping of Regions with the majority of members.

CPMT Society Seeking Newsletter Editor

The IEEE CPMT Society is seeking candidates for the volunteer position of **Editor for its NEWSLETTER** for a term beginning toward the end of 2005. Self-nominations or recommendations of appropriate candidates should be sent in confidence by May 15, 2005 to Paul Wesling, VP-Publications for the CPMT Society, at: p.wesling@ieee.org (phone: +1-408-331-0114; FAX: +1-408-904-6997). Please include a curriculum vitae for the candidate if available.

Candidates should review the PDF and HTML versions of the NEWSLETTER at these locations:

www.cpmt.org/nsltr/
www.cpmt.org/announcements/nsltr0412a.html

CPMT NEWSLETTER:

The goal of the NEWSLETTER is to provide timely information (in combination with our Web site) to our technical community worldwide. It is published in paper form quarterly (March, June, September, December) and mailed to all members of the Society. It is distilled into PDF format and posted on the website. An HTML version is also posted on the website.
The NEWSLETTER prints news from the Society, plus information about upcoming events (Calls for Papers, Announcements). It also allows for paid advertising.

The e-NEWSLETTER is circulated by e-Notice to all members once or twice a quarter, supplementing the printed version. The editor has the option of assuming the tasks associated with the e- NEWSLETTER, but this is not required.

Duties:

The volunteer job of the editor includes:

· Determine editorial direction, based on consultation with the VP-Publications
· When possible, attend Board of Governors meetings and other events of the Society
· Recruit authors for articles, reviews of workshops and conferences, book reviews, and regular columns, as appropriate
· Assemble a staff of volunteer assistant editors and reporters to cover areas of interest to CPMT members
· Identify sources of additional material that could be subject to commentary or discussion within the NEWSLETTER
· Conduct periodic surveys to determine whether the printed and electronic NEWSLETTER meet the goals and expectations of CPMT members
· Master a preferred set of composition tools (or our current ones) suitable for page layout and export in a format that can be printed by the IEEE Magazines/Newsletters staff
· Work with IEEE staff to facilitate printing and distribution

A small budget is available for purchase of tools, travel reimbursement, and ancillary services.

New Senior Members in Our Societv

Robert Brocato -- Albuquerque
Michael Burka -- Boston
Paul P. Conway -- Ireland
Aaron C. DerMarderosian -- Boston
Joseph C. Fjelstad -- Santa Clara Valley
Tzyy-Sheng Horng -- Tainan
Telesphor Kamgaing -- Phoenix
Kwang-Lung Lin -- Tainan
Yong Liu -- Maine
Elizabeth A. Logan -- Santa Clara Valley
Yuancheng C. Pan -- Oregon
David V. Plant -- Montreal
Kevin Skadron -- Central Virginia
Ganesh Subbarayan -- Central Indiana

"… a candidate shall be an engineer, scientist, educator, technical executive or originator in IEEE-designated fields. The candidate shall have been in professional practice for at least ten years and shall have shown significant performance over a period of at least five of those years."

Less than 10% of CPMT Society members have applied for the senior member status even though about 50% meet the requirements. See the following website for your path to this deserved honor.

http://www.ieee.org/organizations/rab/md/smprogram.html

New Web Content -- ONLY for CPMT Members!

Your membership in the IEEE and the CPMT Society just got more valuable!

Beginning January 10th, all CPMT members were enabled to use our Members-Only webspace to access full-text papers or presentations, in PDF format, from several recent conferences:
new! 9 talks from the Seminar on **Packaging of Biomedical Electronic Devices**, held in San Diego, CA USA in Jan 2005, and organized by the San Diego CPMT Chapter.
TITLES: - Introduction to Implantable Cardiac Devices - Medical Integrated Circuits - Medical Microelectronic Packaging - Introduction to Medical Materials - Medical Device Energy Sources: An Introduction - Medical Change Management - Reliability Test Levels and Methodologies - Medical Applications: Electronic Device Packaging
new! 6 talks from the Plenary Session on **High-Density Substrate Technology**, held at ECTC in Las Vegas, NV USA in June 2004, and organized by the TC on High Density Substrates and Boards
TITLES: - Dielectric Materials for High Density Interconnect Technology - IVH Multi-Layer Printed Circuit Board with Polyimide Films - Advanced Technology For High Density Substrates And Boards - High-Density and High-Frequency Silicon Substrate Technology for SiP - Technology for Embedded Passives and Actives in a Substrate - A Consideration for Total Mechanical Stress in Flip-Chip Packaging Utilizing Buildup Substrate Technology

The presentations from these Recent Chapter talks are now posted in the Members-Only area.
TITLES: - Long Term Trends in Packaging Technology: The International Packaging Roadmap Update - Stablcor: a technology that controls CTE - Thermally Conductive Printed Circuit Board Materials: The T-lam System - An Introduction to Thermal Clad Insulated Metal Substrates - The Nanotechnology Frontier: Applications of Nano to Materials and Packaging - OLED (Organic LED) Display Technology and Applications
**IEEE Photonic Devices & Systems Packaging (PhoPack) Symposium '03
**EuroSimE'03: 4th Int'l Conference on Thermal Simulation in Micro-Electronics and Micro-Systems (France)
**IEEE Photonics Materials Reliability (PhoMat) Symposium '03
**NEMI Tin Whisker Workshop, Las Vegas '04
These are papers and presentations that cannot be found on IEEE's XPLORE. For someone who is not a CPMT member, they can only be purchased on CD-ROM. If you have a need to learn the latest in any of the fields above, check out the Tables of Contents and read some of the fine papers presented there.

Accessing our Members-Only area is very simple:
Point your Browser to: www.cpmt.org/mem/
When you are asked, enter:
Username: xxxx
Password: xxxxxx

(all lower-case, notice to know what to put in for the xxxx's you must look at page 2 of the latest CPMT printed newsletter, a newsletter that is mailed only to members)***Basis for Judging***: Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society. ***Eligibility***: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2004.

Access to Recent Conference Papers

We have posted the Tables of Contents of two of our recent conferences (EPTC'04 and HDP'04) on the CPMT website, so any technologist can view the sessions (and the paper titles) that each conference contained. Included in each of these PDFs is an embedded link that will take you to the IEEE XPLORE/IEL location of all of the papers themselves. Our purpose is to encourage more access and usage of these great Conference papers, and to help our Members and other technologists keep up with new developments.

Here are the first two examples, ready for you to download:
-- **EPTC'04** TOC: 6th IEEE/CPMT Electronics Packaging Technology Conference, Singapore (Dec, 2004) www.cpmt.org/docs/0412-eptc04-toc.pdf (800kB PDF)
-- **HDP'04** TOC: 6th IEEE/CPMT Conference on High Density Microsystem Design and Packaging and Component Failure Analysis, Shanghai (June, 2004) www.cpmt.org/docs/0406-hdp04-toc.pdf (400kB PDF)

Pick out the papers of interest in your own work and see if they help you resolve problems our define new directions. You can read the Abstract and Keywords on XPLORE without logging in; to download a paper, you'd need a subscription (or you can purchase access at a nominal rate per paper). Most engineers these days work for companies, universities or institutions with access to the IEEE's IEL/XPLORE system; if you are in doubt, please contact your librarian.
If you find this useful, please let us know! Should we discover that this serves a need, I'll post additional Tables of Contents as conferences are completed.

--Paul Wesling, CPMT Webmaster and Vice President of **Publications**

Region 10 Chapter Activity Round up

Malaysia Chapter hosted EMAP 2004 conference as a jointly sponsored event with IMAPS-Malaysia Chapter and IEEE Malaysia section from 5th to 7th Dec 2004 at Penang, Malaysia. Chief Minister of Penang Dr. Koh Tsu Koon inaugurated the gala event. Keynote lectures were delivered by Prof Rao Tummala of Georgia Tech Atlanta, USA, Dr. William Chen of IEEE CPMT Strategic Director, Region 10, Prof Andrew A Tay of National University of Singapore, Mr. Mustafa of Intel USA, Dr Raj Master of AMD USA, Prof K N Bhat of IIT Madras, India. About 107 papers were presented at the conference, which was well attended by 145 delegates.

Singapore Chapter arranged the 3-day international event of 6th Electronics Packaging Technology Conference from 8th to 10th Dec 2004 and 264 participants from 22 countries attended the event.

In addition to the technical program, the event included full-day Short Term Courses as under:-

i. "Solder Alternatives: Isotropic Conductive Adhesives, Anisotropic Conductive Adhesives and Non-Conductive Adhesives" by Prof K. W. Paik, Korean Institute of Science and Technology, Korea.

ii. "Lead-Free Soldering: Metallurgical Fundamentals Soldering Applications and Challenges" by Dr. N. C. Lee, Indium Corporation, USA.

Dr. Pey Kin Leong has also reported the following talks as part of their chapter activities.

(a) "Silicon Technology Scaling and ESD Reliability" by Dr. Natarajan Mahadeva Iyer of IMEC, Belgium on 15th December

(b) "Ohm's law failure: New Insights into the charge transport in the multivally band of structure of Ga As" by Prof V. K. Arora on 5th January 2005.

(c) "Optically induced features in Polymer based Field Effect Transistors" by Prof K S Narayan, Jawaharlal Nehru, Centre for Advanced Scientific Research Jakkur, Bangalore,12th January

(d) "Sky is the Limit: Multi-layer Three-Dimensional Integration Achieved by Wafer Bonding" by Mr. Chuan Seng Tan, Massachusetts Institute of Technology on 27th January 2005.

Hongkong Chapter has reported the new Executive Committee for the two-year term from January 2005 to December 2006 as under:

· Chapter Chair - Dr. Ming Li
· Chapter Vice Chair - Siu Wing Or
· Chapter Secretary - Wai Miing Cheung
· Chapter Treasurer - Run Fu

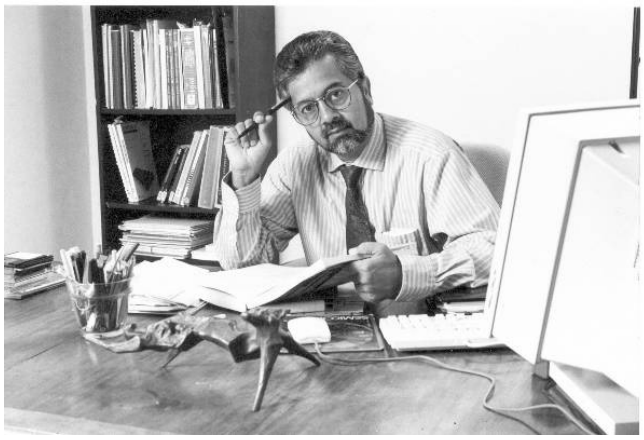
Dr. Ming Li has indicated their plans for a workshop in March, April 2005 and further short-term course on Packaging Technologies and Trends in Electronic Packaging for Global markets. The chapter would have active contacts with CPMT chapter in Mainland China and report their relevant technology level developments.

Dr. Lih- Shan Chen, Secretary of Taipei Chapter has reported the chapter executive committee for 2005 as under:

· Chapter Chair - Dr. Shen Li Fu
· Chapter Secretary - Dr. Lih -Shan Chen

Dr. Chen also reported having discussed the strategy for the development of membership of his chapter at the CPMT Luncheon meeting held during EPTC 2004 in Singapore on December 10, 2004.

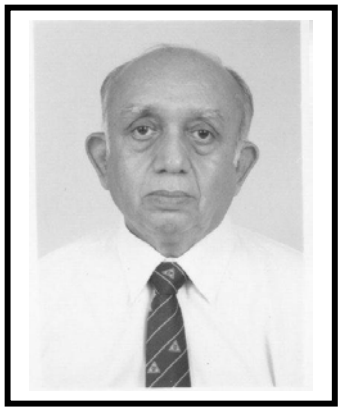
Dr. Shankara Prasad



The **India Council Chapte**r organized a cosponsored (with IEEE Eds Chapter and IEEE Bombay section) technical talk on 14th February 2005 by Prof Vikram L Dalal, Iowa State University USA who was invited as IEEE Eds Distinguished Lecturer. The topic of the talk was "The Photovoltaics Challenge: Role of Thin Film Silicon" and was well attended by about 10 IEEE members and about 40 students from IIT Powai.

As per the reorganization of the new chapter executive committee for the year 2005, Dr. Shankara Prasad of Inkroma E-Business Solutions, Bangalore stepped up to be the Chairman of the Chapter. Prof M. M. Shah has agreed to continue as Secretary/Treasurer of the Chapter and other Executive Committee members are Mr. I. M. Rao and Dr. Dhingra. Dr. Parikh would continue in the Executive Committee as Immediate Past Chairman.

Bangalore Chapter was inaugurated on 10th December in presence of Prof Madhavan Swaminathan of Georgia Tech, USA. The Chapter has organized a tutorial by Dr. P. R. Patel of INTEL on "Fundamentals of Packaging" bringing out the highlights of issues encountered in the recent past. The Bangalore chapter also organized an industry meeting where it was decided to organize an "Introductory Packaging Course" to be offered as a part of continuing education program at the Indian Institute of Science, Bangalore. The chapter is working closely with Georgia Tech University to conduct EDAPS conference at Bangalore in Dec 2005.



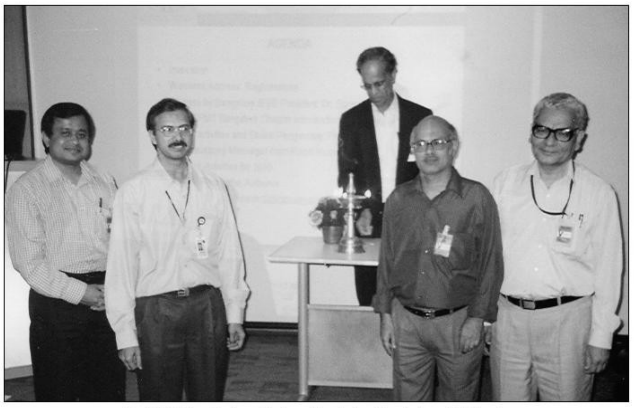
--submitted by ***Dr. P. B. Parikh***

Bangalore, India launches newest CPMT Chapter

(Compiled by CPMT chair: K Raghunathan)

India's newest CPMT chapter was launched in Bangalore on 10 December at the Texas Instruments India facility. Representatives from VLSI design, Package design, Board design, EDA, Test Services and Reliability analysis were in attendance to make it a successful beginning. Dr. Surendra Pal, President of the Bangalore IEEE presided over the function. Prof. Madhavan

Swaminathan, Deputy Director of Georgia Tech's Packaging Research Center (GT PRC) launched the chapter. K Raghu Raghunathan (Texas Instruments) and Suresh V Subramanyam (Intel) with support from the local Industry, GT PRC & India Institute of Science, Bangalore organized the chapter.



Symbolic lighting of the lamp at the inauguration – Raghunathan, Chairman CPMT Chapter
Foreground: Prof. Madhavan Swaminathan - GTPRC, P R Suresh – Chairman ED & SSC Chapter, Anand Mohan – Chairman CAS Chapter & Surendra Pal – President IEEE Bangalore Section

The main goal for the coming year will be to raise the awareness of packaging related issues. An ambitious program was outlined to educate through introductory course followed by advanced topics in the areas of Electrical, Thermo-mechanical, Manufacturing and Reliability. The chapter is also planning to hold regular meetings along with tutorials. The audience feedback was positive with pledge for active participation in the events. EDAPS conference was identified as another opportunity to interact with other experts. IEEE Bangalore (Surendra Pal), IEEE/CPMT Global (Ralph Russell) and GT PRC pledged to guide and support the chapter initiatives.

The CPMT chapter recognized the petitioners and also the efforts of Marsha Tickman, Executive Director, IEEE CPMT Society to expedite the approval process were appreciated. Following were chosen as the office bearers for 2005:

Chairman: K. Raghunathan (Texas Instruments)
Vice-Chairman: Suresh Subramanyam (Intel)
Secretary: M. Saketuraman (GE)
Treasurer: Manish Rawat (Wipro)

The newly appointed Chairman Raghunathan outlined the priorities. They are

o Plan to raise the membership to reach critical mass
o Raise awareness by means of tutorials, educational activities
o Join the Region 10 chapters and assist growth of the industry
o Looking for closer cooperation with other CPMT chapters
o Plan to organize a region wide conference in 2005
o Become a conduit for Indian industry to reach out to the global network

Dr. Surendra Pal provided an overview of the local IEEE chapters and extended his support in terms of getting experts for delivering lectures and also mentioned that he will support on fund needs for the CPMT chapter. P R Patel, from Intel, shared his thoughts that the CPMT chapter will serve as a platform to generate interest with the local industry and with knowledge sharing by experts from different domains happening as part of CPMT chapter lectures, it will help the businesses to integrate into the Semiconductor Packaging world.

Vice-Chairman Suresh Subramanyam in his vote of thanks requested the audience to make the best use of the local CPMT chapter and make it a successful one.

Singapore Hosts EPTC'04

6th Electronics Packaging Technology Conference (EPTC 2004), 8th - 10th December 2004, Pan Pacific Hotel, Singapore With the 6th conference in the series, the Electronics Packaging Technology Conference (EPTC) has truly achieved the status of a major packaging conference and is now the premier event for the Asian region. 264 participants from 22 countries attended the 3-day event. Besides participation by all the major electronics manufacturers and design houses in the island republic, there were strong contingents from USA, Malaysia, Taiwan, Germany and Japan. The delegates represent a total of 91 organizations, about two-thirds from the commercial sector and one-third comprising universities and research institutes.

Since its inception in 1997, the EPTC has grown to encompass almost all aspects associated with the packaging of high performance electronics. EPTC 2004 featured about 150 technical presentations dealing with advancements in core technologies such as interconnects, electrical and thermal design, materials and mechanical characterization, assembly and reliability methodologies; and technologies for state-of-the-art platforms such as 3D packaging and Systems-in-a-Package. In his welcome address, KC Toh, General Chair of EPTC 2004, said that the keen interest from participants was because a high proportion of the global packaging activities, in particular assembly, design and test, were now carried out in this region.

The conference was organized by the IEEE Reliability/CPMT/ED Singapore Chapter and was technically co-sponsored by the IEEE CPMT Society and IMAPS, with strong support from four patrons, Advanced Micro Devices (S) Pte Ltd, GE Silicones, Infineon Technologies Asia Pacific Pte Ltd and Micron Semiconductor Asia Pte Ltd. It was opened by Rolf Aschenbrenner, Vice-President (Technical), IEEE CPMT Society, who expressed the Society's commitment in making EPTC one of the major events in its calendar. The plenary session

featured two keynote speeches. **Carlo Cognetti,** Vice President for New Package Development at ST Microelectronics, spoke of the pace in "Package Level Integration: Much More Than Moore", while Dr **Bill Bottoms**, Chairman of Third Millenium Test Solutions, emphasized the need to tackle the "Test Challenges for Systems in a Package (SiP)". Two other invited speeches were delivered by Rolf Aschenbrenner, representing CPMT Society, and Dr Chuck Bauer of Tech Lead Corporation during the conference lunches.

The success of a conference is measured not only by its technical program but also a host of supporting activities. At EPTC 2004, participants had the opportunity to interact with 22

exhibitors who displayed their products and services during the conference. Two pre-conference short courses, conducted by Professor KW Paik of KAIST and Dr NC Lee of Indium Corporation, were also held to help industries prepare for lead-free implementation. Also, for the very first time, we had an Executive Forum session featuring three eminent speakers from the International Technology Roadmap for Semiconductors (ITRS). Dr Bill Bottoms, Dr William Chen and Dr T Fukushima, fresh from the ITRS meeting in Japan, updated the participants on "Packaging Technology Trends and Challenges" in the area of design, materials, assembly and test. As befitting our Asian origins, symbolized by the warmth and friendliness of its peoples, participants were also taken for a cable car ride around one of the busiest ports in the world, before enjoying a sumptuous banquet atop scenic Mount Faber, which provided opportunities for networking among the participants.

IPFA'05

The deadline for the submission of abstracts for the 2005 International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA'05), organized by the IEEE Rel/CPMT/ED Singapore Chapter, and technically co-sponsored by the IEEE EDS and Reliability Society is just over. Currently, the technical committee is busy reviewing abstracts submitted. For more information, please visit the IPFA'05 website at http://www.ewh.ieee.org/reg/10/ipfa/html/2005/.

A Region 10 Chapter meeting was held 10 Dec 2004, in conjunction with EPTC 2004. This luncheon meeting was organized by the CMPT BOG and sponsored by the Singapore Chapter. Besides the various Region 10 Chapter Chairs (Singapore, Beijing, Hong Kong, Malaysia, Korea and Taipei), CPMT BoG Delegates, Ricky Lee, William Chen, Marsha Tickman and Kristine Martin were present. The Singapore Chapter was represented by KL Pey, KC Toh, Charles Lee (also BoG member) and Andrew Tay. On behalf of the CPMT Society, Dr. William Chen, Strategic Director, Region 10, presented an award to Dr. Ong Soon Huat, and appreciation letters to the EPTC'03 and '04 key appointment holders. A CMPT banner was presented to the Singapore Chapter. In addition, Dr. Chen and Dr. Lee, VP for Conference outlined the strategy for the Region 10 activities and the forthcoming key conferences, respectively. In particular, EPTC has been identified as a strategic conference for IEEE CPMT Society in Asia. The participants at the meeting shared and exchanged views on improving and promoting CPMT activities.

By KL PEY, Chair, Singapore REL/CPMT/ED Chapter

Editor Note: Phoenix Workshop has new write up. Check out Newsletter website at URL listed at top of page 1 in this issue.

Packaging of Biomedical Electronic Devices

Review by Merrill Palmer

Saturday, January 22, 2005, IEEE CPMT San Diego Chapter conducted a full-day technical seminar on the subject "Packaging of Biomedical Electronic Devices". The seminar was organized by Merrill Palmer under the direction of Chapter President Steve Adamson. Forty-one persons attended.

Speakers included Dr. Darryl D'Lima, Scripps Clinic Center for Orthopaedic Research and Education; Dr. Christopher Druzgalski, California State University, Long Beach; Jim Steele, Mark Henschel, and Clive Groom, Medtronic; and Robert Czajkowski, NxGen.

Through the efforts of Paul Wesling, nine presentations from the seminar are available on the Members Only area of the CPMT web site, http://www.cpmt.org/mem/. San Diego Chapter recognizes and expresses appreciation for UCSD for facility use and to IEEE Regional Activities and CPMT Chapters Committee for financial support.

TC-1 News -- Holm Conference

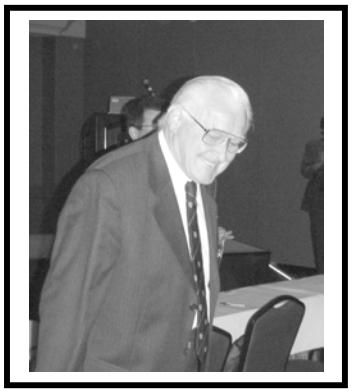
The scope of this Committee is to be the focal point within the IEEE CPMT Society for electrical contacts, electrical connectors, and interconnecting cable. Its membership consists of individuals having an interest in the research, development, manufacture, and utilization of electrical contacts and devices that contain them. The Committee holds regularly scheduled meetings and functions through the Holm Organization and through task forces having specific objectives. The Committee sponsors or supports conferences, publications, educational, standardization, and other activities.

Holm: The Joint 2004 IEEE 50th Holm Conference on Electrical Contacts and the 22nd International Conference on Electrical Contacts was held in Seattle, Washington on September 20 to 24. After 2 years on low attendance due to the slow economy, the 2004 conference was a great success with over 170 attendees from many countries.

The technical program was very successful with 79 papers in 16 sessions. This included 21 from North America, 37 from Europe and 21 from Asia. Papers were presented on electric contacts in switches, relays and connectors, new contact materials and coatings, arc fundamentals, thermal models, finite element analysis and corrosion. New technology areas on MEM and high frequency contacts were special topics organized by the TC1 subcommittees to focus the importance of contact physics. More details of the program and abstracts can be found in our web site.

The Ragnar Holm Scientific Achievement Award Lecture was done by **Professor Koichio Sawa** of Keio University, and the Morton Antler Lecture was done by Dr. Robert Mrockowski. Again their expertise in the electrical contacts area made the lectures most informative for everyone.

On Wednesday night, we also had a successful social event to the Kiana Lodge. This was a true Northwest experience with a cruise through Puget Sound to taste the world famous salmon fish and steamed clams, and more importantly, the opportunity to mingle among international friends and colleagues.



At the conference, a standing ovation was also given to Professor Werner Rieder for his being recognized by the Austrian government for his scientific contributions with a special Dr. Werner Rieder stamp. A real rare feat for any engineer.

TC1 also completed a DVD project with Dr. Thomas Schoepf as editor. The DVD contains all the technical papers of 50 Holm Conferences. This dates from 1953 to 2004. A must have information source for anyone in the field of electrical contacts.

The 2005 IEEE Holm Conference will be back to Chicago on September 26-28. The International Committee also announced that the 23rd ICEC will be on 6-9 June 2006 in the beautiful city of Sendai, Japan.

For more information on many special events organized by this committee such as annual IEEE Holm conference, intensive course, international conference, DVD library and link to other societies, please visit our web site at www.ewh.ieee.org/soc/cpmt/tc1.

2003 Prize Paper Award Michael Little and Xin Zhou

TC-MEMS and TC-WLP at ECTC

With the joint technological aspects these topics share, it was conceived that the exchange during the TC meetings should try to bring up synergies. Therefore both TC´s will share their meeting in a joint "round table".

To ensure a broad basis for this exchange, simultaneously with ECTC (Orlando, FL,USA) and DTIP (Montreux, CH), such joint TC meetings will be held.

Details will be posted via the respective mailing lists and will be made visible during the conference events´ black boards.

-- submitted by TC Chairs Erik Jung and Michael Toepper

Advanced Flexible Circuit Board Technologies

Thursday, June 2, 2005 - 7:30 PM - 10:00 PM

Chair: Yoshitaka Fukuoka - Weisti

Co-Chair: Kishio Yokouchi - Fujitsu Laboratories Ltd.

A dramatic improvement in performance has been achieved in recent mobile electronic products, such as cellular phones, digital camcorders, digital still cameras, personal digital assistant, note PC and so on. Additional improvement would require a higher density and layer count flexible printed circuit board and rigid/flex circuits board technologies. Especially in Japan, those technologies are developing remarkably. This session focuses on the latest technical information of advanced flexible, rigid/flexible circuit board technologies, advanced processes and advanced materials, and their characteristics estimation results.

1. Technical Trends of Advanced Two-Layer Flexible Copper Clad Laminate, Masahiko Takeuchi - Nippon Steel Chemical
2. Ultra Thin Flexible Circuit Board Used Photo-Sensitive Polyimide and Semi-Additive Process
   Yasuhito Oowaki - Nitto Denko Corporation
3. Advanced Rigid-Flexible Circuit Board Technologies
   Yoshihisa Katoh - CMK Corporation
4. All Layer IVH Substrate Made From the Polyimide Film
   Masaaki Katsumata, Hitoshi Nakamura and Fumio Echigo - Matsushita Electronic Components Co., Ltd.
5. Electrical Characterization of Thin-Film Embedded Passives
   Koichiro Nakase, Daisuke Ohshima, and Hirobumi Inoue - NEC Corporation

This session is open to all conference and exhibit attendees.

Get Class at ECTC Orlando

An all-day educational seminar will be offered on Tuesday, May 31, 2005 consisting of 16 Professional Development Courses. Mr. Rao Bonda and the Professional Development Course committee have brought together industry experts from a wide variety of disciplines to offer state-of-the-art technology reviews and updates in condensed half-day and full-day formats.

<u>Course topics cover a wide range of technologies:</u>

Nanoscale Packaging and Systems--Zhong Wang, Georgia Tech
3D Integration Technologies - Rajen Chanchani, Sandia Labs
Trends in Advanced Packaging - E. Jan Vardaman, TechSearch
Moisture Related Reliability in Electronic Packaging - Xuejun Fan, Intel
Lead-Free Soldering - Ning-Cheng Lee, Indium Corp.
Embedded Passive Technology -- Richard Ulrich, U. Arkansas
Stacked SIP Production--Larry Gilg, Die Products Consortium
Sim and Modeling of HF PCB and Pkg --O. Ramahl, Xin Wu
Integration & Packaging for Wi-Fi -- M. Swaminathan, GT
Lead Free Solders - John Lau, Agilent Technologies
Microelectronic and MEMS Sensors - G. Harsanyi & Z Vitez
Package Failure Analysis - D. Goyal & R. Dias, Intel
Polymers for Electronic Packaging, C. P. Wong, Georgia Tech
Virtual Thermo Prototyping - G. Q. Zhang, Philips
Wafer-Level Chip-Scale Packaging - Luu Nguyen, National

These courses are eligible for Continuing Education Unit (CEU) credits.

PRINTED CIRCUIT BOARD INNOVATOR RECEIVES CPMT-IEEE AWARD

The IEEE has named Yutaka Tsukada, managing director of the Advanced Packaging Laboratory at Kyocera SLC Technologies Corporation in Shiga-Kan, Japan, and formerly with IBM Japan, as recipient of the 2005 IEEE Components, Packaging and Manufacturing Technology Award.

The award honors Tsukada for pioneering contributions in micro-via technology for printed circuit boards and for extending the feasibility of the direct flip-chip attachment process.

In the PCB industry, he is regarded as an innovator in the area of high-performance, economical, compact and lightweight PCB packaging. Technologies developed by Mr. Tsukada are used in most PCB applications, including cellular telephones, portable and desktop PC processors, digital signal processors, digital cameras and workstation components.

He pioneered the development of build-up PCB micro-vias and developed a solution for underfill, reinforced flip-chip bonding. The build-up PCB radically changed the structure of PCBs, allowing a single, build-up layer with micro-vias and fine-line wiring to replace, at a lower cost, as many as four layers of conventional PCB wiring. These advances allow wiring and chips to be attached directly by flip-flop bonding, yet still accommodate the wiring required for signal-line fan-out and power connections.

Leading companies such as IBM, Intel, AMD, Motorola and Texas Instruments, have adopted Mr. Tsukada's innovations in their core package design to gain denser and faster IC chips. He holds three Japanese and three U.S. patents for PCB packaging technology.

Sponsored by the IEEE Components, Packaging and Manufacturing Technology Society, the award recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. It will be presented at the 2005 IEEE 55th Electronic Components and Technology Conference in June in Lake Buena Vista, Fla.

Workshop Report

2005 IEEE European Systems Packaging Workshop

Conference Dates: January 31 -- February 2, 2005
Location: Park Inn Hotel - Alexanderplatz, Berlin Germany
General Chairs: Christine Kallmayer and Rolf Aschenbrenner

Keynote Speakers:

****Evan Davidson** presented in his talk, "The History of Electronic Packaging," an overview of the entire 100 years of packaging used at the board and component levels. He finished with an outlook for future technology directions.

****Werner Weber** (Infineon) discussed in "Ambient Intelligence - Industrial Research on a Visionary Concept" his vision of the "disappearing computer", a powerful concept of the computer absorbed/imbedded in every day apparatus/personal items. The consequence of this vision is the effort not only to miniaturize the electronics but also to make them self sufficient by including the power generation and rectification along with transmitters and RFIDs in the packages.

****Robert Guernsey** gave a very impressive outlook in his presentation, "Current View of Package Technology Opportunities in the 45 nm Silicon Generation," for the future technology trends including the key messages that passive power is approaching active power and cooling technology cannot support much more frequency scaling. As a consequence, we will see the end of frequency scaling resulting in an increase of integration on chip (multi-cores, multi-threading, multi-fabrics).

**** Herbert Reichl** from Fraunhofer IZM/Technical University of Berlin predicted in his talk "Hetero-system Integration Technologies: Challenges & Choices" system requirements for new applications with integrated electrical and non-electrical (sensor, actuator) functions. The hetero-system functionality can be considerably enlarged by the integration of mechanical, optical and/or biological functions. The applications that the EU is focusing on are: auto, mobile communication, life sciences, smart homes, wearables, RFID, and bio-interfaces.

Highlights of the Conference

In Session 1, challenging packaging technologies were described for smart cards, flex technologies, electronics in textiles and wireless temperature sensors. The requirements for micropower delivery were also discussed.

Michael Huber highlighted in his presentation that the development of new materials for flip-chip technology and that the optimization of the production process led to the use of these technologies for smart cards and RFIDs.

Jan Vanfletern discussed interesting trends for smart highly integrated flex technologies; including: resistors, capacitors, RF components and ultra-thin chips using a flex laminate technology.

Special packaging challenges were discussed and shown for special applications by Torsten Linz for integrated microelectronics in textiles.

Robby Rochlitzer presented an electronic system design for a wireless temperature sensor that works autonomously and is connected via an infrared sensor to a PC.

Cian Ó Mathúna introduced ambient systems in the context of a range of potential applications and associated micro-sensor module system architectures and power budgets.

In Session 2, Thomas Velten, Peter Laitenberger, Robert Dickinson and Graeme Maxwell focused on the special demands for biochip and biosensor packaging. This is a very special area for packaging technology challenges. Here, not only is the size extremely small and the need for low power electronics crucial but they also shared some of the requirements for high-end computing namely, reliability and hermeticity.

Session 3 focused on optical interconnect technology, including optical waveguides, ink-jet based optical element manufacturing techniques, optical-electrical comparison/crossover and optical chip assembly technologies.

Elmar Griese outlined in his presentation "Optical Interconnections on PCBs: Fundamentals - Technology - Design" the essential features of waveguide technology including various manufacturing methods (embossing, laser-write and photolithography).

Padraig Hughes included in his presentation many aspects of advanced packaging technologies.

Hermann Oppermans talk mostly focused on a AuSn bonding process for optical sub-assemblies or optical ICs.

Marc Taubenblatt's talk's focus was on high-end computing that typically requires thousands of off node/module interconnect channels and many Tbps of information flow.

In Session 4, high-end computer solutions were described for IBM, Fujitsu and Hitachi systems. Intel's presentation focused on power integrity in high-speed package design.

Hubert Harrer gave a very informative and complete presentation on the packaging technology and attributes of the IBM z-990 mainframe system.

Michael Fisher gave a comprehensive explanation of the requirements and packaging challenges and attributes associated with the IBM mid-range AIX/Linux p-Series Model 570 server.

Burkhard Steinmacher-Burow provided striking graphics and a description of the capability and structure of the IBM Blue Gene/ L Supercomputer and stressed the new paradigm that such an architecture creates.

Haruhiko Yamamoto-san (Fujitsu) presented the system configuration, packaging, and cooling aspects for high-performance server computers using the PRIMEPOWER HPC2500 as an example of a high-end Unix server series.

William Samaras from Intel discussed power integrity in high-speed package design for top-of-the-line microprocessors.

Hiroshi Go-san (Hitachi) presented the model J1 of their SR11000 supercomputer system. He provided a lot of interesting technical system information.

In Session 5, various systems-in-a-package were described showing different product driven packaging solutions.

Klaus Pressel (Infineon) talked about "Experiences & Trends for System-in-a-Package" and kicked off a discussion on silicon carriers.

Erik Jung (IZM) introduced "Hetero-System-Integration" using wafer level assembly for systems-in-a-package realizations.

Charlotte Gillot of IMEC presented "Wafer Level Encapsulation for RF MEMs" in hermetically sealed cavities using only standard IC manufacturing technologies at the wafer level.

Chul Soon Park (Korean Information & Technology Univ.) focused his presentation on the packaging solution for a compact and low cost radio system in

"A System-in-a-Package Integration of a 60 GHz Radio Transmitter For Next Generation WLAN Applications." .

Marc de Samber (Philips) introduced in his presentation "Technology Development for SiP" a silicon based technology and a metal-flex based technology that can be used for more complicated SiP applications.

"Team Building" Sessions

One of the highlights of the workshop was a three-hour tour of the sights of East and West Berlin. We had an informative guide who explained the history of the city as she pointed out the different points-of-interest. Stops at the Brandenberg Gate, Checkpoint Charlie and Museum Island gave us all a chance to interact and ask questions.

At the conclusion of the workshop, most of the attendees went on a field trip to the modern facilities at Fraunhofer IZM to learn more about their plethora of advanced projects. It was a very informative experience and we all are most grateful to IZM for organizing the workshop and for being such gracious hosts.

-- submitted by Thomas Winkel and Evan Davidson.

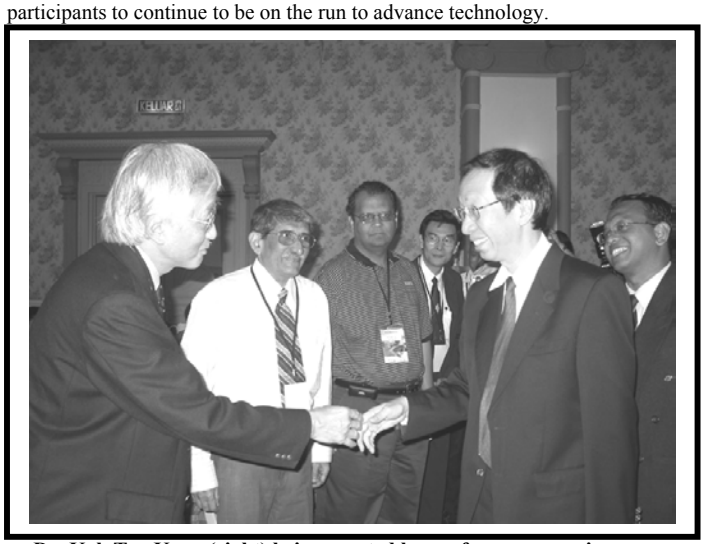
EMAP 2004 Enjoys Success in the Pearl of the Orient

Almost 150 participants enjoyed 16 sessions of well researched papers at the 6th Electronic Materials and Packaging Conference (EMAP) in Penang, Malaysia - known as the "Pearl of the Orient." Hosted by the School of Mechanical Engineering, Universiti Sains Malaysia and jointly organized by Universiti Sains Malaysia, the IEEE Components, Packaging and Manufacturing Technology Society (CPMT) and IMAPS, more than 33 presenters from 12 different countries presented 103 papers during the two-day conference, according to Conference Chair Dr. Azidi Ripin.

The conference specifically targeted the research and development work in electronic materials packaging, two important facets of any chip development on top of the integrated circuit (IC) design itself. China, Hong Kong, Korea Singapore, Japan, Taiwan, India, Austria, Germany, Sweden, Netherlands, the United Kingdom and the United States all contributed to the program and Technical Program Co-chairs K.N. Seetharamu and Tech Joo Goh thanked the various electronic industries within Penang and around the world for supporting the conference.

The Chief Minister of Penang, Tan Sri Dr. Koh Tsu Koon, inaugurated the event and praised the conference organizers and attendees for hosting this very timely and relevant meeting in Penang.

"This is not an evolution, but a series of revolutions," said Koon, advising the participants to continue to be on the run to advance technology.



Dr. Koh Tsu Koon (right) being greeted by conference organizers.

World-class keynote speakers from around the globe included Dr. William Chen, IEEE Fellow, Strategic Director of Region 10, elected CPMT Society Board of Governor member and Senior Advisor, ASE (USA); Prof. Andrew Tay, Director of the Wafer Level Packaging Program for the National University of Singapore, Dr. Mostafa Aghazadeh, General Manager of Platforms Materials Enabling Department (PMED), Intel; and Prof. K.N. Bhat, Microelectronics Laboratory Indian Institute of Technology, Madras, India.

AMD's Dr. Raj Master (Senior AMD Fellow, C4 and Packaging) also delivered a keynote lecture on packaging challenges for microprocessors. Some of the challenges Dr. Master discussed included package choice, performance, cost and thermal issues. Just as the attendees worked to beat the heat on this South Asia Island, both researchers and industry experts alike discussed how to beat the heat in microelectronic products.

The attendees were also treated to a traditional Malaysian dinner during the EMAP banquet, sponsored by the CPMT Society. Traditional drummers entertained the guests, while Ricky Lee, Vice President of CPMT Society Conferences, and Professor, University of Science and Technology (Hong Kong) gave a quick presentation about the CPMT Society and thanked everyone for supporting this very successful conference.

Preliminary work on EMAP 2005 is already underway and is scheduled for December in Tokyo, Japan. EMAP continues to grow both in terms of numbers and paper submission quality, making this conference a key up-and-coming event for microelectronics professionals.

Jang-Kyo Kim (Hong Kong University of Science and Technology) and Mikio Horie (Tokyo Institute of Technology)

Conference Chair and Bill Chen show Malaysia CPMT Chapter banner

Upcoming Conferences

***6th Quality Electronic Design (ISQED), March 28 - 30, 2005, San Jose, California, www.isqed.org**

*** 16th Annual IEEEE?SEMI Advanced Semiconductor Manufacturing Conference (ASMC'05) Mucich, Germany (in conjunction with SEMICON Europa, 11-12 April 2005.**

Contact: Hartmut Grabinski, Laboratorium fur Information-stechnologie, Hannover, Germany - Ph +49-511-762-5030; Fax +49-511-762-5051; grabinski@lfi.uni-hannover.de

***Workshop on Signal Propagation on Interconnects (SPI'05), May 10-13, 2005 -- Garmisch-Partenkirchen, Germany**

***8th International Academic Conference on Electronics Packaging Education and Training, Vienna, Austria, May 18-19, 2005**

***28th International Spring Seminar on Electronics Technology (ISSE'05) Vienna, Austria, May 19-22, 2005.**

***EuroSime2005, April 17 - 20, Berlin Germany, www.eurosime.com**

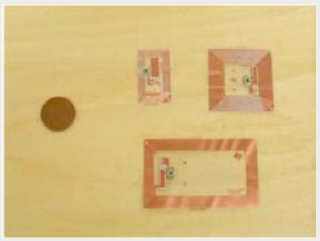
***55th Electronic Components and Technology Conference (ECTC'05), May 31 - June 3, 2005, Orlando, Florida -- Contact: Donna Noctor, noctor@ectc.net**

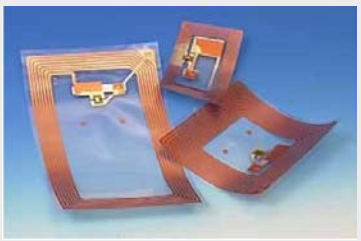
*** Symposium on Design, Test, Integration, and Packaging of MEMS/MOEMS (DTIP'05), Montreux, Switzerland, June 1-3, 2005**

***30th International Electronics Manufacturing Technology Symposium (IEMT'05), July 11 - 13, 2005, San Francisco, California -- Contact: Sheri Mukai, smukai@semi.org**

Santa Clara Valley Chapter,
Components, Packaging & Mfg Technology Society

Packaging and Manufacturing of RFID Technology





- **Wednesday, April 13, 2005**
- **Seminar: 1:00 – 5:30 PM**
- **Registration: begins at Noon**
- **Santa Clara Convention Center**
- **In conjunction with IEEE WESCON'05**
- **Includes free admission to WESCON exhibits**
- **Plenty of free parking**

With the advent of RFID chips in the commercial sphere, many companies and individuals are taking an interest in this emerging market. Major retail outlets as well as government uses of the devices are spurring a great deal of speculation about the future of the technology and creating demands for lower cost. Because of the small size and extreme cost constraints, packaging and test of these unique devices presents a challenge in terms of handling, yield and cost. This seminar will bring together leading experts in the field to discuss manufacturing, infrastructure, packaging and cost reduction efforts in the industry as well as an overview of RF packaging at Freescale Semiconductor.

The topics include:

- RFID technology and deployment
- Packaging technology and standards
- Frequency ranges and antenna packaging
- Manufacturing and cost considerations
- Training opportunities and sources of more information

PROGRAM

Introduction and Overview – Seminar Chairman

- Al Scott - Besser Associates "**Overview of RFID Technology and Deployment**"
- Raj Bridgelall - Alien Technology – "**Packaging Technology for UHF RFID Tags**"
- Jim Eagleson - Savi Technology – **International RFID Frequencies and Package Outline Standards"**
- Rod Petrianos - Escort Memory Systems – **"Packaging for RFID Antennas, Controllers, and Network Interface Modules"**
- Norm Owens - Freescale Semiconductor – **"RF/Microwave Packaging Technology at Freescale Semiconductor"**

REGISTER TODAY!

The seminar is filling up fast, so register early to ensure a seat for this interesting technical program.

REGISTRATION	By April 1	After April 1
IEEE MEMBER	$75.00	$95.00
NON-MEMBER	$110.00	$125.00
STUDENT (fulltime)	$30.00	$35.00
UNEMPLOYED*	$30.00	$35.00

*With proof of unemployment

Register through PayPal or get **registration form**:

www.cpmt.org/scv/courses/rfid.html

In conjunction with IEEE Wescon: **www.wescon.com**

Current Editor's Turn

I want to thank everyone who participated in identifying and nominating members of CPMT for the IEEE Fellow Award. The due date for all the write-ups was March 1. It was refreshing to receive spontaneous input from at least 30 members over the last year suggesting those that deserved to be nominated. It is worth noting (with only limited knowledge of those nominations that made it to IEEE by the deadline) that it appears that CPMT Society has nominees from Europe, Africa, South Asia, East Asia, and North America. It is also worth mentioning that there is quite a depth of volunteers that qualify for Fellow nomination and our Society appears to have provided opportunities to more this year than in the recent past. A thanks goes out to all the existing Fellows that took the time to review each nominee's credits and wrote reference letters. It is also worth noting that each year about 50% of potential nominees decide not to submit. This is to be expected with all the demands on the time of our active volunteers, however, we all hope that the invitation for nomination is seen as high recognition in itself. Each year about 0.1% of the full IEEE membership can be promoted to the Fellow ranks (about 250).

For this issue I would like to thank all the volunteers who forwarded their paragraphs and pictures. Particularly I would like to thank those that did the interim editing: Pey Kin Leong, Evan Davidson, Dr. P. B. Parikh, Marsha Tickman, Paul Wesling, Merrill Palmer, Vasu Atluri, Leung Chi, Phil Garrou, Donna Noctor, Alina Deutsch, K. Raghunathan, Geyun Zhang, Y. C. Mui, Robert Jackson, Reed Crouch, Ephraim Suhir.

VOLUNTEER ASSIGNMENT AVAILABLE:

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Editor for the IEEE *Transactions on Components and Packaging Technologies*

The CPMT Society of IEEE is seeking candidates for the volunteer position of Editor for its ***Transactions on Components and Packaging Technologies***. Self-nominations or recommendations of appropriate candidates should be sent in confidence to Paul Wesling, VP-Publications for the CPMT Society, at: **p.wesling@ieee.org (phone: +1-408-331-0114; FAX: +1-408-904-6997).** Please include a *curriculum vitae* for the candidate if available.

Start of Assignment: September 2005 **Length of Service: normally for 4 years, renewable**

Background:

The IEEE ***Transactions on Components and Packaging Technologies*** is the leading refereed journal in the field of electronics/photonics packaging, including materials, reliability, thermal analysis, mechanics, thermomechanics, high temperature effects, applied optics, power electronics, and measurement/characterization techniques. Original manuscripts describing the results of modeling and simulation, experimental characterization and validation, and/or packaging technology development efforts, as well as research and development efforts involving contacts science and technology**,** are welcome. The ***Transactions*** dates back to 1954, through various predecessors, and is available to CPMT subscribers in printed form; in an on-line version (IEEE XPLORE); and to corporate and university libraries (through the IEEE Electronic Library – IEL – and the all-Transactions packages). It is available by subscription to any IEEE member. For a listing of the topical areas addressed, please see our website: **www.cpmt.org/trans/trans-cpt.html**.

With a budget of 750 pages and some funding for administrative staff support, this ***Transactions*** selects about 150 papers each year for archival publication from those submitted directly or those recommended as "selected papers" from conferences. The Editor has a current working staff of 22 Associate Editors and 4 Guest Editors, each with a specialized technical area of expertise. The AE/GE selects from our 150 Reviewers (or nominates additional Reviewers) for the peer analysis. Suggestions for each submitted manuscript are returned to the author for revisions. For papers meeting our quality and novelty standards, the authors are invited to make revisions and submit them for final analysis and publication.

Manuscript-Flow Process:

The manuscript handling process is highly automated and has been designed to require only modest investment of time by the Editor. Authors use our Manuscript Central (MC) website for all submissions, and correspondence is automatically generated and archived as email. The MC system has high persistence, so the Editor can remain logged on indefinitely. Our IEEE staff screen each incoming manuscript to assure proper formatting (double-spaced PDF) before each is staged to the Editor's queue. Based on content, the Editor can assign it to an appropriate AE or move the manuscript to a different ***Transactions***. The MC system tracks the progress from AE to Reviewers and to completion of the AE Recommendation for each paper. The Editor then scans the reviews and recommendation and originates the Author Letter (a generated, customizable email). Author-revised files are submitted on-line, and the AE verifies that updates have been completed. Accepted papers are then queued for the next quarterly issue by the Editor. An "Editorial" is usually written by the Editor for each issue, giving high visibility and influence within the technical community.

The desired candidate will be comfortable with on-line systems and tools and will use university and industry relationships to add staff to the editorial team for topical areas, working with the Editor-in-Chief and the VP-Publications. Ability to work well with and encourage other busy volunteers throughout our profession is a plus. Past experience with an archival packaging journal is desirable.

Additional Details:

Please conduct your own review of our website for familiarity with our ***Transactions*** and its sister journals: **www.cpmt.org/trans/**. Review past Tables of Contents, and scan the Instructions to Authors or to Associate Editors. Then correspond with Paul Wesling at the phone/email above. You will be invited to discuss this assignment with one or more other Editors currently using the MC system.

Rev. C 2/21/05

Preliminary program and content of the
The 7th IEEE CPMT International Conference on High Density Microsystem Design and Packaging and Component Failure Analysis (HDP´05)

Date: June 27 – 30, 2004 Venue: Shanghai, China

Co-sponsored by: Shanghai Science and Technology Commission, Shanghai Government
IEEE CPMT Society, IEEE CPMT Scandinavian Chapter, IEEE CPMT China Chapter

Microsystem design, manufacturing, assembly and packaging technology is playing a key technology for the progress of the microsystems and microelectronics industry in the world. China is not an exception. Therefore, many multi-national companies are establishing new facilities in China for expanding their global business and interest. Following the successful previous conferences, we are proud to announce the sixth International IEEE CPMT Symposium on High Density Microsystem Design and Packaging and Component Failure Analysis in Electronics Manufacturing (HDP´05).

Documentation: The documentation from the conference will be published as an IEEE Conference proceedings with CD ROM

Journal publication: In addition, high quality papers will be selected to be published as special editions of the IEEE CPMT Transactions.

Preliminary key note and invited speaker lists are given below:

- Sergio Camerlo, engineering director, Cisco, USA
- William Chen, Senior advisor, ASE; USA: Semiconductor Packaging Roadmap, USA
- Paul Conway, Reader, Loughborough University, UK
- Jenq-Gong Duh, Professor, Tsinghua University, Taiwan: Intermetallic Compound Formation and Diffusion Path Evolution in the Flip Chip Sn - 37Pb Solder Bump after aging
- Andrew Tay, Professor, National University of Singapore, Singapore: Mechanics of Interfacial Delamination in IC Packages Undergoing Solder Reflow
- Quinones, Horatio, Manager process development, Asymtek, USA
- Itsuo Watanabe, Senior manager, Hitachi Chemcials, Tentative, Japan
- Lawrence Wu, Professor, City University of Hong Kong, Kong Kong
- Dr. Dongkai Shangguan, Flextronics, USA: Trend in Global Electronics Manufacturing
- Dr Wayne Koh, An overview of the latest technology market, and assembly of flash memory cards--3D stacking and SIP, Kingston, USA

The following is the preliminary paper list:

- Novel MMAP (Molded Matrix Array Package) Stacking Method By Laser Engraving Pattern and Metal Deposition, Qian Li, Intel, Shanghai, China
- Reliability Modeling for Stacked-CSP Components Thermal Cycling, Derek Zhou, Yi Xuan, BQ Wang, Intel Products (Shanghai) Co.Ltd, China
- 0.8mm Ball Pitch Accelerated Test Challenges in Micro-Electronic Packaging, Keh Shin Beh, Wei Keat Loh, Jenn Seong Leong & Wooi Aun Tan, Assembly Technology Development- Malaysia, Intel Technology (M) Sdn. Bhd.
- Quanta Low Resistance ICT Failure Issue Resolution, Sherry Pan, Intel, Shanghai, China
- High temp bake impact evaluation and it's solution study, Nicole Qian, Intel, Shanghai, China
- Eliminate Vcc/Vdd check process before SHBI through IDDQ mode, Joyce Liu, Intel, Shanghai, China
- Lot Level Sampling CPV Methodology, Yaoguang Cheng, Intel, Shanghai, China
- BIB First Articale Checkout with UBID and MPHS, Eric Huan, Intel, Shanghai, China
- Wafer Fabricated Thin film Strain Gauge, Zhao Jun, He Jun , Tan Ming Li, School of Mechanical & Power Engineering, Shanghai Jiaotong University, China, Hewlett Packard Pte Ltd, Singapore
- Shape Prediction of BGA (Ball Grid Array) Solder Joint and Its Reliability Optimization Design, Zhou Wenfan and Chunqing Wang, Harbin Institute of Technology, China
- A New Partitioning Scheme of Parallel VHDL Simulation, WU Yue, JIAN Ling, YANG, Hong-Bin and LIU Zong-Tian, School of Computer Engineering and Science, Shanghai University, Shanghai 200072, china
- An Improved IP Wrapper Design for SOC DFT, Ren Xiao-jun Zhang Jin-yi, The Micro-Electronics Research and Design Center of Shanghai University
- Elemental Redistribution and Diffusion Path Configuration near the edge of Sn-95Pb Solder Bump/Ni-Cu UBM Joints after Aging in the Flip-Chip Technology, S. Y. Tsai, C. L. Lee, G. J. Chiu and J. G. Duh, Department of Chemical Engineering, Minghsin University of Science and Technology, Hsin-Fong, Hsin-chu, Taiwan and Department of Material Science and Engineering, National Tsing-Hua University, Hsinchu 300, Taiwan
- Optimization of lead free solder paste for robust process and reliable solder joint, Anne-Marie Laügt , Avantec , France – J Klerk , P.C.J.Evers, Philips CFT, The Nederlands, D Caban Thomson Multimedia France, P. Wilczec, G Spilka AB Mikroelektroniks, Austria.
- High Density Data and Telecommunication Center Cooling Challenges and Solutions, David Wang, Teradata, A division of NCR, San Diego, California, USA
- Circuit Tracks on 3D Thermoplastic Surfaces, Teija Laine-Ma, Jani Kujansuu, Jarmo Määttänen, Tampere University of Technology, Pori, Finland
- Integrated Capacitors and Resistors on Liquid Crystal Polymer Substrate, Gang Zou, Hans Grönqvist, Johan LiuTest speed dependency of peel strength of ACF joints, Masahiro Inoue, Katsuaki Suganuma, The Institute of Scientific and Industrial Research, Osaka Univ., 8-1 Mihogaoka, Ibaraki, Osaka 567-0047, Japan
- Effect of curing condition on interconnect properties of isotropic conductive adhesive composing of an epoxy-based binder, Masahiro Inoue, Katsuaki Suganuma, The Institute of Scientific and Industrial Research, Osaka Univ. 8-1 Mihogaoka, Ibaraki, Osaka 567-0047, Japan

We still accept some late papers. If you wish to submit a paper, please contact Liqiang Cao at smit@mail.shu.edu.cn. or johan.liu@mc2.chalmers.se at SMIT Centre, Shanghai, China and Sweden.

Further information will be posted at the website at http://www.smit-shu.com/english/mainframeen.htm and look for HDP05.

Hotel Information: Most quality hotels such as Sheraton, SAS Radiosson Hotel, Holiday Inn, Regents etc. at reasonable rates ranging from RMB from 500 to 700 per night (70-100 USD). Please make your reservations directly with the hotel via Internet or other means. Alternatively, SMIT Center, Shanghai University can offer good hotel-like guest rooms within campus at RMB200 per night. If you are interested in this accommodation, please contact Liqiang Cao for details:

Liqiang Cao, SMIT Center, Shanghai University, China Phone: +86-21-56331599, mobile: +86-130421 80386,
Fax: +86-21-56332054 email: smit@mail.shu.edu.cn, website: www.smit-shu.com
Or Yang Liu, Göteborg, Sweden Tel : +46-70-5693821, Fax: +46-31-772 3622, email: yuw@student.chalmers.se, www.smitcenter.chalmers.se

First International Workshop on 3S Electronic Technologies

September 22 & 23, 2005

Global Learning & Conference Center at Technology Square

84 Fifth Street, Atlanta, GA, 30308 USA

Online registration & program updates:
http://www.prc.gatech.edu/3s

General Chair: Prof. Rao R Tummala

Program Coordinator: Boyd Wiedenman

boyd.wiedenman@ece.gatech.edu

CALL FOR ABSTRACTS

Due June 15, 2005

Send abstracts (300 words or less) to Program Coordinator Boyd Wiedenman at boyd.wiedenman@ece.gatech.edu

The SOP paradigm changes the current chip-centric SOC methodology to a cheaper, faster-to-market system-driven IC-package-system co-design flow. The advantages of the SOP paradigm over SOC appear overwhelming due to SOP's design simplicity, lower cost, higher system function integration and electrical performance, without the intellectual property issues that dominate SOC. The SOP is also different from, and offers advantages over, 3D and SIP. The 3D packaging is typically stacking of similar, or dissimilar, chips such as DRAMS. The SIP goes beyond to embed both actives and passives with different functions but the passives are discrete, thick and bulky components leading to sub-system modules. The SOP goes one step further in the ultimate 3D integration of components in thin film form at microscale, in the short term, and nanoscale in the long term leading to system boards.. The SOP focuses on integrating of both single function as well as heterogeneous system functions, optimizing ICs for transistors and package for integration of digital, RF, optical, sensor and others. It accomplishes this by both build-up SOP, similar to ICs and stacked SOP, similar to parallel board fabrication.

This workshop reviews the latest R & D and manufacturing status of each of these 3 "hottest" electronic technologies around the world. It will also attempt to compare and contrast SOC, 3D stacking, SIP, SOP and MCM.

Keynote Speakers

SOC - TBD

SOP - TBD

SIP - TBD

Sessions

Mixed Signal Design & Tools

Embedded Passives & Capacitor

Embedded Optical Integration & Modules

Embedded RF Integration & Modules

Multifunction Integration & Modules

Wafer Level Nano Interconnects & Assembly

Mixed Signal Test

Mixed Signal Reliability

Online registration & program updates:
http://www.prc.gatech.edu/3s

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

Announcement

Future Directions in IC and Package Design Workshop, FDIP'05

sponsored by:

IEEE Components, Packaging, and Manufacturing Technology Society

organized by:

CPMT Technical Committee on Electrical Design, Modeling, and Simulation (TC-EDMS)

October 23, 2005
Austin, Texas

The goal of this workshop is to provide a forum to address the future needs associated with the design of next generation ICs and packages. The Technical Program Committee will solicit invited presentations from experts in the university and industrial communities. The workshop will be held in conjunction with the **IEEE Topical Meeting on Electrical Performance of Electronic Packaging** in order to enhance this conference with presentations that give directions for future requirements and developments in the area of electrical analysis and design. The workshop will foster active participation and discussions from all the speakers and attendees during the meeting.

The following talks are planned:

- ***Designing Servers In a Commodity World – Carl Anderson, IBM Corporation***
- ***Signal Interconnect Trends and Challenges Inside the CEC – George Katopis, IBM Corporation***
- ***High Volume Signal and Power Integrity Design for ASICs – Brian Young, Texas Instruments***
- ***Electromagnetic Field Visualization System for IC/Package Design Based on Optical Techniques – Mizuki Iwanami, NEC Corporation***
- ***Harnessing the Power of Parallel Computation on the IBM BlueGene/L to Analyze Complex Digital and RF Systems – Raj Mittra, Pennsylvania State University***
- ***Computational Electromagnetics for Circuits Simulations – the Challenges – Weng Cho Chew, University of Illinois, Urbana-Champaign***

Workshop will be held at the Radisson Hotel & Suites Town Lake, 111 E. Cesar Chavez, Austin, Texas 78701 (512) 478-9611. They are holding a block of rooms at $109.00 plus tax. Reservations must be made by September 30, 2005 in order to guarantee this rate. Be sure to mention that you are attending the EPEP conference in order to secure this rate. For more information on the hotel go to http://www.radisson.com/austintx. Additional information can be obtained at www.epep.org. Workshop chairs are Alina Deutsch (deutsch@us.ibm.com) and Madhavan Swaminathan (madhavan.swaminathan@ece.gatech.edu)

11th International Workshops on THERMal INvestigations of ICs and Systems
Call for Papers

THERMINIC Workshops are a series of events to discuss the essential thermal questions of microelectronic microstructures and electronic parts in general. These questions are becoming more and more crucial with the increasing element density of circuits packaged together and with the move to nanotechnology. These trends are calling for thermal simulation, monitoring and cooling. Thermal management is expected to become an increasingly dominating factor of a system's cost. The growing power dissipated in a package, the mobile parts of microsystems raise new thermal problems to be solved in the near future necessitating the regular discussion of the experts in these fields. Finally, there is an increasing need for accurate assessment of the boundary conditions used in the analysis of electronic parts, which requires a concurrent solution of the thermal behaviour of the whole system.

This year THERMINIC will address in addition to the "traditional" thermal management problems, also stress and thermal-stress-related-reliability issues, both in micro- and opto-electronics fields. These issues, including various nanotechnology applications, are of significant importance and of high interest to the engineering community engaged in the field of thermal phenomens in "high-tech" systems.

The Workshop is sponsored by the IEEE Components, Packaging, and Manufacturing Technology Society, the IEEE Computer Society, Test Technology Technical Council and TIMA Laboratory in cooperation with the Thermal Committee of IEEE CMPT

AREAS OF INTEREST include, but are not limited to, the following topics:

- Thermal and Temperature Sensors
- Thermal Simulation
- Electro-thermal Simulation
- Thermal Modelling and Investigation of Packages
- Reliability Issues
- High Temperature Electronics
- Heat Transfer Education
- Flow Visualisation Techniques
- Turbulence Modelling in Complex Geometrics
- Defect and failure modelling
- Reliability evolution and prediction
- Multiphysics simulation
- Nanoengineering issues
- Education
- Measurement of Thermal Properties
- Acquisition and analysis of Thermal data
- Temperature Mapping
- Novel and Advanced Cooling Techniques
- Thermal Performance of Interconnects
- Heat Transfer Enhancement
- Validation of Thermal Software
- Coupled (Thermo-mechanical, Thermo-optical, etc.) Effects.
- Thermal Stress: Theory and Experiment
- Thermal Stress Failures: Prediction and Prevention
- Nanotechnology Applications

TECHNICAL PROGRAMME will include oral talks, poster presentations, a panel discussion, and invited talks given by prominent speakers.

AUTHORS ARE INVITED to submit electronic papers describing recent work. Panel proposals are also invited. Papers may be extended summaries (minimum 500 words) or full papers although preference will be given to full paper submissions. In either case, clearly describe the nature of the work, explain its significance, highlight novel features, and describe its current status. Submission will be electronically only. Only papers of PDF (.pdf), MS Word (.doc), RTF (.rtf) or PS (.ps) formats can be submitted. Compressed paper versions (.zip or .gz) are highly recommended. You are allowed to submit at most 2 formats of your paper. Detailed information about the submission process will be made available on the THERMINIC Web page: http://tima.imag.fr/conferences/therminic/

In case you experience any problems with the submission procedure, please contact the General Chair Bernard Courtois, TIMA Laboratory, Grenoble, France - E-mail: THERMINIC@imag.fr

Accepted contributions will be included in Workshop Proceedings.

Submission deadline:	30 April 2005
Notification of acceptance:	20 June 2005
Submission of manuscripts for distribution at the Workshop:	24 August 2005

VENDORS AND BOOK EXHIBITIONS are invited to offer products in the scope of the Workshop to exhibit. Editors are invited to exhibit books.

SPECIAL ISSUES AND SPECIAL SECTIONS of leading periodicals have been organised regarding the previous Workshops (Journal of Sensors and Actuators, Microelectronics Journal, IEEE Transactions on VLSI Systems, IEEE Transactions on Components and Packaging Technologies, Journal of Electronic Packaging). It is again expected to have special issues and special sections of leading periodicals as follow up of the Workshop 2005.

PROFESSIONAL DEVELOPMENT COURSE/TUTORIAL will be offered on 27 September, prior to the Workshop. Details will be published in the Programme booklet.

http://tima.imag.fr/conferences/therminic/

7th Electronics Packaging Technology Conference (EPTC 2005)

7- 9 December 2005, Singapore

Mark Your Calendar

Announcement and CALL FOR PAPERS

IEEE

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

IMAPS

About EPTC

The 7th Electronics Packaging Technology Conference (EPTC 2005) is an International event organized by the IEEE Rel/CPMT/ED Singapore Chapter, sponsored by IEEE CPMT Society with technical sponsorship from IMAPS.

EPTC 2005 will feature technical sessions, short courses and an exhibition. It aims to provide a good coverage of technological developments in all areas of electronic packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts in the field.

Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in Asia and is well attended by experts in all aspects related to packaging technology from all over the world.

Conference Topics

You are invited to submit an abstract presenting new developments in the following categories:

- **Emerging Packaging Technologies:** 3D integration, embedded passives & actives on substrates, high power, RF modules, SiP and other system integration technologies
- **Interconnection Technologies:** gold and copper wire bonding and flip chip (eutectic/lead-free solders) on standard and copper low k wafers, solder replacement flip chip (ICP, ACP, ACF, NCP), under bump metallurgy, microvia and build-up technologies, nano interconnects.
- **Manufacturing Technologies:** Process characterization, yield improvement, cost and cycle time reduction, environmental improvements, Statistical process control.
- **Materials & Processes:** Advancements in adhesives, encapsulants, underfills, solder alloys, halogen-free materials, dielectrics, ceramics, composites, thin film processes on laminates, nano-materials and processes for packaging.
- **MEMS Packaging:** Packaging solutions for Inertial MEMS - Pressure sensors, actuators, microrelays Bio-MEMS, RF MEMS – Resonators, Switches and Optical MEMS- Switches, Crossconnects.
- **Electrical Modeling & Signal Integrity:** Modeling simulation & measurement for coupling, reflection & switching noise, EMI/EMC analysis on package & subsystems, Time & frequency domain measurements for advanced modules.
- **Thermal Characterization & Cooling solutions**: Modeling & simulation methodology for thermal characterization of advanced packaging, modules & systems. Novel thermal management solutions. Enhanced air & liquid cooling techniques, Hot-spot management.
- **Mechanical Modeling & Structural Integrity**: Thermo mechanical stress analysis, moisture diffusion modeling in advanced modules, drop impact, vibration & shock test for modules & sub-systems.
- **Optoelectronics**: Passive components (waveguides, splitters etc), Photonic interconnects, Design, Modeling & Measurements for Gb/sec & Tb/secl modules, and Optical backplanes.
- **Quality & Reliability:** Component, board and system level reliability assessment, failure analysis, interfacial adhesion, accelerated testing and models, component and systems

Important Dates

15 June 2005	**Submission of abstract**
1 August 2005	**Notification of Acceptance**
16 September 2005	**Submission of manuscript**

Extended Abstract and Paper Submission

Extended abstracts are solicited to describe original and unpublished work. The abstract should be about 500 words and it must clearly state the purpose, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications and how the work enhances existing knowledge should be included in the abstract as well.

Authors must designate two appropriate categories for abstract review. All submissions must be in English and should be made via electronic mail to **abstract@eptc-ieee.net**. The preferred file format is **Adobe Acrobat® PDF** with only one single pdf file for each submission. Please limit the file size to a maximum of 2MB. Contact us to supply a MS Word abstract. See instructions at **www.eptc-ieee.net.**

The abstracts must be received by **15 June 2005**. Authors must include their affiliation, mailing address, telephone and fax numbers, and email address. Authors will be notified of paper acceptance with publication instructions by 29 July 2005. The final manuscript for publication in the conference proceedings is due by 16 September 2005.

Outstanding Technical Papers

The conference proceedings will be an official IEEE publication. Top quality papers will be submitted to IEEE/CPMT Transactions to be considered for publication. Author(s) of Outstanding Technical Paper(s) will receive an award at the next conference.

Short Courses

The conference program includes full-day short courses which will be conducted by leading experts in the field. Details will be updated in the conference website and available in subsequent mailings.

Exhibition

A tabletop exhibition featuring suppliers of materials, equipment, components, software and service providers of the microelectronics and electronic assembly industries will be held during the conference. To exhibit, please see information on the website.

Conference information & contacts: **Website: http://www.eptc-ieee.net**

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Polytronic 2005

5th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics

http://www.polytronic2005.org

Polytronic 2005, the 5th International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics, will be held on **October 23-26, 2005** in Wroclaw, Poland.

The conference provides a unique opportunity for the meeting of polymer developers with polymer users from the electronics industries. Research paper presentations will cover all aspects of adhesives and polymers in microelectronics and photonics, including new polymers, organic devices, polymers in packaging, and adhesive applications.

Polytronic 2005 will be the fifth in the Conference series, begun in 2001 as an amalgamation of the previously successful series of IEEE Conferences on adhesives and polymers: Polymeric Materials for Microelectronic & Photonic Applications (POLY), Adhesives in Electronics, and Polymeric Electronics Packaging (PEP).

The topics that will be covered include:

Materials: Thermosetting/thermoplastic systems; inorganic adhesives; composites; filler materials; isotropic conductive adhesives; anisotropic conductive adhesives; underfill compounds; pastes and films; heat seal connectors; thermally conductive adhesives; polymers with adapted refractive index; photosensitive polymers; high temperature materials; PCB materials, polymer thick and thin films, low and high dielectric materials.
Processing and Manufacturing: Advanced packaging; lamination; printing; dispensing; spraying; transfer techniques; underfilling; potting; adhesion improvement; curing; equipment; statistical process control; economic analyses.
Design and CAD: Design, modeling, simulation, CAD of compounds and processes; thermo-mechanical behavior.
Reliability and Testing: Degradation mechanisms; adhesion; hermeticity; accelerated testing; humidity and environmental sensitivities; non-destructive testing methods; stress behavior.
Functional Polymers for Microelectronics: Conductivity of polymers; electronic transport; self-assembly; photoactivity; polymeric materials for molecular electronics.
Applications: Polymer electronic devices; polymer optical fibers; polymer wave guides; organic displays; polymer batteries; e-paper; flexible electronics.
Environmental Issues: Ecology and toxicology; life cycle analyses.

Submission of abstracts (31 May 2005)

Abstract should include the following:

- **ABSTRACT TITLE**
- **AUTHOR LISTING** (principal author first): First (given) name, Last (family) name, and affiliations, mailing address, telephone, fax and e-mail address.
- **PRESENTATION:** Indicate which Session Topic your paper matches and whether you prefer to do an Oral Presentation or a Poster Presentation. Placement is at the Chair's discretion.
- **ABSTRACT TEXT:** Not less than 250 words; preferably 1500 words.
- **KEY WORDS** List a maximum of five key words.
- **BRIEF BIOGRAPHY** (of principal author) Approximately 50 words.

Note: Electronic submission only. Submit abstracts to: papers@polytronic2005.org. Detailed information about the submission process for final papers will be posted later on the official conference web site (http://www.polytronic2005.org).

- **Notification of acceptance: 15 June 2005**
- **Final papers due: 05 September 2005**

ISEPT - China

CALL FOR PAPERS

Sixth International Symposium on

Aug. 30 - Sept. 2, 2005

Electronics Packaging Technology

Shenzhen, China

Who Should Attend: Attendees of this conference in the past have been researchers, developers, producers and users of packaging technology for IC, MEMS, optoelectronics, LEDs, LCDs, magnetic heads, sensors and PC Boards and assembly. There were over 400 attendees at the past five ISEPT conferences in China.

Conference Chair: Keyun Bi, China Electronic Technology Corporation, China

Co-Chair: Rao R. Tummala, Georgia Institute of Technology, U.S.A.

General Secretary: Xiang Wu, China Electronic Technology Corporation, China

Organizing Committee

Chunqing Wang, Harbin Institute - wangcq@hit.edu.cn
Fuhan Liu, U.S.A. - fliu@ece.gatech.edu
Y. C. Chan, Hong Kong
K. N. Chiang, National Tsing Hua Univ., Taiwan
Sei Ichi Denda, JIEP, Japan
Willian T. Chen, ASE, U.S.A.
Shenli Fu, I-SHOU Univ., Taiwan
S. T. Gao, Heibei Inst. Semiconductor
Ken Gilleo, Cookson, U.S.A.
Yifan Guo, Conexant Systems, U.S.A.
Peter Ku, Chipmos, Taiwan
John H. Lau, Agilent, U.S.A.
Dale Lee, Valor, U.S.A.
Ning-Cheng.Lee, Indium, U.S.A.
Ricky Lee, H.K.S & T Univ., Hong Kong
M. Y. Li, China
T. B. Lim, IME, Singapore
Charles Lin, Bridge Semiconductor, Taiwan
C. Y. Lu, Ardentec, Taiwan
James E. Morris, PSU, U.S.A.
Michael O'Donoghue, IMAPS, U.S.A.
Kyung W. Paik, KAIST, Korea
Bruce Romenesko, JH Univ., U.S.A.
Sarah Shen, Kingston, U.S.A.
Tadatomo Suga, Tokyo Univ., Japan
K. Suganuma, JIEP, Japan
S. Wakabayashi, Shinko, Japan
C. Q. Wang, China
Richard Wang, Amertron, U.S.A.
C. P. Wong, U.S.A.
Feijian Wu, Chipbond, Taiwan
Jianhua Wu, Anadigics, U.S.A.
Y. P. Wu, China
C. P. Yeh, Innosis, Taiwan
Phil Zarrow, ITM, U.S.A.

Abstracts due May 25, 2005: If you are interested in presenting a paper at this conference, please send an abstract (500-1000 words) via email to wangcq@hit.edu.cn. Please include your affiliation, email address, postal code, mailing address, and phone number in your submission.

System Packaging
SIP, SOP, 3D

Electrical & Mechanical Design
BGA, CSP, MCM, flip chip, 3D package, WLP, SIP

Materials & Processes
Underfill, thin films, coatings, substrates

Reliability
Modeling and testing analysis

MEMS, LED & Optoelectronics Packaging
Materials, processes, applications

High Density Substrates & Dielectrics
Advanced technologies & materials, processing

Surface Mount Technology
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For more information, please email Prof. Rao Tummala, rao.tummala@ee.gatech.edu

Publication Date
June 2006

13 Chapters
Over 450 pages

Publisher
McGraw-Hill, NY

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14th Topical Meeting on
Electrical Performance of Electronic Packaging

IEEE COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY SOCIETY

EPEP 2005

October 24-26, 2005
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Call for Papers

The **general subject of the meeting** is the electrical modeling, design, analysis, and characterization of electronic interconnections and packaging structures. Authors are invited to submit papers describing new technical contributions in the areas broadly covered below:

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- Advances in modeling core switching noise, and design of novel solutions
- On-chip measurement techniques
- Package analysis, including numerical methods
- Electromagnetic analysis tools
- Advances in transmission-line techniques
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- Prediction/measurement of radiation from on-chip sources, interconnect structures and packages
- Electrical design implications for low cost, high volume packaging
- Packaging concerns for wireless communication: design and modeling
- Packaging solutions for one chip radios: design and modeling
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Conference Co-chairs: Robert W. Jackson, University of Massachusetts; Moises Cases, IBM

Conference Web Page: Detailed information can be found at **www.epep.org**

Paper Submission: Information for authors can be found on the conference web page. Electronic submissions of no more than four pages must be received no later than **July 9, 2005.**

Student Paper Award: Two awards will be presented to the best two papers submitted by students

Short Courses/Workshops: On Sunday, October 23, 2005, a workshop entitled "**Future Directions in Packaging**" will be presented and short courses/tutorials will be offered.

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9th IEEE WORKSHOP ON

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and by the IEEE Components, Packaging, and Manufacturing Technology (CPMT) Society

May 10-13, 2005
"Dorint Sporthotel", Garmisch-Partenkirchen, Germany

During the last eight years, the IEEE Workshop on Signal Propagation on Interconnects has developed into a forum of exchange on the latest research results in this area. The aim of this ensuing workshop is to report on the most recent developments in the field of interconnect modeling, simulation and measurement on chips, boards, and packages. The event is also meant to bring together developers and researchers from industry and academia in order to encourage cooperation. In view of the last years' success, the committee is looking forward to the 9th IEEE Workshop on Signal Propagation on Interconnects where world class developers and researchers will share and discuss leading edge results in Garmisch-Partenkirchen, Germany. The workshop will be held in English. Detailed information about the workshop and its location are available on the website **http://www.spi.uni-hannover.de**. The committee is looking forward to your participation.

As already in the last years, the Committee intends to publish a CPMT special issue comprising selected papers from the SPI 2005 edition.

Main topics of the workshop will include, but are not limited to:

- Frequency Domain Measurement Techniques
- Time Domain Measurement Techniques
- Modeling of Package & On-Chip Interconnects
- Macro-Modeling
- Simulation of Interconnect Structures
- Electromagnetic Field Theory
- Analysis and Modeling of Power Distribution Networks
- Propagation Characteristics on Transmission Lines
- Coupling Effects on Interconnects
- Substrate Effects
- Guided Waves on Interconnects
- Radiation & Interference
- Electromagnetic Compatibility
- Power/Ground-Noise
- Testing & Interconnects
- Optical Interconnects

Submission of abstracts:
Those who wish to contribute to the workshop should send (by e-mail only) a formatted paper of up to four pages to the Program Chair **by January 31, 2005** (please see the submission instructions on our website **http://www.spi.uni-hannover.de** and use the author's kit provided there to ensure a consistent layout). If the paper is accepted, it will be reproduced, as is, in the workshop proceedings. Notification about acceptance will be given by March 14, 2005.

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