## Components, Packaging,



## and Manufacturing **Technology Society**







The Global Society for Microelectronics Systems Packaging

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### President's Column.....



Dr. William T. Chen IEEE Fellow President, IEEE CPMT Society Santa Clara, CA, USA wt-chen@ieee.org

Greetings!!!

### What is in a Name?

In one of my earlier messages to you I mentioned that the name "Packaging Engineer" or "Packaging Scientist" is not always understood outside of our industry. In the semiconductor industry, we are sometimes known as the "backend" signifying that packaging and test are at the backend of semiconductor (IC) manufacturing. Perhaps we can call ourselves "Backend Engineers", or tell our in-laws that we do "backend engineering". We may tell people that we work in the field of CPMT. Somehow it carries an aura of intellectual mystery that the mundane word "packaging" could never match. Try this acronym sometime with your friends. You may gain some new respect.

CPMT is one of the 39 Technical Societies of IEEE, and in "IEEE" we have a name that is widely recognized and respected worldwide. It is up to us to make IEEE/CPMT a readily recognized name in the world.

### **IEEE/CPMT Community**

In CPMT we are a profession of diverse academic disciplines, multiple global industries, and our business spans from major multinational companies to small entrepreneur start-ups. We are a truly multidisciplinary professional society. In our ranks are: electrical engineers, mechanical engineers, manufacturing engineers, chemical engineers, materials scientists and engineers, physicists, chemists, mathematicians and statisticians. While in each discipline we have our own vocabulary and acronyms, scientific values, and way of looking at problems, we do communicate around the same set of professional interests, and share in the same passion for technology and science advancement. We work at the interface of these disciplines. Learning to collaborate with each other greatly adds to the richness, color, and dynamism in our work. Within our membership ranks are some of the best minds in science and technology.

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### **IEEE CPMT Society Board of Governors** (June 3<sup>rd</sup>, 2006) Meeting Summary

Submitted by Marsha Tickman Executive Director, IEEE CPMT Society

The IEEE CPMT Society Board of Governors Meeting was held on Saturday, June 3<sup>rd</sup>, 2006, following the ECTC 2006 conference in San Diego, California. The following paragraphs summarize the highlights of the meeting.

Society President Dr. William Chen called the meeting to order at 8:30 a.m. It was confirmed that a quorum was present. President Chen introduced IEEE Division II Director, Bob Lorenz.

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### **IEEE-CPMT Society Awards for Year 2007** (Nomination Due Date: January 31, 2007)

Submitted by Dr. Kitty Pearsall **CPMT Society Strategic Awards Director** 

The CPMT Strategic Awards Director announces the call for nominations for our five, 2007 Society awards. The CPMT Society offers these awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and CPMT Society.

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#### 2007:

Eric O. Beyne, Steve J. Bezuk, N. Rao Bonda, Rajen Chanchani, Kitty Pearsall, and C.P. Wong

#### 2006:

E. Suhir, T.G. Reynolds, III, P.C H. Chan, J. Liu, W. D. Brown, C. Lee

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2006 / 2007 Deadlines for Submitting Articles:

November 25<sup>th</sup>, 2006 February 25<sup>th</sup>, 2007 May 25<sup>th</sup>, 2007

Members-only Web (www.cpmt.org/mem/)

**UserName:** 

Password: (Join CPMT for access)

### President's Column (Continued from Page 1)

CPMT members come from commercial companies, universities, government laboratories, and research institutes. Many of our members work in electronic products and semiconductor (IC) manufacturing industries. Some work in communication, computer, automotive, aerospace, medical, entertainment, materials, equipment and many other industry sectors that do not bear the word "electronic" in their names, but have significant electronic content in their products, and depend critically on electronic packaging as the major differentiation on their function, form, cost and performance. We have a very strong contingent in academia and a sizeable number of student members ready to enter the profession.

The technology started in the United States with the invention of the transistor in 1947, and the invention of integrated circuits some years later. Jack Kilby was a CPMT member (and our only Nobel laureate). The industry has now become global, and our profession is also global. In the pages of this newsletter you will find reports of CPMT global activities in North America, Europe, and Asia. In the last three months I have attended several conferences and seminars in the US, Europe and Asia. I attended presentations at formal paper sessions and dialogued at off-line meetings. While there are indeed regional differences, the major sets of professional interests and technical challenges differ very little. We are indeed a global professional community – the *IEEE/CPMT Community*.

### **Networking the Global Community**

I made it a point to engage in discussion with people during the conferences in Europe (ESTC) and China (ICEPT & HDP). I asked them what they valued most from attending the conferences. I choose to ask this question mostly of young people whom I meet for the first or second time. A common theme in the dialogue is their joy in finding other people sharing the same professional interests, working in the same topical area, puzzling over the same scientific questions, and perhaps bouncing ideas off each other. It reminds me of when I ventured into packaging research many years ago. The topic was the mechanics of peeling and adhesion. I was very excited to find chemists, physicists and manufacturing engineers in my company sharing the same interest.

Meeting fellow professionals and building one's professional network is serious business. It was true then and it is doubly true today. IEEE's motto – *networking the world* – is a great motto for all of us to aspire to.

Conferences such as ECTC (USA), ESTC (Europe), and the coming IMPACT, IEMT, VLSI Packaging, EMAP and EPTC (Asia) are the more visible part of our global community gatherings. The regional, section and chapter level activities reach many people, some of whom are not able to travel far to attend the larger conferences. In the United States, regional workshops such as the Wireless Communication Workshop in Phoenix, Arizona, in November and the Emerging Technology and Chemical Sciences Workshop (joint with MRS and ACS) in Binghamton, New York, are community gatherings sponsored by the respective CPMT chapters at these two cities. Elsewhere in this newsletter you will read about a Japan Chapter seminar in Tokyo on September 20th as a kick-off of a

chapter revitalization initiative. During a European Chapter Chairs meeting in Dresden, Germany, I was pleased to learn from our colleagues in the region their ideas and experiences on chapter programs and to learn of plans for forming a CPMT Chapter in Norway. During ECTC in May the idea for forming a new CPMT Chapter in Ottawa was germinated, and we are looking forward to initiation of activities there. In the same vein, new topical technical committees are being planned (flexible electronics, avionics and automotive electronics, 3D packaging), while the inactive ones are being reviewed for new directions.

International and regional conferences, chapter seminars, and technical committee activities are like "town meetings" and "tea shop and coffee house" gatherings in the global village. The IEEE/CPMT *Transactions* are the trusted global village newspapers and wall posters. They serve another important sector of our professional community: those who strive to communicate the latest innovations and research, and those who hunger for the best knowledge and data. Authors, reviewers, editors and readers are all crucial stakeholders of our globally networked CPMT community. To them we owe the most respected set of technical journals in our profession.

Your CPMT Society has a strong volunteer base with passion and commitment. They organize and run conferences. They develop section and chapter programs. They are authors, reviewers, and editors for our Transactions. They are the backbone of the CPMT society. They are supported by our excellent staff and the IEEE infrastructure. We are experiencing a momentum of interest in CPMT professional activities across the globe in the USA, Asia and Europe. Let us ride with the momentum in facilitating our professionals networking the global IEEE/CPMT community.

Visit the CPMT Website (www.cpmt.org). See what is there that interests you. Give us your ideas and volunteer. We shall be delighted to hear from you.

### IEEE CPMT Society Board of Governors Meeting Summary (Continued from Page 1)

The Board of Governors present at the meeting confirmed the results of e-mail ballots as follows:

- 2006-01 Approve cosponsorship of 8th International Conference on Electronics Materials and Packaging (EMAP 2006):
   20% CPMTSociety/40% CPMT Hong Kong Chapter/40% HKUST APPROVED
- 2006-02 Approve cosponsorship of 31st International Electronics Manufacturing Technology Symposium (IEMT 2006):
   30% CPMT Society/70% CPMT Malaysia Chapter and IEEE Malaysia Section APPROVED
- Approve technical cosponsorship of 2007 International Conference on Thermal Issues in Emerging Technologies (ThETA 2007) APPROVED
- 2006-04 Approve proposed CPMT 2007 Budget Parameters:
  - o CPMT member fee: \$12 (no change from 2006)
  - o CPMT Student member fee: \$6 (no change from 2006)
  - o Trans on Components and Packaging Technologies
    - page budget 900 (no change from 2006)
    - member price \$12 (no change from 2006)
    - student price \$6 (no change from 2006)

- member interdisciplinary price (IEEE member) \$24 (no change from 2006)
- non-member list price \$580 ( \$555 in 2006)
- o Trans on Advanced Packaging
  - page budget 850 (800 in 2006)
  - member price \$12 (no change from 2006)
  - student price \$6 (no change from 2006)
  - member interdisciplinary price (IEEE member) \$24 (no change from 2006)
  - non-member list price \$540 ( \$515 in 2006)
- o Trans on Electronics Packaging Manufacturing
  - page budget 425 (400 in 2006)
  - member price \$8 (no change from 2006)
  - student price \$4 (no change from 2006)
  - member interdisciplinary price (IEEE member) \$20 (no change from 2006)
  - non-member list price \$485 ( \$465 in 2006)

### **APPROVED**

CPMT President William Chen reviewed his report, including newly-elected BoG members, newly appointed Strategic Program Directors (Awards, Region 10), CPMT Society response to IEEE TAB questions, the industrial environment and CPMT Society "treasures." He defined the next step in the Society's globalization efforts as building global communities. IEEE Division II Director Bob Lorenz presented a report on the IEEE Board of Directors Vision and Issues. This was followed by Society Vice President reports.

CPMT Vice President for Finance, Thomas Reynolds, reviewed his report and noted that the 2005 year-end surplus (unaudited) was \$558.6K - bringing reserves up to nearly \$3M. Vice President Reynolds presented a proposal for the 2007 Budget development process with the goals of developing a budget that is net zero or better and increasing ownership and accountability. A motion was made to approve development and submission of a 2007 Budget of net zero or better. Extensive discussion followed, with a focus on spending of reserves (and submission of deficit budget) to fund projects. The motion passed. Society Vice President for Technical, Dr. Rao Bonda reviewed his report on technical activities, including his plans and goals as follows: work with Technical Committees and CPMT web administration to update the websites by August 2006; identify plan and resources needed to update TC websites at least every three months; promote technical interests of our members and chapters through Technical Committees; increase the participation and collaboration of TCs in conferences in US and abroad; enhance communication with/among the TCs to share their activities; look for new and emerging technologies and form Technical Committees in those areas. Society Vice President for Education, Albert Puttlitz reviewed his report on the 2006 Motorola Fellowship competition and the Distinguished Lecturer program. Society Vice President for Publications Paul Wesling reviewed his report, including a new paradigm for Transactions Special Sections and planned ontologies/review articles for topical areas. He discussed the change in the revenue distribution algorithm for Transactions, the largest piece of which is tied to the number of articles downloaded by IEL customers (usually non-members). He stressed the importance of creating communication techniques to drive traffic to our articles. Society Vice President for Conferences Rolf Aschenbrenner reviewed his report, which included a summary of the 2006 conferences sponsored/cosponsored by the CPMT Society.

The standing committee reports were reviewed. Nominating Committee Chair, Dr. Philip Garrou, reviewed his report on the election of BoG Members-at-Large, noting that this would be the second election to implement regionally-proportional representation. Results are scheduled to be announced by November 17<sup>th</sup>, 2006. Fellows Evaluation Chair Dr. C. P. Wong reported that 8 candidates were reviewed by the CPMT committee, from countries including China, Hong Kong, Japan, as well as from USA and Europe. Fellows Search Co-chair Rao Tummala reviewed plans for soliciting nominations, including a coordination of efforts on a Regional basis led by the Strategic Directors for Regions 8 and 10. Constitution and Bylaws Chair Tony Mak reported that no changes were under consideration at this time.

Strategic Program Director Dr. C.P. Wong reported on the issue of supporting/encouraging student attendance at ECTC Professional Development Courses and the differing viewpoints of CPMT and ECA towards this. 56<sup>th</sup> ECTC General Chair Patrick Thompson requested that CPMT submit a proposal for resolution to the ECTC Executive Committee. CP Wong, Rao Tummala, Al Puttlitz and Philip Chan agreed to develop a proposal. 56<sup>th</sup> ECTC Program Chair Torsten Wipiejewski provided an overview of the results of the 56<sup>th</sup> ECTC. Incoming officers for the 57<sup>th</sup> ECTC were announced. Strategic Program Director Kitty Pearsall reviewed her report, including recipients of the 2006 CPMT Awards and plans for the 2007 Awards cycle. President Chen presented a report on behalf of Dennis Olsen, Chair, IEEE CPMT Field Award Committee, addressing the Committee's efforts to strengthen the nomination process and the positive response from CPMT BoG members. Strategic Program Director Ralph Russell reviewed his report on membership and Chapters, noting that as of April 2006, CPMT membership was down by 3% as compared to April 2005. He reviewed IEEE membership study data that defined the "at risk" group of members. Rolf Aschenbrenner reported on behalf of Strategic Program Director Johan Liu from Region 8, and presented a summary of the upcoming ESTC 2006 and initial plans for ESTC 2008. President Chen announced plans for the CPMT BoG delegation to ESTC, to include the President, VP Technical, VP Publications, VP Education, and Executive Director. Delegates will lead and/or participate in meetings and activities to help add value to the Conference, build the European CPMT community, and strengthen Chapters and membership. Strategic Program Director Charles Lee reported on upcoming conference activities in the Region, with a focus on EMAP 2006. Strategic Program Director William Brown summarized his report, which included reports submitted by the Chalmers (Sweden), Shanghai (in formation) and Georgia Tech Student Branch Chapters. Strategic Director Brown recommended implementation of a student poster competition at ECTC. 56th ECTC General Chair Pat Thompson expressed interest in the idea and agreed to bring it to the ECTC Executive Committee for discussion.

Kristine Martin, Potomac Communications Group reviewed her report, highlighting accomplishments with ECTC promotion, Award winner promotion and media placements.

The next BoG meetings will take place on November 10<sup>th</sup> and 11<sup>th</sup>, 2006, following the ECTC Paper Selection Meeting in Dallas, Texas, USA, and on June 1<sup>st</sup> and 2<sup>nd</sup>, 2007 following the 57<sup>th</sup> ECTC, Reno, NV, USA.

## **Charles Lee - Strategic Director for Region 10 - CPMT Board of Governors**



Charles Lee is currently a Principal of Materials Science and Technology Integration at Infineon Technologies Asia Pacific Pte Ltd, Singapore. He received the M.App.Sc degree in Materials Science and Engineering from the University of New South Wales, Australia in 1993.

Charles Lee began his professional career with Siemens Components Pte Ltd, Singapore (now Infineon Technologies Asia Pacific Pte Ltd) in 1993 as a Package Development Engineer. In Siemens/Infineon, he held several functions, spanning from spearheading research development to technology management. He supported package developments in materials characterization and qualification, deflashing and solder plating process. He has made numerous contributions on low temperature wire bonding, copper oxidation, popcorn improvement and surface cleaning issues of surface mount packages. In 1997, he was awarded the Regional Siemens 150 Years Innovation Award. Charles Lee is highly recognized within his organization for pioneering the adhesion technology of a novel inorganic adhesion system and its successful implementation in automotive and lead-free applications. In 2000, he was appointed by the Institute of Microelectronics, Singapore to lead an industrial Electronic Package Research Consortium project to develop a high performance System-in-Package.

In 2001, Charles Lee was promoted to the position of Principal, Materials Science and Technology Integration, at Infineon where he currently heads the Technology and Services Group in Asia Pacific. He is responsible for technology development of wafer dicing/thinning and flip chip programs, and providing modeling/simulation and analytical services for Infineon's Communications Business Group. To date, he has more than 10 patents on assembly packaging technologies and has contributed more than 40 publications in major IEEE conferences and journals.

Charles Lee is currently an elected member of the IEEE/CPMT Society Board-of-Governors (2004-2006) and was a recipient of the 2001 IEEE/CPMT Society Outstanding Young Engineer Award. He is also an executive committee member of the IEEE REL/CPMT/ED Singapore Chapter since 2000. He has been actively involved in the organizing committee of the Electronics Packaging Technology Conference (EPTC) from 1997 and has served as the International Advisory Board member since 2004, Past General Chairman in 2003, General Chairman in 2002 and Technical Chairman in 2000. He is also a member of the IEEE/CPMT Technical Committee on Materials and the Interconnect Program Committee of Electronic Components & Technology Conference (ECTC).

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## **Meet IEEE CPMT Society Transactions Editors**



**Dr. Ganesh Subbarayan** is a Professor of Mechanical Engineering at Purdue University. He was previously at University of Colorado (1994-2002) and at IBM Corporation (1990-1993). He holds a B.Tech degree in Mechanical Engineering (1985) from the Indian Institute of Technology, Madras and M. S. and Ph. D. (1991) de-

grees in Mechanical Engineering from Cornell University. Dr. Subbarayan's research is in Computational Mechanics with applications to Microelectronics. Dr. Subbarayan is a recipient of the 2005 Outstanding Contributions Award from ASME EPP Division, 2005 University Faculty Scholar Award from Purdue University, NSF CAREER award, the NSF Research Initiation Award, the 2003 Charles E. Ives Outstanding Paper Award from the Journal of Imaging Science and Technology, the 2002 Highly Commended Award from Soldering and Surface Mount Technology journal, the Itherm 2000 Best Paper Award, the 1996 Peter A. Engel Best Paper Award from ASME Journal of Electronic Packaging, and an IBM Invention Achievement Award. He has served on the program committees of several conferences including the ASME/Pacific Rim International Intersociety Conferences on Electronics Packaging (1997 program co-chair, 1999 reliability track chair, 2001 Modeling and Characterization track chair), ASME International Mechanical Engineering Conference and Exhibition (2002 Program Chair, EPP Division) and Intersociety Conference on Thermal and Thermomechanical Phenomenon in Electronic Systems (2002 program co-chair, Mechanics). He currently serves as the Editor-in-Chief of IEEE Transactions on Advanced Packaging. He has served as an Associate Editor of IEEE Transactions on Components, Packaging and Manufacturing Technology.

For future correspondence with Dr. Ganesh Subbarayan, his contact information is as follows:

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**Dr. R. Wayne Johnson** is a Professor of Electrical and Computer Engineering at Auburn University and Director of the Laboratory for Electronics Assembly and Packaging (LEAP). During his 19 years at Auburn, he has established teaching and research laboratories for advanced packaging and electronics assembly. Research efforts are

focused on materials, processing, and reliability for electronics assembly and for extreme environment electronics. Current research projects span the temperature range for -180°C to +485°C. He has published and presented numerous papers at workshops and conferences and in technical journals. He has also co-edited one IEEE book on MCM technology and written book chapters in the areas of silicon MCM technology, MCM assembly, automotive MCMs (IEEE Press), flip chip assembly and high temperature packaging (IEEE Press). He is the Editor-in-Chief of the IEEE *Transactions on Electronics Packaging Manufacturing* and served as an Associate Editor prior to this appointment. He was

elected a Fellow of IEEE in 2004 for 'his contributions to electronics that must operate in harsh environments."

Dr. Johnson received the B.E. and M.Sc. degrees in 1979 and 1982 from Vanderbilt University, Nashville, TN, and the Ph.D. degree in 1987 from Auburn University, Auburn, AL, all in electrical engineering.

Wayne is also a member of the International Microelectronics and Packaging Society (IMAPS), the Surface Mount Technology Association (SMTA) and IPC. He was the Technical Vice President of IMAPS from 2000-2004.

Editor's Note: Refer to June, 2006, issue of the Newsletter for profile of other CPMT Transaction editors.

## Interview with Dr. Avram Bar-Cohen, CPMT's Transactions Editor in Chief .....

By Dr. Vasudeva P. Atluri, Newsletter Editor



**Editor:** Tell us a little about yourself and your family.

**ABC:** I was born in 1946 and lived many of my childhood years in Brooklyn, NY, graduating from a neighborhood elementary school (PS225) and later Abraham Lincoln High School. I then headed to MIT for 3

engineering degrees, completing a PhD in Mech Eng in 1971. After a few years at Raytheon in Bedford, Mass, I joined the faculty at the Ben Gurion University in Israel, spent a sabbatical at MIT in the late 1970's, and following a second sabbatical, joined the corporate staff of Control Data Corporation in Minneapolis. In 1988 I accepted a faculty position on the Minneapolis campus of the University of Minnesota and spent some 14 years in the Mechanical Engineering Department running a laboratory dedicated to the Thermal Management of Micro and Nano Systems (TherMNs) and later directing the University's Center for Development of Technological Leadership. In 2002 I joined the Department of Mechanical Engineering at the University of Maryland as Professor and Chair and was named Distinguished University Professor in 2005. My current Laboratory, Thermal Packaging of Photonic and Electronic Systems (TherPES), provides me with the opportunity to keep studying the thermal aspects of these fascinating optical and semiconductor devices.

My wife, Anat, and I recently celebrated 40 years of marriage and now live in Washington DC, where she serves as Director of Programs for the National Breast Cancer Coalition. Our daughter Talia is a professional modern dancer in DC; our son Raanan is Director of on-line services for a major national publisher and lives with his wife and daughter in Brooklyn, NY; and our son Barak is President of a telecom investment company and lives in Princeton, NJ, with his wife and 2 sons.

**Editor:** Tell us how you got involved in the field of packaging and something about your career.

**ABC:** For as long as I can remember, I wanted to be an engineer and as a kid I was forever dreaming up ways to use technology to cure the world's ills. My father was a master plumber – and later a technical high school teacher – and the weekends I spent as his "go-fer" (helper) – threading pipes, melting lead with a torch for sealing cast iron waste pipes, trying to "persuade" 20ft segments of steam pipes into align-

ment, and coaxing a furnace back into operation - taught me the love of all things thermal and the joy of seeing a system spring into life, after arduous assembly and fabrication.

My MS Thesis at MIT, under the supervision of Prof. Art Bergles, dealt with direct contact heat exchangers and I had intended to begin my career in applications of solar energy and development of desalination systems. But, my first real job in 1968 was as an R&D Engineer at Raytheon, working on military electronics and radar systems, dealing – of course – with thermal management issues. I quickly became fascinated with the thermal challenges inherent in these miniaturized solid state logic, memory, and phase shifter devices and in 1969 – with Raytheon's support returned to MIT to pursue a PhD in immersion cooling with Art Bergles. Two years later I resumed my career at Raytheon as a Section Manager for Advanced Thermal Management.

When my attention began to encompass the assembly of devices into compact, later miniaturized, systems, a talent for visualization and geometric reasoning helped me transition into the broader domain of packaging. No one could pack a suitcase or the trunk of a car better than my father and in later years – though he didn't know much about electronic packaging - we would compete on who could get to the higher "packaging density" in these more mundane applications. I rarely won the competition, but the acquired subtle skill in exploiting the 3rd-dimension has served me very well.

**Editor:** What do you see as the needs of our members around the world – what are the most important issues the CPMT Society can address?

**ABC:** It has been my privilege these past few decades to witness and participate in the transformation of electronic packaging from a field dominated by "art" to a field with a growing scientific base. Like a Mangrove or a Banyon tree, and some other domains of engineering, packaging science - the "roots" - have grown from packaging practice - the "branches." Today there is little tolerance for the "trial and error" approach of the past and products must be "correct by design" on the day they are released to the commercial marketplace. The growing sophistication of packaging science, facilitating the use of fundamental relations for the prediction of performance and failure and helping to identify barriers to greater precision, predictability, and reliability, has allowed the packaging community to keep pace with the Moore's Law cadence and assure the continued progress in miniaturization, performance, and reliability we now take for granted in electronic systems.

The CPMT Society is today one of the most important depositories for, and guardians of, the packaging knowledgebase, including the collective memory of where we have been, the roadmap of where we are going, and the techniques and tools that will get us there. Through the publications, workshops, conferences, tutorials, and the more diffuse CPMT-centered professional networks, CPMT makes it possible for our members to be part of a "learning community," applying progressively more sophisticated solutions to emerging packaging problems.

**Editor:** What are your visions for the society in short and long term? Where do you see the Society (and your area within it) in 5 to 10 years?

**ABC:** In the short term CPMT must continue to refine its "value proposition," finding new ways to more efficiently create, showcase, and disseminate packaging knowledge at an affordable price

for its members and for others in the packaging and system integration community. Due to the intensity of present economic competition – across product domains and continents – corporate and even governmental investment in knowledge creation and consolidation, with some exceptions, is far below what is needed to meet society's expectations for performance, reliability, and cost of tomorrow's engineered systems.

I believe that in the future, when cheap labor, cheap raw materials, and cheap energy are no longer available anywhere on the globe, the need for new technology and desire for financial rewards will drive a wave of re-investment in corporate R&D, albeit leaner than in the past, more international than in the past, more integrated than in the past, more impatient than in the past, and probably more efficient than in the past. But until that day, CPMT must - in some ways - play the role of the monasteries during the "dark ages" - safeguarding generations-old techniques and insights, until the dawning of the Enlightenment, when the broader society once again embraced and supported scientific inquiry and technological exploration. A day will come when the private and public economic institutions will once again recognize the need for broad - rather than trendy - investment in science and technology with a time horizon for useful results that is not measured by the number of months to the next financial statement. Until that time, CPMT must play the crucial role of "packaging guild." When we arrive at the inflection point, it will be time to develop a more cooperative partnership style with the major economic and educational institutions and – at that time – we may very well experience a renaissance of the old model of corporate-supported volunteerism that drove the early growth of CPMT and other professional societies.

**Editor:** What are your plans for the Society within your Publications area?

**ABC:** As you may be aware, the CPMT BOG has created this new position of CPMT Editor in Chief and asked me to champion the transition of our 3 Transactions (Components and Packaging Technologies, Advanced Packaging, and Electronic Packaging Manufacturing) from "well managed" to "high impact." Working with Paul Wesling, the CPMT VP of Publications, and the editors of the individual Transactions, we hope to solidify the CPMT Transactions as the venue of choice for obtaining and publishing cutting edge knowledge in packaging art and science.

By better managing the selection, review, and publication of submitted manuscripts we hope to consistently attain an Impact Factor of at least unity for each of our Transactions. This is the threshold for quality in engineering journals and would mean that, in the two years after publication, each published manuscript, on average, would be cited at least once in the scientific/engineering literature. We are well on our way towards attaining, and perhaps exceeding, this target. We are also working to "raise the bar" on acceptance of manuscripts, by including consideration of the "significance" of the work, along with its "correctness."

Readers will soon begin to see evidence of a change in the "Special Sections" appearing in the Transactions, as we capitalize on this component of the Transactions to highlight emerging or "break through" areas by moving from conference-based to topic-based groupings. Readers can also expect to find greater consistency in the topical coverage of each of

the 3 Transactions, as we continue to refine the specific domains of interest of the Transactions and actively re-direct submitted manuscripts to the most appropriate Transactions. We are also actively supporting the creation of "ontologies" that will define the key publications in specific domains of CPMT's interests and help our readers keep abreast of these developments.

**Editor:** What would be your advice to engineers who are in or entering this field for career growth?

**ABC:** To succeed, you have to be passionate about your work and never stop learning! here are few professions that can be as rewarding as engineering, with many opportunities for creativity, problem solving, working with and sometimes directing teams of smart people, and tackling many of society's unmet needs; all this for pretty decent salaries and significant equity in, or outright ownership of, new products and organizations. However, the pace of knowledge obsolescence is murderous. If early in your career you do not commit to life-long learning, your mid-career years will turn into an "end of (technical) life" scenario.

Editor: Where (on what tasks) could you use help from members?

**ABC:** I would very much like to see much greater involvement of the membership in the three CPMT Transactions. Not just in writing more papers – that would be good, but we do generally attract a large number of submissions to the Transactions – but, more importantly, in volunteering to review papers and doing so carefully, in integrating the findings into packaging practice and packaging research, in commenting on what is working and what isn't in Letters to the Editor, Open Forum pieces, or Review articles, and in contributing to the scientific/technological dialog by citing these publications in subsequent manuscripts. At the present time, we are falling short in all 4 of these areas.

**Editor:** What do you like to do in your spare time?

**ABC:** Fortunately, I have so little spare time that it is not a problem to fill it. As my wife will tell you if asked, "Avi works whenever he is not doing anything else." But, together with my wife, friends, and our family, we do enjoy supporting and watching the performing arts – from dance to opera to theatre to jazz – and being out in the great outdoors – from mountain biking to canoeing and from hiking to a Mechanical Engineer's special delight - snowmobiles and RV's.

Editor: Thank you, Avi.

## Interview with Marsha Tickman, Executive Director, IEEE CPMT Society .....

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By Dr. Vasudeva P. Atluri, Newsletter Editor

Editor: Tell us a little about yourself.

Marsha: I'd start with my twenty years at IEEE in various positions within Regional Activities (working with Sections and Chapter officers), Educational Activities (supporting the Educational Activities Board and its Committees), Membership (managing the admission and advancement and membership development activities), and Technical Activities (supporting activities of Societies, Councils and their volunteers.)

I've now spent ten years as Executive Director of the CPMT Society in the one-person Executive Office. I'm responsible for managing the business operations of the Society and supporting

volunteer leaders in areas including governance, finances, publications, conferences, and membership.

**Editor:** What do you see as the needs of our members around the world – what are the most important issues the CPMT Society can address?

Marsha: Our members (and non-members for that matter) need access to information that will allow them to succeed and advance in their careers. Whether the source of this information is publications (either in print or on-line), conferences, workshops, professional development courses, Chapter meetings or "informal networking," – the CPMT Society provides it all. High quality, peer-reviewed Transactions, available online and in print; Conferences in the Asia, Europe and USA – such as EPTC and EMAPS, ESTC, and ECTC – that attract the leading technologists as both presenters and attendees; Chapter meetings that bring together local groups for short presentations and networking. Many opportunities exist to serve the individual needs – and fit the individual's schedule.

**Editor:** What would be your advice to engineers who are in or entering this field for career growth?

Marsha: Become a CPMT Society volunteer. This may sound like a self-serving suggestion (yes – the Society relies on a few thousand volunteers to accomplish its goals and serve its members) – but volunteers will find that they gain as much as or more than they give. Volunteering within the CPMT Society provides opportunities to network with other technical professionals and gain valuable management and leadership skills. There are many areas in which to volunteer: Serve on the program or organizing committee of a conference or workshop; become a reviewer or associate editor for the Transactions; work with your local Chapter.

Editor: Thank you, Marsha.

### Highlights of ICEPT2006 Shanghai, China

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Submitted by Dr G. Q. Zhang from Philips Semiconductor

The 7<sup>th</sup> International Conference on Electronics Packaging Technology (ICEPT 2006) was held successfully in Shanghai from August 27 to 29, 2006. ICEPT is sponsored by CEPS (China Electronic Packaging Society) and IEEE-CPMT. It is the major international electronic packaging conference in Mainland China, organized, authorized and supported by Chinese central (such as Ministry of Information Industry, etc.) and local authorities.

The focuses of ICEPT 2006 cover all the important elements of value chain for electronic packaging, from materials, equipment, concept development, design, process, manufacturing and assembly, reliability and qualification, and applications. Both mainstream Semiconductors technologies (Moore's law) and More than Moore are covered. Advanced short courses on Advances of Microelectronic and Microsystems Packaging, Designing for Reliability and LED Packaging were given by four distinguished instructors.

In total more than 350 people, representing more than 200 different organizations, covering 16 countries and districts, attended this conference. Although it is the first year that ICEPT changed from once per two years to an annual interna-

tional conference, the numbers of participations are satisfactory. It is anticipated that the number of participants in ICEPT2007 will recover to about 500. The conference received 202 contributing papers, 21 invited keynote presentations, organized in 13 technical sessions. A number of papers were granted with "Philips Semiconductors Best Paper Awards". Note that Philips Semiconductors becomes NXP Semiconductors from 1 September 2006.

As the general chair of ICEPT2006, Prof. K.Y. Bi summarized the development trends and key data of Chinese packaging industries and R&D status. Member of Chinese Academician Shichang Zou presented the trends and status of Chinese Semiconductors industries. The vice secretary-general of CIE (Chinese Institute of Electronics) Zhi-wu Li also highlighted some key development trends and status in China. William Chen, Bill Bottoms, R. Yang, R. Aschenbrenner, G.Q. Zhang and other distinguished plenary keynote speakers presented their vision and research results in the keynote session.

Due to the transition from once per two years to an annual event, some organizing and technical issues should and must be improved. In the committee meetings, the problems occurred during ICEPT2006 were analyzed, and suggestions for ICEPT2007 were collected. It is strongly believed by all the members of committees that ICEPT2007 will be an even great success.



Prof. Ke-Yun Bi President of CEPS



Prof. Shang Tong Gao Vice President of CEPS

### ESTC 2006 1<sup>st</sup> Electronics Systemintegration Technology Conference

Submitted by Thomas Zerna, Conference Executive Chair

More than two years ago during a meeting in Shanghai some CPMT colleagues from Europe, USA and Asia discussed the necessity to improve CPMT conference activities in Europe. *Klaus-Jürgen Wolter*, Director of the Electronics Packaging Laboratory of Dresden University of Technology, German, and meanwhile member of the CPMT BoG, together with his team took the initiative to start organizing a European, but international conference.

Now, two years later, the 1<sup>st</sup> Electronics Systemintegration Technology Conference, ESTC 2006, held from September 5 to 7 in Dresden, Germany, has become reality. And, to come to the point, ESTC 2006 was a really great success! But, let's go back to the beginning.

The conference title already emphasizes the focus of the conference: Systemintegration.

Looking back one of the perhaps most important activities in the early beginning of organizing this conference was to found a program committee which is indeed international. 97 scientists from 25 countries, led by the Conference Program Chair *Chris Bailey* from Greenwich University, UK, did a really great job.

Following the successful model of ECTC, the world wide most important conference in electronics packaging, the ESTC program

committee announced ten major topics. These topics and the responsible Subcommittee Chairs have been:

- Advanced Packaging Rolf Aschenbrenner, Fraunhofer IZM Berlin, Germany
- Materials and Processing Johan Liu, Chalmers University of Technology, Goeteborg, Sweden
- Optoelectronics Torsten Wipiejewski, Firecomms Ltd., Cork, Ireland
- Manufacturing Technology David Whalley, Loughborough University, UK
- Microsystems Packaging Zsolt Illyefalvi-Vitez, Budapest University of Technology and Economics, Hungary
- Electrical Modeling Flavio Canavero, Politecnico di Torino, Italy
- Thermal-Mechanical Modeling Bernd Michel, Fraunhofer IZM Chemnitz, Germany
- Emerging Technologies Jorma Kivilahti, Helsinki University of Technology, Finland
- Quality and Reliability Hans-Jürgen Albrecht, Siemens AG Berlin, Germany
- Passive Components Paul Svasta, "Politehnica" University of Bucharest, Romania

Additional subcommittees where focused on preparing the poster presentations and professional short courses:

- Poster Committee Pavel Mach, Technical University Prague, Czech Republic
- Short Courses Committee Bernard Courtois, TIMA-CMP, Grenoble, France

Another very important fact was the wide cooperation in organizing the conference. The local organizers, that means the Electronics Packaging Laboratory of Dresden University of Technology and the "Society for Knowledge and Technology Transfer of Dresden University of Technology Ltd." (German abbreviation GWT-TUD GmbH), have strongly been supported by IEEE-CPMT. Additional support came from the respective German association, which is the VDE-GMM (German Association for Electrical, Electronic & Information Technologies - Society of Microelectronics, Micro and Precision Engineering), IMAPS Germany and Silicon Saxony, Germany's largest trade association for the microelectronic industry.

The first conference day started with six half-day short courses where attendees have had the possibility to improve their knowledge about special topics. Those six short courses where attended by more than 50 people.

The technical program of the conference was started with an opening session in the afternoon. *Klaus-Jürgen Wolter* welcomed all attendees and announced the technical program including **8 Keynote Presentations**, an evening **Panel Discussion**, some **160 oral presentations** and **60 poster presentations** as well as a **3-day industrial exhibition** with 22 companies and organizations presenting their latest products and developments. The official opening entitled "Micro-/Nano-/Bio-Technologies and Lifelong Learning - Key Factors for the Development of an Industrial Society in a Global Environment" was given by *Kurt Biedenkopf*, former Prime Minister of Saxony and Honorary President of Dresden International University. The first two keynote presentations where held by *Herbert Reichl*, Director of Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin, Germany, and *Thomas* 

Zeiger, Product Manager at Siemens AG, A&D, Optical Solutions, Munich, Germany. Herbert Reichl addressed his vision about the future developments in electronics packaging in his presentation entitled "Systemintegration Technologies for Autarchic Miniaturized Sensor Systems". The presentation was a perfect overall introduction into the field of systemintegration the whole conference was dedicated to. Thomas Zeiger introduced the new concept of Siemens to integrate SMD assembly machines and Flip Chip bonders into one platform entitled "Chip Assembly Today and Tomorrow". The opening session was completed by a welcome address from CPMT, presented by William Chen, CPMT President. He leaded the CPMT delegation with Marsha Tickman, Rolf Aschenbrenner, Rao Bonda, Al Puttlitz and Paul Wesling.



Klaus-Jürgen Wolter, opening ESTC 2006



Audience during keynote sessions

After this the presentations of technical papers started, scheduled in five parallel technical session streams. The day ended with a Welcome Reception, where all the attendees enjoyed socializing with each other.

The second conference day was continued with technical sessions with high quality presentations. The keynote presentations where continued as well. In two different sessions the very important topic of lead-free electronics and especially the problem of tin whiskers where addressed, completed by two presentations about the specific demands of the product branches avionics and automotive on electronic products. Michael Pecht, Chair Professor and Director of CALCE Electronic Products and Systems Center, University of Maryland, USA, presented "Today's and Future Challenges Concerning Lead-free Electronics". Katsuaki Suganuma, Director of Nanoscience and Nanotechnology Center, Institute of Scientific and Industrial Research, Osaka University, Japan, spoke about "Low/high Temperature Lead-free Soldering, Tin Whiskers and Next Steps Towards the Future". The avionics industry was represented by Josephine Vann, Principal Component Engineer, Smiths Aerospace UK. She explained "Future challenges for the Qualification of Electronic Components for Avionics Applications". The specific demands of automotive industry were emphasized by *Steve Prosser*, Chief Engineer – Technology, Electronic Control Systems, TRW Automotive, Solihull, UK, with his presentation "Advanced Automotive Electronic Systems: Packaging & Environmental Challenges".

The evening Panel Discussion entitled "Next Generation Interconnects, Packaging and Systemintegration" was undoubtedly another highlight of the conference beside the keynote presentations. This discussion was organized and chaired by *Rao Bonda*, CPMT Vice President Technical. He introduced the four outstanding short presentations by worldwide leading experts:

- Packaging Innovations on Rise William Chen, Senior Technical Advisor, ASE, Inc., Santa Clara, CA, USA
- 3D Interconnection and Packaging Eric Beyne, Director, Advanced Packaging and Interconnect Center, IMEC, Leuven, Belgium
- Packaging and Integration of Components, New Challenges on Wafer Level Packaging - Gilles Poupon, Program Manager, Packaging and Interconnections Group, CEA-LETI, Grenoble, France
- Advanced Assembly and Packaging Technologies for Miniaturized Microelectronic Systems - Klaus-Dieter Lang, Deputy Director, Fraunhofer IZM, Berlin, Germany



Audience during the evening discussion

The third conference day completed a high quality and really busy technical program of the conference. In addition to the technical sessions another keynote session was held, presenting two different topics. *Ralf Plieninger*, Senior Director Technology, Assembly and Test, Communications Group, Infineon Technologies AG, Regensburg, Germany, emphasized "Challenges and New Solutions for High Integration IC Packaging". From the view of semiconductor industry he contributed new aspects to the topic of systemintegration. "Microelectronic Technologies for the LHCb Experiment at CERN - A Challenge for the Electronics Packaging", presented by *Udo Dehne*, Sales and Marketing Director, RHe Microsystems GmbH, Germany, showed a special application of electronics packaging for the large hadron collider (LHC), a particle accelerator at CERN.

During the closing session *Thomas Zerna*, Conference Executive Chair, announced some statistical data. The conference was attended by 395 people from 26 countries. 38% of the attendees came from industry, another 38% from universities, 19% from research institutions and the remaining 5% from organizations and societies.

ESTC 2006 awarded the best presentation and the best poster. The Best Presentation Award went to:

"C4NP as a High-Volume Manufacturing Method for Fine-Pitch and Lead-Free FlipChip Solder Bumping" by *Klaus Ruhmer*, SUSS MicroTec AG, Germany; *Eric Laine*, SUSS MicroTec, Inc., USA; *Eric Perfecto*, *Hai Longworth* and *David Hawken*, IBM Microelectronics, USA.



Panel during the evening discussion Left to Right: Gilles Poupon, Eric Beyne, William Chen, and Klaus-Dieter Lange

The Best Poster Award went to:

"High Energy Density Magnetic Materials for Electronic Packaging" by Wilhelm Kappel, Mirela M. Codescu, Nicolae Stancu, Jana Pintea and Eros Patroi, Incdie ICPE-CA, Romania.

The next ESTC will take place in 2008 in Greenwich, London, UK. A challenge cup, created by the ESTC 2006 Organizing Committee, was handed over by *Klaus-Jürgen Wolter* and *Thomas Zerna* to *Chris Bailey*, Program Chair of ESTC 2006 and General Chair of ESTC 2008, and to *Nihal Sinnadurai*, CPMT Chapter Chair UK and Ireland and Executive Chair of ESTC 2008. *Chris Bailey* presented an outlook to ESTC 2008.



Handing over the ESTC Challenge Cup Left to Right: Thomas Zerna, Chris Bailey, William Chen, Klaus-Jürgen Wolter, Nihal Sinnadurai

During his closing address CPMT President *William Chen* assessed ESTC 2006 as a great success and acknowledged all people having been involved in the conference organization.

The conference was finished by a beautiful river tour in the evening. Detailed information about the technical program and some impressions of the conference as well as first information about ESTC 2008 are available at www.estc-conference.net.

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## **IEEE-CPMT Society Awards for Year 2007** (Continued from Page 1)

While a nominee may have a specific award in mind when applying, the Awards and Recognition Committee reserves the right to consider any nomination for awards other than the award suggested when, in its opinion, the support and justification may more appropriately apply to a different CPMT Society award. Winners will be notified by 28 February 2007 and the awards will be presented at the 57th Electronic Components and Technology Conference, May 29- June 1, 2007, in Reno, Nevada, USA.

After reviewing the high level summaries presented below, you will find a list of nomination submission requirements. The awards nomination form can be found on the CPMT Society Home page (www.cpmt.org/awards).

David Feldman Outstanding Contribution Award: This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.

Prize: \$2,500 and Certificate

**Basis for Judging:** Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.

**Eligibility:** Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2006.

➤ Outstanding Sustained Technical Contributions Award: This award recognizes outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society.

Prize: \$2,500 and Certificate

**Basis for Judging**: Technical contributions must be sustained and continuing over a period of at least five (5) and preferably ten (10) years. One major contribution *will not* qualify. Contributions must be documented by open literature publications such as papers, patents, books and reports (available to the public).

**Eligibility**: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2006.

➤ Electronics Manufacturing Technology Award: This award recognizes major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.

Prize: \$2,500 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.

**Eligibility:** No need to be a member of IEEE and CPMT Society.

Exceptional Technical Achievement Award: This award recognizes an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.

Prize: \$2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved by most members. A single major contribution *will* qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-theart in CPMT's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

**Eligibility:** Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2006. There are no requirements for service to the IEEE or CPMT Society.

➤ Outstanding Young Engineer Award: This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.

**Prize**: \$1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

**Eligibility**: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2006, and must be 35 years of age, or younger, on December 31<sup>st</sup>, 2006. Please provide Date of Birth (Month/Year) to ensure eligibility.

### **Guidelines for Nominators:**

- Minimum three (3) reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members.
- Past recipients of an award are not eligible to receive that same award a second time. For a list of past awardees, see the CPMT Society Home page located at www.cpmt.org/awards.
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.
- Please send nominations to CPMT Awards Committee Chair by e-mail, fax or mail. If you fax a nomination, please followup with an email.

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Email address: kittyp@us.ibm.com

### Member-Get-A-Member Program Gets An Upgrade For 2007

Submitted by Ralph W. Russell, II IEEE CPMT Society Strategic Director for Membership and Chapter Development

Beginning in September of this year, the Member-Get-A-Member (MGM) program will undergo several significant enhancements. First, the payout for recruited higher grade members will be raised from the current \$5.00, to \$15.00 per member. Further, recruiters will have the option of using their reward vouchers to pay for IEEE products or services (including their membership renewal), or, if they prefer, they can choose to use the vouchers to have a donation made in their name to the IEEE Foundation.

The MGM program has been one of our more successful recruitment programs. Please spread the word of these important changes and help to make this program even more successful in 2007. Find out more at **www.ieee.org/mgm.** 

To assist members who wish to participate in the program, some tools have been developed. These include a descriptive brochure of the MGM program with recruiting tips, and an IEEE-logo'd business card with space where the recruiter can fill in their name and member number. The brochures for the 2007 program will be available in September, while the business cards are available now. Both can be ordered online at: www.ieee.org/ra/md/mdsupplyform.html.

Please note that the vouchers for the 2006 MGM program, which will be issued during September, will be calculated under the 2006 program rules. No changes have been made to the Student-Get-A-Student (SGS) program.

### **Chapter News**

Region 10 Chapter Activity Round-up By Dr. P.B. Parikh, Region 10 News Coordinator TAIPEI CHAPTER:

**Prof. Lih-Shan Chen-** Chairman of Taipei CPMT Chapter has reported the following activities during this quarter.

As reported in our previous issue, CPMT Taipei Chapter coorganized the "2006 International Symposium on Advanced Packaging and Green Packaging Technology", with IMAPS Taiwan Chapter. This four day event was held from June 28th to July 1st, 2006 at the Taipei World Trade Center, Taipei, Taiwan. More than 120 participants took part in this seminar. Besides the technical program, there was an Exhibition for four days of the seminar.

Invited speakers at the seminar included

- Dr. Ho-Ming Tong "IC Packaging Trends and Challenges from New Packaging Materials".
- ii) **Dr. Michael Pecht** "Accelerated Testing; Ways to Understand Reliability Quickly and Accurately".

Dr. William T Chen- President of IEEE CPMT Society and Dr. Ho-Ming Tong - President of Advanced Semiconductor Engineering (ASE) Inc. visited Dr. Shen-Li Fu Chairman of IEEE CPMT Taipei Chapter on 2<sup>nd</sup> August, 2006 and had discussions on the affairs of the Society.

#### MALAYSIA CHAPTER

**Dr. Ch Chew** –Chairman of Malaysia CPMT Chapter, has reported that the chapter activities have picked up and the chapter has become more eminent and diversified with joint efforts from the newly pulled-in committee members from FREESCALE, INTEL and INFINEON.

The following talks have been planned and being conducted during this quarter by the chapter;

- i) "Applications of FEA in Semiconductor packaging design"
- ii) "Analytical tools in Semiconductor Industry".

The executive committee members of the chapter are busy preparing for the International Conference on Electronics and Manufacturing Technology (IEMT 2006 – 8,9,10 Nov) and four informative DLPs. These are to be held for the first time in KL Asia with the support from CPMT SCV, IEEE and various industry sponsors.

Around 78 papers and more than 20 posters have been selected out of 130+ abstracts received till date. In addition to a well organized technical conference as above, the organizers have assured varieties of food, sceneries and cultural shows of Malaysia.

Further information for registration and conference details can be obtained from the link **www.ieee.org.my/iemt2006**/.

The Chapter Officers and the Committee members for 2006 are

Chair: Dr. CH Chew, ON Semiconductor
Vice Chair: Dr. Ishak Abdul Azid, University Science

Malaysia

Treasurer: Azhar Aripin

Committee Members: Dr. Chee Choong Kooi, Intel

Wee Teck Lim, ON Semiconductor

Fuaida Harun, Infineon

Shutesh Krishnan, ON Semiconductor

LC Tan, Freescale

#### IEEE INDIA COUNCIL CHAPTER

The chapter has launched a well organized membership drive since October 2005 through our contacts with the electronic component industry and the academic institutions. Effective presentations on IEEE CPMT Society activities in India and at global levels were made during the three co-organized events (seminars and conferences) during the year. One more such opportunity will be availed during the forthcoming annual IEEE India Council seminar in December 2006.

Due stress is being placed on increased awareness of the activities of the CPMT society and the need for knowledge sharing on latest technological developments in the areas of electronic component production and electronic equipment manufacturing activities including Surface Mount Technology.

### IEEE CPMT Phoenix Chapter Tutorial Update

Submitted by Dr. Mali Mahalingam IEEE CPMT Phoenix Chapter

### Thermal Design and Management in Electronics

Thermal design and management challenges are common across a wide range of electronic products and applications. Road mapping by leading organizations (ITRS, SIA, and NEMI) identifies thermal management as one of the key enablers for the sustained growth in electronics industry. Higher density, increasing performance, robust reliability requirements and lower cost demand much from the thermal management professionals in creating thermal solutions. This half-day tutorial organized by the IEEE CPMT Phoenix Chapter was taught by four Phoenix area professionals and addressed: Modeling and Characterization, Design & Applications challenges in the Computational and Wireless Communication Products, and Emerging Technologies. Nearly sixty professionals took advantage of this professional learning opportunity.



Dr. Tom Lee, Freescale Semiconductor Inc., discussed "Simulation and Characterization Methods in Electronics Thermal Design and Management". Thermal simulation and characterization are two essential tools to evaluate and optimize thermal performance of elec-

tronics products. Experimental characterization usually can provide a direct and accurate way to measure device or package temperature; however, the efforts to prepare samples and the number of experimental matrix needed may be time consuming and sometimes costly. On the other hand, advancements in software and computing speed make modeling and simulation as effective methods in analyzing and predicting thermal performance. However, the uncertainty in material properties, modeling simplification and assumptions, plus various numerical meshing techniques may limit the accuracy of the results. Careful use of both experimental characterization and simulation can make up for the deficiency in each and provide realistic and accurate results. Infrared (IR) Thermal Imaging is a direct tool to measure the surface temperature, both for the area thermal field and for detecting the local hot spot. A simulation and modeling methodology generally includes model building, assigning material properties, assigning boundary conditions, meshing, numerical solution, and post processing for temperature and flow visualization. There are a variety of Finite Element Method-based and Finite Volume Method-based software tools available in the market. Each tool has its uniqueness and limitations. The recent trends for commercial codes are: enhanced interfaces with MCAD and ECAD tools; add-on capability for board-level thermal analysis; ability to create Compact Thermal Models (CTM); Improved parametric and design optimization capabilities; and supporting 64-bit processors for computational efficiency.



Dr. Chia-Pin Chiu, Intel Corporation, presented "Thermal Design and Management for High-Power Microprocessors". Increasing microprocessor performance has historically been accompanied by increasing power and increasing on-chip power density

both of which present a cooling challenge. With the transition to multi-core microprocessor architectures, dramatic increases

in Thermal Design Power (TDP) are not observed to occur when processor performance increases. Thermal designers still need to account for areas of thermal non-uniformity typically referred to as hot spots, where power densities of 300+ W/cm2 are possible. These hot spots typically caused by a non-uniform distribution of power dissipation on the die will dictate reliability and performance. In addition to the die, the hot spots can also occur in the interconnect, package substrate, and socket contacts due to Joule heating. It must be noticed that processor current levels have increased over the past two decades. Industrial and academic researchers have correspondingly increased their focus on elucidating the problem of hot spots and developing innovative solutions in devices, circuits, architectures, packaging and system level heat sinking. The current strategy is to enhance heat spreading and reduce package thermal resistance. This is followed by additional system-level thermal solution such as liquid cooling and refrigeration.



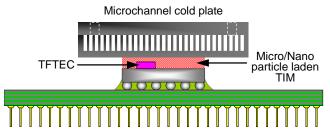
Dr. Mali Mahalingam, Freescale Semiconductor Inc., presented "Thermal Design and Management for RFPAs in Wireless Applications". Similar to Microprocessors being the key component in computing applications, Radio Frequency Power Amplifiers (RFPAs) are the key components in the wireless communication applica-

tions. Trends in power levels for RFPAs used in both mobile products and fixed infrastructure equipment were reviewed. Thermal design and management at the component level are conduction dominated. The presentation addressed both the fundamental aspects of conduction heat transfer and the state of the art practices in creating successful solutions at the product level. RFPA devices in a mobile phone, even as they dissipate small amounts of heat (~ 1+ W), are in a very limited space and require careful thermal solution; device layout, die thinning, and thermal vias in the Printed Circuit Board (PCB) play key roles in achieving effective thermal management. RFPA devices in basestations dissipate large amounts of heat (~ 5W - 250 W) and pose many tough thermal challenges; at the device level they represent one of the highest thermal density among electronic devices (~ 3 kW/cm<sup>2</sup> at die level); die layout to reduce spreading resistance, die thinning, improved metallurgical bond to reduce bond resistance, engineering high thermal conductivity substrate materials, and reducing interfacial contact resistance by managing flatness & surface roughness all play key roles in the thermal management at the component level. For basestation equipment, at the system level, cooling is primarily by free and forced air convection utilizing large heatsinks.



Dr. Ravi Prasher, Intel Corporation, discussed "Micro/Nanotechnology in Electronics Thermal Management Applications". There are two thermal problems in microprocessors: increasing total power dissipation and non-uniform heat generation that gives rise to multiple hotspots. The design requirement for electronics cooling is

to maintain the hottest location (hotspot) on the die (chip) below the specified temperature. Due to the presence of multiple hotspots, the thermal resistance near the die (package) is high; thus the focus of next-generation electronics cooling is on developing efficient cooling solutions near the package. Futuristic cooling solutions may be based on micro and nano technologies. The schematic of such a cooling solution is shown in below figure. These solutions might include a Thermal Interface Material (TIM) made from micro and nanoparticles, a microchannel heat exchanger, and a Thin Film Thermoelectric Cooler (TFTEC) that is made of thin film superlattices, or nanocomposites, placed directly above the hotspots to provide localized cooling. To enable these micro/nanotechnologies, however various challenges must be met. The main challenges are a) to reduce the boundary/interface resistance between the nanoparticles and the host medium for nanoparticles-based TIMs and to increase the reliability performance of TIMs, b) reduce the assembly-related parasitic effects seen in TFTEC, thus improve the effective Figure of Merit, ZT and c) pumping requirements and pump reliability for microchannel cooling.



Schematic of futuristic thermal solutions

### **Failure Analyses for Electronics Packaging**

This half-a-day tutorial organized by IEEE CPMT Phoenix section was taught on Sept. 19<sup>th</sup> 2006 by four Phoenix area professionals. Basic methods, tools and techniques practiced in the failure analyses of electronic packaging were addressed with an in-depth discussion on acoustic microscopy. Applications in Eutectic die attach, Pb-free solders, Plastic Packaging and Flip Chip Interconnect were discussed. The tutorial looked beyond the limitations of current day's tools and techniques to address the needs of next generation interconnect and package technologies. Nearly forty five professionals took advantage of this professional learning opportunity.



Dr. Jonathan Harris, CMC Interconnect Technologies, discussed "How Interfacial Structure Can Play a Major Role in Package Reliability?" He explained what IMCs (Inter Metallic Compounds) are and the general role of IMC's microstructure on the reliability of package construction. Specifically, he elabo-

rated on the role of intermetallic compound morphology in determining failure modes when mechanical stress is applied to the package. His examples were drawn from AuSi and AuSn eutectic attaches as well as Pb free solder SnAgCu. He also explained for each of these three examples how to control the microstructure of IMCs to minimize their impact on interfacial reliability.



Mr. Ken Tylor, Sonoscan, Inc., presented an "Introduction to Acoustic Micro Imaging and Its Applications". Ultrasound is a form of mechanical energy and is, therefore, sensitive to the elastic properties of the materials it travels through. It is particularly sensitive to

locating air gaps (cracks, delaminations and voids). Acoustic Micro Imaging (AMI) uses high frequency ultrasound (5 – 300MHz) to image internal features and characterize physical defects that occur during the manufacturing process or environmental stress. In his presentation, Ken provided an over-

view of the basics of ultrasound, how it is used for Acoustic Imaging, and explored a wide variety of applications (die attach void, interfacial delamination in plastic encapsulated ICs, power devices and flip chip packages). He covered the role of AMI in industry standards and current developments for improved imaging techniques.



Dr. Dev Gupta, APSTL, presented "Failure Analyses for Flip Chip Packages". Dev emphasized on the philosophy of FA analyses for Flip chip packaging, from the traditional analyst approach, from the team (design, material. Process) approach and finally from the root cause

analysis i.e a unified approach. Dev walked through the basics of Flip chip packaging technology (bump, substrate, assembly, accelerated test) and typical failures. He elaborated on two case studies – void and delamination.



Dr. Rajen Dias, Intel Corporation, discussed "Next Generation Analytical Tools for Package Failure Analysis" Advanced packaging solutions for high performance microprocessors involve use of multi-level interconnections, shrinking geometries and improved thermal

solutions. These trends together with the introduction of low k dielectrics and Cu metallization in next generation Si technologies and new package substrate materials has resulted in severe die/package thermal - mechanical mismatch concerns. Packaging solutions for non CPU applications such as memory, chip sets, networking and communication chips are driven by miniaturization, stacked die for increase in functionality and Pb free applications. Understanding the defect and intrinsic failure mechanisms during the development and certification of these new package technologies is becoming extremely difficult and time consuming using traditional approaches to failure analysis. In his presentation, Rajen focused on advancements in three nondestructive tools - Scanning SQUID microscopy for detecting shorts, 3D x-ray radiography / tomography for imaging various levels of interconnections and thermal imaging for fault isolation in thermal failures. In addition, he also discussed analytical tools such as Laser Spallation for understanding interfacial adhesion and Laser milling for package delayering and microsurgery.

## **Support IEEE CPMT Society** and Chapters

Participate in Seminars, Workshops, and Conferences by Organizing and Attending

Additional Information at www.cpmt.org

### High Density Microsystem Design and Packaging and Component Failure Analysis Conference (HDP'06)

Submitted by Yan Zhang
IEEE CPMT Student Chapter, Shanghai
Sino-Swedish Microsystem Integration Technology Center
Shanghai University

The 2006 Conference on High Density Microsystem Design and Packaging and Component Failure Analysis (HDP'06) has been successfully hold from June 27 to June 30, 2006 in Shanghai with the support of shanghai science and technology commission, Shanghai Government, and the hard work of the members of Sino-Swedish Microsystem Integration Technology Center (SMIT Center), Shanghai University.

The HDP'06 conference was sponsored by Institute of Electrical and Electronics Engineers Components, Packaging and Manufacture Technology Society (IEEE CPMT), and supported by IEEE, Ministry of Information Industry of the People's Republic of China, shanghai science and technology commission, Shanghai Government and Shanghai University with great assistance from companies and institutes. And the HDP'06 conference was undertaken by Sino-Swedish Microsystem Integration Technology Center, Shanghai University. We are very honoured to have the welcome speeches by Wu Yi, director of Comprehensive Department, Torch High-Tech Industry Development Center, Ministry of Science And Technology, P. R. China, Jijun Xing, director for Europe, Department of International Cooperation, Ministry of Science And Technology, P. R. China, Prof. William Chen, president of IEEE Components, Packaging and Manufacture Technology Society, Guoqing Fu, director of department of international collaboration, shanghai science and technology commission, Shanghai Government, Prof. Zhewei Zhou, Vice President of Shanghai University, and Mr Lars Andreasson, Consul General of the Consulate General of Sweden in Shanghai.

More than 130 experts and researches participated the HDP'06 conference, and they came from countries and districts such as U.S.A., U.K., France, Sweden, Japan, India, German, Malaysia, Singapore, Hongkong, Taiwai and so on, and there are more than 80 papers had been presented. Moreover, we are honoured to have outstanding peoples such as Prof. C.P. Wong, member of academy of engineers, USA, Fellow of the IEEE, Georgia Tech, USA Prof. James E. Morris, Maseeh College of Engineering and Computer Science, Portland State University, USA, Dr. Tim Chen, vice general manager of Henkel Huawei Electronics Ltd, Dr. Dongkai Shangguan, Senior Director of Flextronics U.S.A., Ricky Lee, ASEM Fellow, Hong Kong University of Science and Technology as well as well-known industries like Intel, Kingston, Huawei Technologies co., Ltd., 3M, ASE Inc., Mitsubishi, Lucent Technologies, and universities as Shanghai University, Shanghai Jiaotong University, Huazhong University of Science and Technology, Central South University, Dalian University of Technology, Harbin Institute of Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy Science.

The HDP'06 conference provides a convenient way for the microelectronics and microsystem industries to be informed of the latest development and services as an information platform

of improving innovation capability in science and technology for microelectronics industries, Shanghai.



Conference Opening Ceremony Left to Right: Johan, Jian Hao, Jijun Xing, Yi Wu, Guoqing Fu, William Chen, and Lars Andreasson



Dr. James E. Morris, Portland State University, USA



Mahesh G. Varadarajan, Indian Institute of Science, India



Satoshi Okamoto Sumitomo Chemical Co. Ltd., Japan



Cristina Andersson, Chalmers University of Technology, Sweden



iNEMI 2007 Roadmap study workshop





Conference Welcome Banquet



Best Student Paper Award Presented to Cong-qian Cheng of Dalian University of Technology by CPMT President William Chen accompanied by Daoqiang Daniel Lu, Award Committee chair.





Cocktail Party at Consulate General of Sweden, Shanghai



IEEE CPMT Outstanding Young Engineer Award Presented to Teck-Joo Goh of Intel Corporation by CPMT President William Chen.



Conference Participants on their way to Intel Corporation



Dr. Xu, R & D director of Intel Corporation speaking to tour participants



More then 40 participants for Industry Visit to Intel, Shanghai

Thanks to All Contributors of Articles to the IEEE CPMT Society Newsletter, September, 2006, Issue ..... Editorial Staff





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IEEE CPMT Society Newsletter Send inputs, suggestions, and articles by email to <a href="mailto:nsltr-input@cpmt.org">nsltr-input@cpmt.org</a>

..... Editor

CHASE PALMER, 200







## Institute of Electrical and Electronics Engineers, Inc. Phoenix Section

Components, Packaging and Manufacturing Technology Society Chapter

&

Waves and Devices Chapter
PRESENT AN ALL-DAY WORKSHOP ON

## **Convergence in Communication and Computing**

Date: Friday, November 17<sup>th</sup>, 2006 Time: 7:00 A.M. – 5:00 P.M.

Location: Arizona State University, Tempe, Arizona – ASU Memorial Union (Arizona Room)

### **TOPICS**

Vision – A View of the Future of Convergence Market – Current Status and Future Trends Communication Technology Options and Standards Packaging – Mobile Products and Infrastructure Business Model System and Architecture Antenna / Propagation System Integration

Device Technology – RF, Microwave, Analog, and Base Band / Graphic Processing Panel discussion on the Future of Convergence in Communications

For Additional Information Access http://www.ieee.org/phoenix

### 31st International

### Electronics Manufacturing Technology Symposium (IEMT 2006) 8-10 November 2006 Petaling Jaya, Kuala Lumpur, MALAYSIA

The 31st IEMT is an international event organized by the IEEE CPMT Malaysia Chapter with co-sponsorship from the CPMT Society of IEEE and the Santa Clara Valley CPMT Chapter, featuring short courses, 3 parallel tracks of technical sessions, and exhibitions. It provides good coverage of technological developments in all areas of electronics packaging, from design to manufacturing and operation.

### **Professional Development Courses:**

Emerging Technology In IC Packaging
 Thermal
 Test Methods for Integrated Circuits
 Wafer Dicing
 Technology
 Design, Materials, Process and Reliability of Pb-Free Packaging and Assembly

### Tabletop Exhibits space still available!

Contact Mr. Eric Ng, eric.ng@st.com

### **Keynote Speakers and Instructors**

- Dr Rolf Aschenbrenner Dr Carlo Cognetti
- Dr Annette Teng Cheung Bernie Siegal
- Charles Vath Kin Gan Dr John Lau
- Yee Eh Horng Dr. Dongkai Shangguan

**IEEE Member fee:** RM720 (approx US\$200)

Visit our website for more information:

www.ieee.org.my/iemt2006



# 2006 Electrical Design of Advanced Packaging and Systems EDAPS-2006

17<sup>th</sup> and 18<sup>th</sup>, Dec. 2006 Shanghai, China



### **Final ANNOUNCEMENT**

The international workshop of EDAPS-2006 will be held in Shanghai, China, on Dec.17-18, 2006. This workshop is the fifth EDAPS in its series, organized this year by the Center for Microwave and RF Technologies of Shanghai Jiao Tong University and National Key Laboratory of EMC of China, technically sponsored by IEEE CPMT Subcommittee on Electrical Design, Modeling and Simulation (EDMS)

**Objective** The EDAPS-2006 International Workshop is to enhance the technical awareness in the Asia region specifically in the area of package and on-chip system electrical design concepts with focus pm issues and challenges ahead for next generation electronic products.

### **International Advisory Committee**

Alina Deutsch: IBM Corp., USA (Co-Chair, EDMS)

Andreas Cangellaris: Univ. of Illinois, USA

Andreas Weisshaar : Oregon State Univ., USA

Ching Chao Huang : Rambus, USA

F. G. Canavero : Univ. of Torino, Italy

James Libous : IBM Corporation, USA

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Madhavan Swaminathan: Georgia Tech., USA (Co-Chair, EDMS)

Ravi Kaw : Agilent Technologies, USA

Robert Jackson : Univ. of Massachusetts, USA

Tawfik Arabi : Intel Corp., USA

Joungho Kim : KAIST, Korea (Co-Chair)

T. Sudo : Toshiba Company, Japan (Co-Chair) E. P. Li : IHPC, Singapore (Co-Chair)

Topics Computer-Aided Design Issues for SoC and SiP/ SoP Modeling and Design EM and Thermal Modeling for SoC and SiP/SoP Electrical Design and Modeling, with Experimental Verification Field-Circuit Interactions and Simulations Interconnect Modeling, Design, and Testing for System-on-Chip (SoC) Mixed Technology Modules Nanotube and Nanowire Interconnects Optical Approaches to Packaging On-Chip High-Power and Ultra-Wideband EMC and EMI Power Delivery and Low Power Consumption Package Reliability System-in-Packaging (SIP) Testing Strategies and Techniques RF, Microwave, Millimeter-Wave and Light Wave Circuit Packages Signal Integrity Specific Implementation of Thermal Management to Advanced High-Power Packages Wireless Interconnects

Speakers The speakers consist of experts in the system integration field from around the world

Technically sponsored by IEEE CPMT Subcommittee on Electrical Design, Modeling and Simulation (EDMS)

### **Contact Details**





### IEEE/CPMT 8th International Conference on

### **Electronics Materials and Packaging**

Hong Kong Univ of Science and Technology (HKUST), Hong Kong, December 11-14, 2006

The EMAP conference includes all fundamental and applied science and technology related to the fields of electronic materials, devices, and packaging. Its purpose is to promote awareness of new advances in materials, design and simulations, fabrication, reliability, and thermal management of microsystem/MEMS packages. Also, the technical program will include invited and contributed presentations on theoretical, numerical, and experimental work of electronic materials and packaging. Technical workshops and industrial visit will also be arranged.

Short Courses: Lead-Free Soldering – Materials, Processes, Troubleshooting, and Reliability, Ning Cheng Lee; and 3D Integration Technologies – An Overview, Rajen Chanchani

Keynote Lectures: **Electromigration in Flip Chip Solder Joints**, King Ning Tu; and **Enabling Electronic Prognostics**, Michael Pecht

### **Sessions and Papers address these Topical Areas:**

- Materials and Processing
- Passive and Active Components
- Optoelectronics / Photonics
- Sensor, Actuator, and Transducer Technologies
- Advanced Packaging
- Emerging Packaging Technologies
- Interconnection Technologies
- System-in-Package (SiP) and 3D Stacked Die Packaging
- Thermal-Mechanical Modeling and Characterization
- Packaging Technologies for High Brightness LEDs
- Quality and Reliability

For more details, and the **Advance Program**, visit our website:

### www.ust.hk/emap2006

Coordinate international travel plans to attend one or two other CPMT Society events: **EPTC'06**, 6-8 December, 2006, in Singapore; and **VLSI Chip Packaging Workshop**, Dec. 4 - 5, 2006, Kyoto, Japan.



Conference on

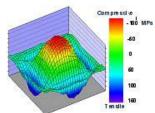
Thermal, Mechanical and Multiphysics Simulation and Experiments in Micro-Electronics and Micro-Systems

### London, England April 15-18, 2007

EuroSimE will address the results of both fundamental research and industrial application for thermal, mechanical and multiphysics solutions of (micro)-electronics and Microsystems, focusing on advanced simulation and experiments. The conference will include keynote presentations and sessions with a wide range of topics including, but not limited to:

- Mechanical simulation (static & dynamic)
- Thermo-mechanical simulation
- Thermal simulation (steady state & transient)
- Failure analysis and failure mode extraction
- Validation of simulations by experiments
- Integrated process modelling
- Advanced numerical and analytical simulation methodologies and tools
- Behavioural modelling
- Simulation-based optimisation, virtual prototyping in product and/or process design

### **CALL FOR PAPERS**



Components and packaging (flip-chip, BGA, CSP, Wafer-Level packages, MCM, Cu/low-k packages, fluidic components)

- Opto-electronic packages
- High temperature packaging
- Piezoelectric components
- Packaging for harsh environments
- "More than Moore" applications, such as various SiP, Microsystems, MEMS, sensors actuators, and MOEMS
- Wafer processing, chip design and reliability
- Nanoelectronics
- PWB design ad application
- Electronics system assembly

Abstracts due **October 30, 2006** For the full Call for Papers, visit:

### www.eurosime.org

Sponsored by the CPMT Society

## International Microsystems, Packaging, Assembly Conference Taiwan (IMPACT 2006)

October 18-20, 2006 Grand Formosa Regent Hotel Taipei, Taiwan Conference Website: impact.itri.org.tw/

In line with its very strong IC foundry industry, Taiwan has also developed into a pivotal position in the world's IC packaging arena. With the number one packaging revenue generated and a promising MEMS industry sprouting, the International Microsystems, Packaging, Assembly Conference Taiwan (IMPACT), organized by the Industrial Technology Research Institute (ITRI), will be held on October 18-20, 2006 in Taiwan. The purpose of the Conference is to bring together scientists and engineers actively engaged in research and development on Microsystems as well as semiconductor packaging and assembly to discuss current progress in the field.

### **Keynote Speakers**

Dr. Rolf Aschenbrenner, FhG-IZM, Germany Topic: Innovative Substrate Technologies for New Products

Dr. Avram Bar Cohen, University of Maryland, U.S.A. Topic: Thermal Packaging Challenges and Opportunities at the Micro and Nano Scales

Dr. Masayoshi Esashi, Tohoku University, Japan Topic: **MEMS for Practical Applications with Attention to Packaging** 

Dr. Douglas C.H. Yu., TSMC, Taiwan Topic: **The 3rd dimension—More Life for Moore's Law** 

Time	October 18,		Oct	ober 19,	October 20,	
	Wednesday		Th	ursday	Friday	
	Ballroom A	Ballroom B	Ballroom A	Ballroom B		
08:30	Opening		Session III -	Session IV	Technical	
	Plenary Session		Assembly &	Industrial Ses-	Tour	
12:20	<b>Keynote Speeches</b>		Manufacturing	sion (ASE)		
12:30	Lunch					
	Ballroom A	Ballroom B	Ballroom A	Ballroom B		
13:30	Session I	Session II	Session V	Session VI		
	Advanced	Microsystems	Model, Simula-	Materials, Proc-		
17:35	Packaging	Integration	tion & Design	ess & Equipment		
	Technology					
18:30						
	Cocktail Reception					
20:30		-				

**Easy on-line registration**. The registration form, in either English or Chinese, may also be downloaded. Special discount for IEEE members.

visit impact.itri.org.tw/

Requests for information about the Symposia should be directed to:

Emily Shen Conference Secretariat 195, Sec. 4, Chung Hsing Road Chutung, Hsinchu, Taiwan Tel: +886-3-591 2029

Fax: +886-3-582 0221 E-mail: impact@itri.org.tw



### **Call for Papers**

### **57th Electronic Components and Technology Conference**

Reno, Nevada, USA May 29 - June 1, 2007

The Electronic Components and Technology Conference is the premier international electronics symposium that brings together the best in packaging, components and microelectronic systems science, technology and education in an environment of cooperation and technical exchange. The ECTC is jointly sponsored by the Components, Packaging and Manufacturing Technology Society of the IEEE and the Electronic Components, Assemblies and Materials Association of the EIA. You are invited to submit abstracts that provide non-commercial information on new developments, technology and knowledge in the following areas:

**Advanced Packaging:** New packaging technologies, systems packaging, density and cooling for single chip, multichip, wafer-level, MEMS and power packages. Special emphasis on flip-chip, fine pitch and high lead count packaging in CSP, BGA, CGA, LGA and SMT packages for both Pbbased and Pb-free bumps and package assembly.

**Components & RF:** New passive or active component technologies, integrated/embedded components, RF and wireless component applications, modules with subsystem functionality, component performance and reliability.

**Emerging Technologies:** All design, fabrication, modeling, and performance aspects of materials, devices, systems, and packaging in the areas of nanoelectronics, bioelectronics, and organic / printable electronics.

**Interconnections:** First-level electronic interconnection technologies including: flip-chip, lead-free interconnect, novel interconnection structures and processes, wirebonding, conductive polymers for interconnect, wafer level interconnect, interconnections for 3D stacking (SIP/SOP), interconnection for new Silicon technologies (e.g. low-k), electromigration of bumped interconnects.

Manufacturing Technology: Advanced process development and equipment improvement for wafer thinning, bumping, stacking; low-k chip and sensor packaging; high-density interconnect and embedded component substrates; testing and burn-in. Cost, yield, performance and environmental improvements, process characterization, design for flexible manufacturing.

Materials & Processing: Processes for IC Packaging that enhance performance (mechanical, thermal and electrical) and cost effectiveness, including new technologies, development and application of adhesives, encapsulants, chip underfills, solders and alloys, thermal interface materials, dielectrics, thin films, nano materials to bonding, plating and other assembly processes.

**Modeling & Simulation:** Electrical, thermal, optical, mechanical modeling, simulation, characterization and packaging solutions including system-level applications.

**Optoelectronics:** Packaging for fiber-optic modules, optical devices and components including optical amplifiers, lasers, detectors, OEICs, and passive components, nonhermetic and plastic optical packages, optoelectronic package manufacturing and materials, solid state lighting (LED's and display arrays), optical data interconnects, WDMs, and optical back-planes.

**Poster Session:** Papers may be submitted on any of the major topics listed by the subcommittees. Presentation of papers format is highly encouraged at ECTC.

**Quality & Reliability:** Reliability testing and data analysis; failure analysis of field and test failures; reliability modeling of accelerated testing; reliability issues in emerging technologies; interconnect reliability physics, testing and predictive simulation.

You are invited to submit a 750-word abstract that describes the scope, content, and key points of your proposed paper via the website.

Abstracts must be received by 30 October, 2006.

For information, contact Rao Bonda

Freescale Semiconductor,

Phone: +1-480-413-6121 Email: rao.bonda@freescale.com

www.ectc.net









### CALL FOR PAPERS

# IEEE Polytronic 2007 Conference on Polymers and Adhesives in Microelectronics and Photonics

Miraikan - Odaiba, Tokyo, Japan

January 16-18, 2007

Polytronic 2007 will be held at the Miraikan Hall of the 'National Museum of Emerging Science and Innovation', in Odaiba-Tokyo, Japan. The conference provides experts from polymer developers and electronics manufacuturers with a unique opportunity for sharing ideas, and learning the fundamentals for R&D of polymer and adhesive materials, and polymer electronic packaging. We focus especially on new applications of polymers in electronics such as:

- Conductive Nano-Pastes
   Ink-jet Technologies
- Organic Displays and e-papers
- Organic Semiconductors, Polymer Battery, and Lowcost Processes
- Integration in Non-silicon MEMS

During the conference, Japan's largest exhibition "IN-TERNEPCON JAPAN" is also held from Jan. 17-19 at the same place, featuring materials, equipment and technology for electronics manufacuturing, SMT, and packaging, and hopefully may interest you to visit during the conference.

Sessions and papers cover the following areas:

Polymer and Adhesive Materials: Thermoseting, isotropic/anisotropic/thermal conductive adhesives; underfills Processing and Manufacturing: lamination; printing. transfer techniques; underfilling; curing; equipment.

Low temperatur eprocesses: laminates, bonding, process for non-silicon MEMS.

Reliability and Testing: Degradation; adhesion; hermeticity; accelerated testing; nondestructive testing methods.

Functional Polymers for Microelectronics: Conductivity of polymers; electronic transport; polymeric materials for molecular electronics; polymer-inorganic materials interface.

Applications: Polymer electronic devices; polymer optical fibers; organic displays; polymer batteries; substrates.

Environmental Issues: Ecology and toxicology; life cycle analyses.

Visit the website for the full program:

www.polytronic.jp

### **ThETA Conference** – Cairo – Egypt – Jan 3-6 - 2007

# $\theta_1$

### International Conference on Thermal Issues in Emerging Technologies – Theory and Applications

Objectives: Emerging Technologies in various domains, including Microelectronics, Nanotechnology, Smart Materials, Micro-Electro-Mechanical Systems, Biomedical engineering as well as New Energies, all raise many issues related to thermal effects. The importance of such effects is continuously increasing to a point where they become a dominant factor in determining the performance of such technologies. This is the first event in a series of conferences dedicated to these issues, gathering scientific and industrial communities to exchange experiences, orient research and create cooperation opportunities.

For the Advance Program and registration information, visit

www.thetaconf.org

Sessions and Papers are covering these topics:

- Thermal modeling of electronic systems
- Temperature aware computer systems design
- Cooling of electronic systems and data centers
- Micro and nano-scale heat transfer
- Modeling of multiple scale heat transfer problems
- Compact thermal models
- Thermo-mechanical analysis in electronic systems
  - MEMS multi-physics problems
- Computational methods in heat transfer
  - Energy conservation
  - Fuel cells
    - Solid state energy generation / cooling
  - Multiphase flow with heat transfer
  - Thermal issues in biomedical engineering
  - Thermal issues in micro-fabrication technology
- Thermal issues in new materials
  - New experimental methods in heat transfer



### Announcement and 1st Call for Papers

Theme:

### **Emerging Technologies for Electronics Packaging**

The International Spring Seminar on Electronics Technology is the premier European forum for the exchange of information between young scientists from academic communities and electronic industries from around the world on topics related to their experimental and theoretical work in the very wide-spread field of microelectronics technology and electronics packaging.

Based on a unique combination of oral and poster presentations, as well as individual meetings, senior and junior researchers can come together to discuss scientific problems and organize international cooperation and student exchanges in a convenient atmosphere during three conference days. It is our pleasure to encourage you to participate in ISSE 2007.

Submission of abstracts: By February 16th, 2007

### TOPICS OF INTEREST

- Nanotechnology, nanomaterials and nanoelectronics;
- Advanced packaging, new packages and materials, optoelectronics, optical interconnection technology, bio-compatible electronics packaging;
- Innovative applications of electronics technology;
- Reliability physics: analysis, life time-prediction in electronics;
- Quality management: total quality management, statistical process control, design of experiments, quality function deployment;
- Non-destructive testing, picture acquisition methods;
- System on chip, system in package;
- Manufacturing processes, process simulation and optimization;
- Innovations in PCBs, thin film and thick film techniques;
- Education and information technology in electronics technology, system modeling, CAD/CAE in packaging;
- Environmental, ecology, and toxicology issues in electronics technology

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