Components, Packaging, and Manufacturing Technology Society Newsletter

IEEE

THE GLOBAL SOCIETY FOR MICROELECTRONICS SYSTEMS PACKAGING

VOL. 34 NO. 1, SUMMER 2011, ISSN 1077-2999 www.cpmt.org www.ewh.ieee.org/soc/cpmt/newsletter

President's Column....

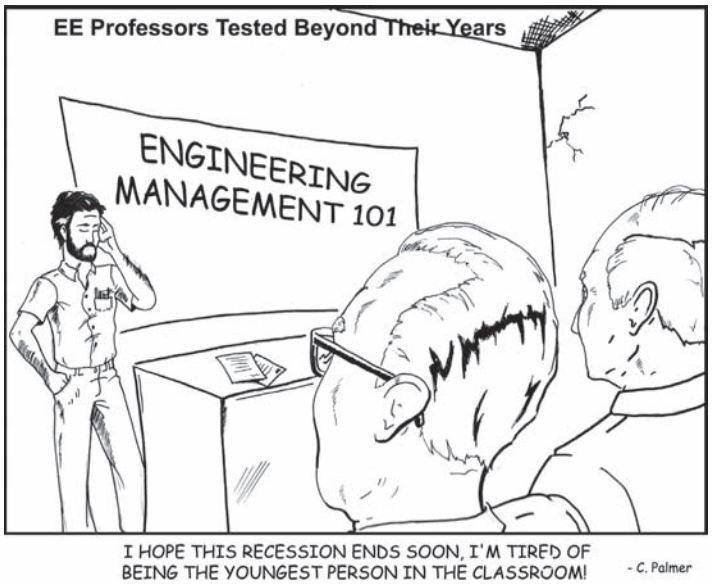
Rolf Aschenbrenner
President, IEEE CPMT Society
Fraunhofer-Institut, Berlin, Germany
rolf.aschenbrenner@izm.fraunhofer.de

This year is turning out well both for the world economy, which continues its climb out of the global recession, and for CPMT. After watching our membership numbers halve over ten years from the beginning of the new millennium, we are finally starting to reverse the trend. The first indication that the situation was turning around was last October, when we saw that membership had increased by 9% compared to the previous year. Since then, the trend has continued and can largely be attributed to our strong public relations and networking efforts at conferences over the past years. Rest assured that we will be maintaining our commitment to this recruitment drive, as a healthy and thriving association is central to furthering our profession and its activities as a whole.

ECTC 2011 has just concluded. This special highlight in CPMT's annual calendar of conferences was held at Lake Buena Vista in Florida, which was colorful and entertaining conference site. The technical program included 32 sessions on hot topics in our industry and an extensive set of professional development courses. The program offered something for everyone, and no one left without some new insights and inspiration to carry them through the following twelve months.

As in every year, we presented the CPMT Awards to young and older, but no less enthusiastic, outstanding researchers. The awards ceremony celebrated talent and hard work–key in any industry, but particularly in ours, which progresses at such a fast pace and whose developments have such a

(continued on page 3)



NEWSLETTER SUBMISSION DEADLINES:

1 August 2011
1 November 2011
1 February 2012
1 May 2012

Submit all material to nsltr-input@cpmt.org

CPMT Officers

President:	Rolf Aschenbrenner	Rolf.Aschenbrenner@izm.fraunhofer.de
VP (Technical):	N. Rao Bonda	r.bonda@ieee.org
VP (Conferences):	Jie Xue	jixue@cisco.com
VP (Publications):	R. Wayne Johnson	johnsr7@auburn.edu
VP (Education):	Kitty Pearsall	kittyp@us.ibm.com
VP (Finance):	Thomas G. Reynolds III	t.reynolds@ieee.org
Sr. Past Pres.:	Phil Garrou	pgarrou/Contractor@rti.org
Jr. Past Pres.:	William T. Chen	William.Chen@ASEUS.COM
Executive Director:	Marsha Tickman	m.tickman@ieee.org

Elected Board Members

2011: Vasudeva Atluri, Koneru Ramakrishna, Patrick Thompson, Paul Wesling, Klaus-Jurgen Wolter, and Kishio Yokkouchi

2012: Chris Bailey, Daniel Donahoe, Paul D. Franzon, S-W (Ricky) Lee, Kwang-Lung Lin, and Leonard W. Schaper

2013: Debendra Mallik, Toni Mattila, James E. Morris, Eric Perfecto, Dongkai Shangguan, Jean Trewhella

CPMT Society Newsletter

Editor-in-Chief: Kitty Pearsall kittyp@us.ibm.com

CPMT Archival Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:
R. Wayne Johnson
Co-Editor, Advanced Packaging:
Ravi Mahajan
Co-Editor, Electrical Performance:
José E. Schutt-Ainé
Co-Editor, Components: Characterization and Modeling:
Koneru Ramakrishna
Co-Editor, Packaging Technologies:
Kuo-Ning Chiang
Co-Editor, Electronics Manufacturing:
R. Wayne Johnson

Technical Committee Chairs

TC-Assy - IC and Package Assembly:
Martin Goetz
TC-ASTR - Environmental Stress & Reliability Test:
John E. Proulx
TC-ECCC - Electrical Contacts, Connectors and Cables:
Jerry Witter
TC-Ed - Education:
Rao R. Tummala
TC-EDMS - Electrical Design, Modeling and Simulation:
Madhavan Swaminathan
TC-EM - Manufacturing - Design & Process:
Vacant
TC-GEMP - Green Electronics Manufacturing and Packaging:
Nils F. Nissen
TC-HDSB - High Density PWB Packaging:
Yoshitaka Fukuoka
TC-M - Materials:
Rajen Chanchani
TC-MEMS - MEMS and Sensor Packaging:
Eric Jung
TC-NANO - Nano Packaging:
Rao Tummala
TC-OPTO - Fiber Optics & Photonics:
Vacant
TC-PEP - Power Electronics Packaging:
Douglas Hopkins
TC-RF+W - RF and Wireless:
Craig A. Gaw
TC-SP - Systems Packaging:
Cian O Mathuna
TC-Test - Electrical Test:
Bruce Kim
TC-Therm - Thermal Management & Thermomech. Design:
Tony Mak
TC-WLP - Wafer Level Packaging:
Michael Toepper

Strategic Program Directors

Awards and Recognition: Patrick Thompson, patrick.thompson@ti.com
Conferences: Jie Xue, jixue@cisco.com
Educational Programs: Kitty Pearsall, kittyp@us.ibm.com
Global Chapters and Membership: Eric Perfecto, perfecto@us.ibm.com
Publications: R. Wayne Johnson, johnsr7@auburn.edu
Student Programs: Chris Bailey, Chris Bailey, C.Bailey@gre.ac.uk
Technical Programs: N.Rao Bonda, r.bonda@ieee.org
Region 8 Programs: Eric Beyne Beyne@imec.be
Region 10 Programs: Charles Lee, charles.lee@ieee.org

Standing Committee Chairs

Awards: Patrick Thompson, patrick.thompson@ti.com
Chapter Development: Eric Perfecto, perfecto@us.ibm.com
Constitution and Bylaws: Tony Mak, t.mak@ieee.org
Distinguished Lecturers: Kitty Pearsall, kittyp@us.ibm.com
Educational Activities: Vacant
Fellows Evaluation: CP Wong, cp.wong@ieee.org
Fellows Search: Rao Tummala, rao.tummala@ee.gatech.edu
Finance: William Chen, william.chen@aseus.com
Long Range / Strategic Planning: Philip E. Garrou, pgarrou/Contractor@rti.org
Membership: Eric Perfecto, perfecto@us.ibm.com
Nominations: William Chen, william.chen@aseus.com

Distinguished Lecturers

Program Director: Kitty Pearsall, kittyp@us.ibm.com
Lecturers: Albert F. Puttlitz, Ph.D., Avram Bar-Cohen, Ph.D., H. Anthony Chan, Ph.D., Rajen Chanchani, Ph.D., William T. Chen, Ph.D., Badih El-Kareh, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., George G. Harman, Ph.D., R. Wayne Johnson, Ph.D., George A. Katopis, Ph.D., Jorma Kalevi Kivilahti, D.Sc., John H. Lau, Ph.D., Michael Lebby, Ph.D, Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., T. Paul Parker, Michael Pecht, Ph.D., Karl J. Puttlitz, Ph.D., Bahgat Sammakia, Ph.D., Dongkai Shangguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Yong-Khim Swee, Yutaka Tsukada, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Ralph W. Wyndrum Jr., Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branches

Refer to www.cpmt.org for CPMT Society Chapters and Student Branches list

IEEE Components, Packaging, and Manufacturing Technology Society Newsletter is published quarterly by the Components, Packaging, and Manufacturing Technology Society of the Institute of Electrical and Electronics Engineers, Inc. Headquarters: 3 Park Avenue, 17th Floor, New York, NY 10016-5997. US$1.00 per member per year is included in Society fee for each member of the Components, Packaging, and Manufacturing Technology Society. Printed in U.S.A. Periodicals postage paid at New York, NY, and at additional mailing offices. Postmaster: Send address changes to IEEE CPMT Newsletter, IEEE 445 Hoes Lane, Piscataway, NJ 08854.

Circulate your printed or PDF copy of this NEWSLETTER to co-workers.

IEEE prohibits discrimination, harassment, and bullying. For more information, visit http://www.ieee.org/web/aboutus/whatis/policies/p9-26.html.

CPMT Members-Only Web
(www.cpmt.org/mem/)

Username: nano
Password: packaging

profound effect on day-to-day life, generally with little recognition of the personalities responsible for the innovation. Details on the Awards and their recipients will be included in the next Newsletter.

If you were unable to attend the ECTC, please look for the conference papers on IEEE Xplore (http://ieeexplore.ieee.org/Xplore/guesthome.jsp). I hope to see you at one of our many CPMT events throughout the year.

CPMT Society News....

IEEE Life Fellow Dimitry Grabbe Passes Away at 83

Recipient of 2007 IEEE Components, Packaging and Manufacturing Technology Award.

Dimitry Grabbe played an integral part in advancing U.S. space exploration. His pioneering work has produced nearly 500 U.S. and foreign patents covering machine design, semiconductor packaging, electronics assembly and optoelectronic connector design. His work in printed circuit board technology for electronic packaging led to the development of large, multi-layer printed circuit boards. This proved crucial in helping U.S. astronauts gain greater real-time control of their space-exploration activities.

In 1964, Mr. Grabbe founded the Maine Research Corporation which specialized in high-end printed circuit boards; the company was dissolved in 1972. He joined AMP, Inc. in 1973, and helped it become a world leader in electrical/electronic connector technology, test socket technology and miniature semiconductor packages.

An IEEE Life Fellow, Mr. Grabbe was also recognized by AMP (now part of Tyco Electronics) with a Lifetime Achievement Award, and by the American Society of Mechnical Engineers, which chose him for its Leonardo da Vinci Award.

In 2007, Mr. Grabbe was presented with the 2007 IEEE Components, Packaging and Manufacturing Technology Award for "For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

E-Mail Alias and IEEE Web Account Needed

2011 CPMT Society Board of Governors Election On-Line

In order to vote in this year's CPMT Board of Governors election, members will need to have a valid e-mail alias on record with IEEE and also have an IEEE Web Account.

Eligible voting members will receive notification by e-mail in the Fall of this year with instructions for voting on-line. You will need an IEEE Web Account to access the ballot and cast your vote. This Web Account is the same one you may use for IEEE services such as renewing membership and accessing IEEE Xplore.

If you do not recall your Web Account username and password, or aren't sure whether you have established an account, please go to http://www.ieee.org/web/accounts to recover your password or establish a new account.

Please be sure to update your IEEE membership record with you current e-mail alias. If you DO NOT HAVE AN E-MAIL address or would prefer to receive a paper ballot by mail, please send your name, mailing address and IEEE Member Number by 20 August to:

Marsha Tickman
IEEE CPMT Executive Office
445 Hoes Lane
Piscataway, NJ 08854 USA
m.tickman@ieee.org

CALL FOR CANDIDATES

CPMT SOCIETY BOARD OF GOVERNORS

The CPMT Society is governed by a Board of Governors composed of officers, 18 elected members-at-large, and various committee chairs and representatives (see inside cover of this Newsletter for details.)

Annually, Society members are asked to elect six members-at-large for a three-year term of office. Candidates for member-at-large are selected in two ways – either by the Society Nominating Committee, or by petition.

This year's election is the fourth in which members-at-large will be elected to achieve totals proportionate to the geographic distribution of CPMT members. Voting members will elect members-at-large from within their Region only (that is, members in Region 8 will vote for members-at-large from Region 8, etc.)

Elected Members of the Board of Governors must be willing to attend two annual Board meetings and participate actively in areas of their interest (publications, conferences, membership development, chapter development, etc.) The term of office for this election is 1 January 2012 through 31 December 2014.

If you are an IEEE and CPMT Society member in good standing and are interested in serving on the Board of Governors, you can become a candidate via petition by following the procedures below.

- Request establishment of electronic petition process, allowing signatures to be collected on-line.
  You must contact Marsha Tickman to implement electronic petition process.

OR

- Prepare a petition that contains your name, member number, and statement of your qualifications for office.
- Provide lines for signatories. Each line should include space for a printed name, member number, and signature.
- Have the petition signed by a MINIMUM of 50 CPMT Society members in good standing (Student grade members are not eligible to sign.)
- Submit your petition by mail no later than Friday, 15 July 2011 to:
  CPMT Society Nominations Committee
  c/o Marsha Tickman
  IEEE CPMT Society Executive Office
  445 Hoes Lane
  Piscataway, NJ 08854 USA

Membership status of all signatories will be validated. It is suggested that you gather more than 50 signatures in order to assure meeting the minimum required number of valid signatures.

If you have questions or need additional information, contact Marsha Tickman at the above address, by phone at 732-562-5529, or by e-mail at m.tickman@ieee.org.

New IEEE CPMT Senior Members

The members listed below were recently elevated to the grade of Senior Member.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

Ahmad, Ibrahim Bin
Chen, Zhuan-Ke
Maffucci, Antonio
Miftakhutdinov, Rais
Moore, Carl
Na, Nanju
Nakajima, Hirofumi
Nath, Jayesh
Oppert, Thomas
Poupon, Gilles
Scott, Steven
Smiley, Stephen
Swaminathan, Rajasekaran
Wong, Kenaz
Wong, Shaw Fong

Congratulations to IEEE CPMT Fellows Class of 2011

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Mark Allen
Georgia Institute of Technology, GA, USA
For contributions to micro and nanofabrication technologies for microelectromechanical systems

Simon Ang
The University of Arkansas, AR, USA
For contributions to education power electronics and microelectronics in packaging education

Debabani Choudhury
Intel Corporation, CA, USA
For contributions to millimeter wave enabling technologies

Kwang-Lung Lin
National Cheng Kung University, Tainan, Taiwan
For contributions to development of lead-free solder alloys and material interactions

Jianqiang Lu
Rensselaer Polytechnic Institute, NY, USA
For contributions to three-dimensional integrated circuit technology

Ioannis (John) Papapolymerou
Georgia Institute of Technology, GA, USA
For contributions to flexible, microwave and wireless components and systems

Robert Puers
Katholieke Universiteit Leuven, Belgium
For contributions to implantable microelectromechanical systems

Frank Shi
University of California, Irvine, CA, USA
For contributions to optoelectronic packaging technologies

Ganesh Subbarayan
Purdue University, IN, USA
For contributions to reliability and their associated computational techniques in mechanics

Jie Xue
Cisco Systems, Inc., CA, USA
For leadership in electronics packaging technology

CPMT Chapter News....

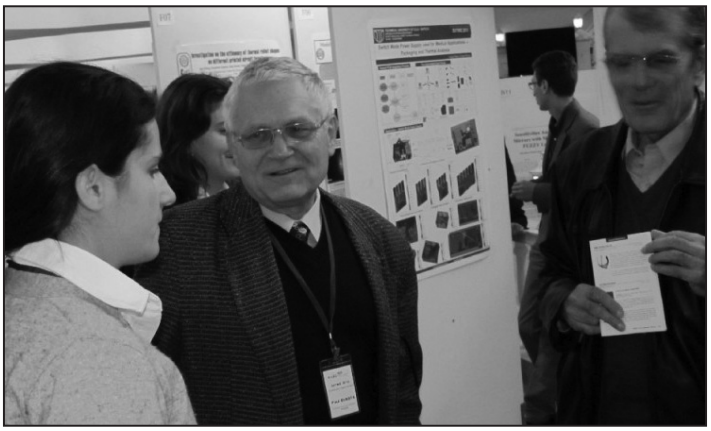
16th IEEE International Symposium for Design and Technology of Electronics Packages – SIITME 2010

submitted by Andreea Bonea, Press Officer of IEEE CPMT Student Branch Chapter of the Politehnica University of Bucharest, Romania

The 16th IEEE 2010 International Symposium for Design and Technology in Electronic Packaging (www.siitme.ro) is a premier Central European event in the field of electronics industry; SIITME event is technically sponsored and organized by IEEE CPMT Society Hu&Ro Joint Chapter. Since its first edition in 1995 it represented a scientific forum for exchanging information between academia and industry from Central and Eastern Europe on the topics related to their experimental and theoretical work in the field of electronics and micro-systems, manufacturing technologies and advanced packaging.

The IEEE-CPMT Hu&Ro Joint Chapter is involved, through Prof. Pitică (Chair) and Prof. Illyefalvi-Vitez(Vice-Chair), in organizing this event as well as TIE, another long tradition event, taking place during spring.

The 16th Edition took place between 23–26 September 2010, on the foothills of the Carpathians on the Arges river valley, in the



Prof. Paul SVASTA (General Chair of SIITME), left, and Prof. Zsolt ILLYE-FALVI-VITEZ (Publication committee Chair), right, in a discussion with a young researcher during the poster evaluation session.

Prof. Dr. Ing. Karlheinz BOCK (Acting Director of Fraunhofer EMFT and Professor with TU Berlin), giving an insightful presentation on "Organic Large Area Electronics and Hetero-System Integration".

city of Pitesti. Like in the previous years the conference covers a variety of topics related to packaging for modeling and simulation, in terms of assembly and manufacturing technology, Microsystems, communications and power electronics. The stress also falls on emerging technologies and education as these new fields are the basis for the state-of-the-art research of tomorrow, as lifelong learning is particularly relevant to the member states of the European Union in accordance to the global tendency.

This year various members of Academia, young scientists and students attended from Germany, Italy, France, Morocco, Bulgaria, Czech Republic, Hungary and Romania. The Romanian participants came from all over the country, representing the technical universities from Cluj-Napoca, Pitesti, Suceava, Timisoara, Galati, Sibiu, Alba Iulia, Iasi, Brasov and Bucharest.

During the first day of the Symposium included several workshops. The "E-Training Microsystems Technologies" was intended to demonstrate the importance of Microsystems e-training in the frame of electronics industry, making use of e-learning platforms destined to vocational education, training of SMEs specialists, students and other potential users(engineers, physicists, etc.) looking for additional training for employment. The topics included the basics of Microsystems technologies, fundamental aspects on thermal management at Microsystems level, and engineering aspects of photo masks data preparation.

Also a workshop on nuclear electronics and another on transmission line animations were held. The latter went through aspects of high-speed electronic applications taking into account the effects of the transmission line propagation equations. Animated results of the phenomena defined by the equations were presented using MATLAB.

The second day of the conference started with the presentations given by the keynote speakers, followed by the oral and poster sessions. During the poster presentations one would first deliver a short 5-slider presentation, which has the role of drawing the attention to the poster presented afterwards in more detail. This structure was used because it verifies the author's synthesis capacity.

Then, Prof. Dr. Ing. Karlheinz BOCK, Professor at TU Berlin, Acting Director of Fraunhofer EMFT, and Department Head of Polytronic and multi-functional Systems at the Fraunhofer Research Institution for Modular Solid State Technologies EMFT, gave a very attractive and attention-grabbing talk on "OLAE (Organic Large Area Electronics) and Hetero-System Integration".

Dr. Philippe MOREY-CHAISEMARTIN, from Institut National Polytechnique de Grenoble, CIME Nanotech also delivered an informational presentation on "Teaching microsystems in a moving industry environment".

The activities of the Joint Chapter were the organization of the conference, both in the scientific and in technical sense, which has lead to a high level conference and a pleasant atmosphere. Stages were lead by Prof. Paul Svasta General Chair of SIITME,

The steering committee meeting of SIITME 2010.

Prof. Dan Pitica General-Co Chair of SIITME, Prof. Ioan LIŢĂ Conference Chair, Prof Vlad CEHAN Scientific Chair, Prof. Zsolt ILLYEFALVI-VITEZ Publication Committee Chair and Dr. Heinz WOHLRABE Poster Committee General Chair.

SIITME 2010 also was an IEEE Conference, registered in the conference database. After the final evaluation, the papers of the highest scientific value are included in the IEEE Xplore database. The members of the Steering and the Scientific committees have work hard in helping the authors and evaluating their abstracts, papers and presentations in terms of originality, appropriateness to the Conference, technical strength and quality of the presentation.

At the closing ceremony, the best scientists were awarded: the Best Poster Award was given to Senior Researcher Ciprian Ionescu (UPBCETTI, Bucharest); the Best Oral Presentation was received by Senior Researcher Dan Tudor VUZA, Institutul de Matematica al Academiei Romane, Romania; Excellent oral presentation for young scientist awards were granted to Bogdan ALECSA, Universitatea Tehnică "Gheorghe Asachi" Iaşi, Reka BATORFI, Budapest Univ. of Technology and Economics, Maximilian NICOLAE, Universitatea "Politehnica" din Bucureşti, Attila GÉCZY, Budapest Univ. of Technology and Economics. Also, Excellent poster presentation was given to Senior Researcher Daniel VISAN, Universitatea din Piteşti, while the Best Poster presentation for young scientist went to Attila GÉCZY, Budapest Univ. of Technology and Economics. Last but not least the excellent poster presentation for young scientist was received by Radu ETZ, Technical University of Cluj-Napoca and Catalin NEGREA, Universitatea "Politehnica" din Timisoara. SIITME encourages the participation of young researchers, which is why several awards are intended especially for them

The awarding ceremony of SIITME 2010 for Excellent Oral Presentation for Young Scientist.

During the cultural program of the conference, the organizers made their best efforts to give an insight into the local specialties during the wine tasting session and to present some of the surrounding sites including the historical monument "Curtea de Arges" monastery, founded in 1512, and the impressing "Vidraru" dam. The program presented a good opportunity for networking which forecasts future scientific and social relationships.

We are eagerly anticipating the next edition of the conference, SIITME 2011, which will be held in Timişoara, România, 20–23 October 2011.

Interconnection Techniques in Electronics (TIE) Event – International Student Professional Contest 20th Edition

submitted by Cristina Marghescu, IEEE CPMT Student Branch Chapter of the Politehnica University of Bucharest, Romania cristina.marghescu@cetti.ro

Between the 13th and the 16th of April the 20th Interconnection Techniques in Electronics (TIE – www.tie.ro) Event took place in Bucharest. The main organizer was "Politehnica" University of Bucharest, Faculty of Electronics, Telecommunications and Information Technology (with the technical help of Prof. Paul Schiopu, Ph.D.), with the support of the IEEE-CPMT Hu&Ro Joint Chapter (Chair Professor Dan Pitica) and of the IEEE-CPMT Student Branch Chapter of the "Politehnica" University of Bucharest, Romania (Advisor Professor Paul Svasta).

This was an anniversary edition, the 20th, an opportunity to look back: an event that started as a local contest grew to become first a national and then an international event (the Budapest University of Technology and Economics, coordinator Prof. Zsolt Illyefalvi-Vitez, is a participant since the 2009 edition).

The event comprised one day of workshops and two competition days. The workshops consisted in lectures given by professionals from companies in the field (Eng. Mircea Slanina from Mentor Graphics, Marian Vladescu Ph.D. from Cadence, Corné Hoppenbrouwers, Ralph Christ, and László Rédey from Cookson Electronics Assembly Materials). There was also an interactive presentation from Continental Automotive Timisoara and Sibiu throughout the event.

The subjects were created by a team of professionals both from the academic field and from the industry (Technical Committee – Committee Manager Norocel Codreanu, Ph.D.). The project goal this year was to design and generate layout and fabrication files for the electronic system of a vehicle instrument cluster.

The contest was a 4 hour challenge. English has become the language used since the 2009 edition in Galati. The contestants were allowed to use their own computers with CAD software installed. They received the subjects in printed and digital form as well as the data sheets for the components used. A 15 minute period was given before the official start of the contest for studying the subjects.

The Industrial Advisor Committee, chaired by Cosmin Moisa, Continental Automotive Timisoara, participates in the writing of

Figure 1 – (left to right) Prof. Dan Pitica, IEEE-CPMT Hu&Ro Joint Chapter Chair, Technical University of Cluj-Napoca, Romania, Prof. Zsolt Illyefalvi-Vitez, IEEE-CPMT Hu&Ro Joint Chapter, Vice-chair, Budapest University of Technology and Economics, Hungary, and Prof. Paul Svasta, Advisor IEEE-CPMT Student Branch Chapter of "Politehnica" University of Bucharest, Romania with the Winner's Cups (one of the cups is given to the winner's university and is transmissible, the other goes to the winner).

Figure 2 – Brainstorming session of the technical committee for preparing the proposed subject for the 20th edition.

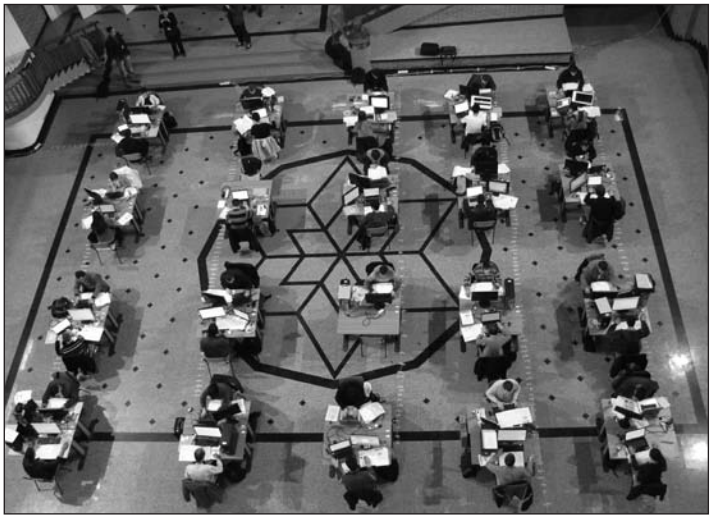


Figure 3 – Top view – the competition "arena".

Figure 4 –The evaluation process.

Figure 5 – TIE Awards Session. From left to right: Dorin Antonovici 2nd Prize Winner - "Stefan cel Mare" University of Suceava, Marius Rangu, Ph.D. - Representative of the "Politehnica" University of Timişoara, Calin Precup 1st Prize Winner - "Politehnica" University of Timişoara, Mares Mihai 3rd Prize Winner - University of Pitesti.

subjects as well as in the evaluation and sets the line above which are located the people with real knowledge in the field of PCB design, those students being recommended as PCB designers.

There is special emphasis on the problems that could appear in the manufacturing phase: distinct files for non-plated and plated holes, distinct files for board outline cut-out and inside cut-outs, generation of pick-and-place file for all SMT components.

At the final stage of the contest participated three students from Hungary and 35 students from 12 universities from Romania, students who had received top scores during the local phase of the competition.

The results are evaluated by mixed teams, from the academic as well as from the industry. An Evaluation Form where the points are clearly stated is used in order to assure the correctness of the

Figure 6 – Participants to the TIE event.

evaluations. The evaluation process can be followed by anyone who wishes to.

The first three ranked students received a scholarship. Other prizes were awarded by CAD software providers to high ranking students who used their software.

The first 12 competitors have received from the IAC (Industrial Advisor Committee) the "PCB Designer" degree, as recognition of their high level of knowledge in the field of CAD for development of electronic modules and assemblies.

The next edition of the TIE Event will be held in Sibiu (former European Capital of Culture for the year 2007 together with Luxemburg).

We wish the participants all the best until the next edition - Sibiu, Romania 26th–28th of April 2012!

IEEE Xplore® Table of Contents Alert

Any technologist – **member or non-member** – is welcome to receive alerts when upcoming issues of our CPMT *Transactions* are posted to the IEEE's Xplore database and all the papers are available for downloading. This is a handy way to scan the issue's Table of Contents and quickly learn about novel approaches to packaging, modeling, reliability, materials, assembly and other topics.

The website link is:ieeexplore.ieee.org/xpl/tocalerts_signup.jsp

If you already have an IEEE web account, you may sign in and select those journals you wish to track. If you don't have an account, all it takes is your name and email address! Then simply click the Alert Status box next to the journals you wish to monitor. You will receive an email each quarter when that journal is posted to Xplore.

Similarly, if you prefer to receive information by RSS feed, you may add our journals' feeds to your Reader. You'll get a listing of the papers in that issue, along with full abstracts and a link for downloading the paper. The RSS links are shown on this same web page.

Here are the journals we suggest you select for monitoring:

Transactions on Components, Packaging and Manufacturing Technology
Transactions on Semiconductor Manufacturing

Publication News....

CPMT Board of Governors Approves New Co-Editors-in-Chief for the IEEE Transactions on Components, Packaging and Manufacturing Technology

With the start of 2011, Ricky Lee, Co-Editor-in-Chief of the Transactions on Components and Packaging Technologies and Ganesh Subbarayan, Co-Editor-in-Chief of the Transactions on Advanced Packaging have completed their terms of office and have elected not to continue in these roles.

Professor Subbarayan has served as EiC for nine years, agreeing to serve his ninth year to assist with the transition to the merged Transactions. He is a Professor of Mechanical Engineering at Purdue University and Director of the Hierarchical Design and Characterization Lab (HiDAC).

Professor Lee has served as EiC for five years. He is a Professor of Mechanical Engineering at the Hong Kong University of Science and Technology and Director of the Center for Advanced Microsystems Packaging. He also serves as Director of the HKUST Shenzhen Electronic Materials & Packaging Laboratory.

For continuity Professor Subbarayan and Professor Lee will continue to manage the manuscripts that have been submitted during their tenure and are still in the review process. We thank Ricky and Ganesh for their leadership and commitment to this important role.

Dr. Ravi Mahajan and Professor Kuo-Ning Chiang have been selected as new Co-EiCs for the merged Transactions on Components, Packaging and Manufacturing Technology. They will join Co-EiC's Dr. Koneru (Rama) Ramakrishna, Professor Jose Schutt-Aine and Professor Wayne Johnson.

Dr. Mahajan is currently a Senior Principal Engineer in the Pathfinding Group in Intel's Assembly & Test Technology Development (ATTD) in Chandler, Arizona. He is responsible for developing packaging technology architectures to enable packaging and assembly processes for silicon nodes at 11nm and beyond. In his career at Intel he has been responsible for developing thermal solutions for a number of Pentium and Itanium class of products. He is also responsible for technical direction for Intel and consortia funded research in assembly and packaging. He is Intel's representative to the Scientific Technical Advisory Board and a past chair of the Science Area Advisory Committee for the Interconnect and Packaging Sciences thrust for the Semiconductor Research Corporation. He is also one of the founding editors for the Intel Assembly and Test Technology Journal an Intel internal journal that documents challenges and current progress in the area of Assembly & Packaging. He is a Fellow of the ASME, a Senior Member of IEEE and currently serves as an Associate Editor of the IEEE Transactions on Advanced Packaging (since 2001).

Professor Chiang has published more than 250 technical papers in international journals and conference proceedings (68 of them are listed in IEEE Explore) and he holds 31 Taiwan patents, 8 US patents, 1 Mainland China's patent and 1 Singapore patent. Professor Chiang has been an Associate Editor of the IEEE Transactions on Components and Packaging Technologies and the Transactions on Advanced Packaging, His vision and research performance drives to establish a "Design on Simulation (DOS)" based development procedure for advanced packaging products such as WLCSP and 3D packages, he is a well-known scholar in this research and application field. Professor Chiang has collaborated with many electronic packaging house, semiconductor and LED companies such as ACET, TSMC, UMC, EPISTAR (LED), VIA, etc.

We welcome Professor Chiang and Dr. Mahajan to the roles of Co-EiC's for the IEEE Transactions on Components, Packaging and Manufacturing Technology.

2010 CPMT Transactions Best Paper Awards

Each year, the Editors of the three CPMT Society Transactions select the best papers published in the prior year. The papers are selected from among nearly 300 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

The awards will be presented at the 61st Electronic Components and Technology Conference (ECTC).

Subscribers to these publications can access the papers on-line in IEEE Xplore at: http://ieeexplore.ieee.org/xpl/browsePopular.jsp. Members can add the subscriptions to their membership at: https://sbwsweb.ieee.org/ecustomercme_enu/start.swe?SWECmd=Login&SWECM=S&SWEHo=sbwsweb.ieee.org

TRANSACTIONS ON COMPONENTS AND PACKAGING TECHNOLOGIES, VOL. 33, NO. 1, MARCH 2010

"Development of 3-D Silicon Module With TSV for System in Packaging"

Navas Khan, Vempati Srinivasa Rao, Samuel Lim, Ho Soon We, Vincent Lee, Xiaowu Zhang, E. B. Liao, Ranganathan Nagarajan, T. C. Chai, V. Kripesh, and John H. Lau, *Fellow, IEEE;*

Abstract—Portable electronic products demand multifunctional module comprising of digital, radio frequency and memory functions. Through silicon via (TSV) technology provides a means

of implementing complex, multifunctional integration with a higher packing density for a system in package. A 3-D silicon module with TSV has been developed in this paper. Thermo-mechanical analysis has been performed and TSV interconnect design is optimized. Multiple chips representing different functional circuits are assembled using wirebond and flip chip interconnection methods. Silicon carrier is fabricated using via-first approach, the barrier copper via is exposed by the backgrinding process. A two-stack silicon module is developed and module fabrication details are given in this paper. The module reliability has been evaluated under temperature cycling (−40/125 °C) and drop test.

TRANSACTIONS ON ADVANCED PACKAGING, VOL. 33, NO. 3, AUGUST 2010

"Noise Coupling Mitigation in PWR/GND Plane Pair by Means of Photonic Crystal Fence: Sensitivity Analysis and Design Parameters Extraction"

Antonio Ciccomancini Scogna*, Senior Member, IEEE*, Tzong-Lin Wu*, Senior Member, IEEE*, and Antonio Orlandi*, Fellow, IEEE;*

Abstract—A photonic crystal fence is proposed for simultaneous switching noise mitigation in power/ground plane pairs with minimumuse of the high dielectric constant for the rods. In particular a 45 degree rotated square lattice consisting in three rows of periodic rows is used for the fence. Broadband and high efficient noise suppression can be still achieved while minimizing the cost of the structure. A sensitivity analysis investigating the impact of 1) the normalized rods radius, 2) the number of rods rows, and 3) the value of the dielectric rods is performed and design parameters for the calculation of the stop bands are extracted. The normalized radius is not sufficient to correctly predict the stop band of the fence; instead multiple design parameters are necessary. It is found that an extra row of high dielectric constant material introduces an attenuation for the noise coefficient of around 8–10 dB per row and multiple stop bands are predicted while increasing the relative dielectric constant of the rods from 50 to 300. A one-dimensional circuit model is finally developed for a quick and efficient prediction of the stop band performances of these structures.

TRANSACTIONS ON ELECTRONICS PACKAGING MANUFACTURING, VOL. 33, NO. 3, JULY 2010

"Correlation Between Whisker Initiation and Compressive Stress in Electrodeposited Tin–Copper Coating on Copper Leadframes"

Takahiko Kato*, Member, IEEE*, Haruo Akahoshi*, Member, IEEE*, Masato Nakamura, Takeshi Terasaki, Tomio Iwasaki, Tomoaki Hashimoto, and Asao Nishimura*, Member, IEEE;*

Abstract—To evaluate the contribution of coating stress to whisker initiation from IC package leads, the stress distribution in the coating was investigated by finite-element analysis (FEA). Two different leadframe samples, which were composed of the same tin–copper coating on two different copper-leadframe materials, namely, copper–iron (hereafter, CUFE; corresponding to CDA number C19400) and copper–chromium (CUCR; CDA number C18045), were used to examine the whisker-initiation behavior on the coating surfaces. The two samples showed significantly different tendencies of whisker initiation from the coating. That is, after long-term storage at room temperature, no whisker initiation was observed on the coating on the CUCR sample, whereas long whiskers (with a maximum length of more than 200 m) were formed from the coating on the CUFE sample. The FEA calculation on the leadframe samples revealed that the coatings had a two-directional stress gradient, namely, one gradient toward the surface and another toward the base leadframe material. It also indicated a difference between the stress distributions in the two samples. The gradient of normal stress on the coating's grain boundaries (GBs), toward the surface of the CUFE sample, was found to be larger than that in the CUCR sample. This result implies that the tin-atom flux along a GB in the coating on the CUFE sample was larger than that on the CUCR sample because the atom flux along the GB was proportional to the stress gradient. It agrees with the above-mentioned whisker-initiation behaviors in the samples.We thus conclude that in the CUFE sample, a whisker initiates either from a surface grain immediately on top of a GB or from surface grains located on both sides of the same GB. To confirm this conclusion, the correlation between the tin-diffusion sites and whisker formation sites was investigated. Simulation of atom diffusion by molecular dynamics indicated that the dominant tin-diffusion site is a GB when compressive stress is applied in the direction normal to the GB. Investigation of the correlation between the whisker roots and coating microstructures of the CUFE sample showed that the whisker roots were located on top of GB intersections in the coating. These results indicate that whisker-initiation sites are correlated with dominant tin-diffusion sites and that each whisker initiates either from a surface grain located immediately on top of a GB or from surface grains located on both sides of the same GB.

CPMT Transactions Publish Special Sections

Do you have an interest in Through Silicon Vias? Or Electrical Modeling and Simulation of High-Speed ICs and Packages? Then make sure to see the Special Sections on these topics published in the CPMT Transactions. Information on these Sections follows.

Special Section on Recent Progress in Electrical Modeling and Simulation of High-Speed ICs and Packages

IEEE TRANSACTIONS ON ADVANCED PACKAGING, VOL. 33, NO. 4, NOVEMBER 2010

As on-chip design scales into the nanometer regime, the exponentially increased complexity of integrated circuits (ICs) has made circuit modeling and simulation increasingly challenging. The number of transistors has doubled approximately every 18–24 months. All these transistors are connected via interconnect lines. As a result, the circuit modeling and simulation tools are required to solve larger and larger problems. Although state-of-the-art modeling and simulation techniques represent an impressive improvement as compared with conventional techniques, they do not scale well when applied to matrices of exponentially increased sizes encountered with the analysis and design of next-generation ICs. Therefore, it is of critical importance to reduce the computational complexity of existing modeling and simulation methods to pave the way for the continual VLSI revolution for years to come.

Moreover, the modeling and simulation of next-generation ICs and packages is complicated by the need for a full-wave electromagnetics (EM)-based analysis for the following reasons: reduced feature sizes that lead to subwavelength optical lithography; increased interconnect speeds for faster data transmission on the chip and between chips and subsystems; increased level of integration that requires an EM-based analysis to overcome the fundamental limits of a circuit-based analysis; and the advent of alternative technologies such as on-chip wireless communication, etc. While computational electromagnetics has found many successful engineering applications, the performance of existing techniques is still inadequate when tackling large-scale IC design problems.

This special section presents a snapshot of the recent progress in electrical modeling and simulation of high-speed ICs and packages. It is not intended to be an exhaustive review of the work that has been done in this research area, but rather an exhibition of recent work and innovative ideas for inspiring further research in this exciting topic. The papers of this special section were invited from both academia and industry. The industry relevance helps ensure the value and impact of the research conducted in this area. Researchers from both circuits and electromagnetics communities have contributed to this special section. It is envisioned that some of the greatest inventions of future integrated circuits and packages could arise from the intersection of circuits and electromagnetics. The unique modeling and simulation challenges associated with ICs and packages such as exponentially increased problem sizes and a broad electromag- Digital Object Identifier 10.1109/TADVP.2010.2099155 netic spectrum from dc to high frequencies will also serve as the driving force of the innovations in electromagnetics.

There are 10 invited papers in this special section, which can be grouped into two main areas. The first area is simulation, and the second area is modeling. In the area of simulation, the paper entitled "Waveform Relaxation Time Domain Solver for Subsystem Arrays" presents a waveform relaxation approach for the transient analysis of 3-D electromagnetic problems using the partial element equivalent circuit (PEEC) method. The paper entitled "A Flexible Time-Stepping Scheme for Hybrid Field-Circuit Simulation Based on the Extended Time-Domain Finite Element Method" describes a flexible time-stepping scheme for a recently developed hybrid field-circuit solver based on the extended time-domain finite element method (TDFEM) to alleviate the limitation on the use of a system-wide global time-step size. In "A Thermal Simulation Process Based on Electrical Modeling for Complex Interconnect, Packaging and 3D Structures," the authors uses a methodology, which exploits electrical resistance solvers for thermal simulation, to allow the fast acquisition of thermal profiles of complex structures with good accuracy and reasonable computation cost.

In the area of modeling, there are seven papers. Four of them focus on the reduction of the computational cost of existing modeling methods. One is entitled "A Novel High-Capacity Electromagnetic Compression Technique Based on a Direct Matrix Solution," which presents a novel method to compress low rank sub-block matrices into a sparse matrix for obtaining an efficient high-capacity integral-equation based electromagnetic solver. The other is entitled "An LU Decomposition Based Direct Integral Equation Solver of Linear Complexity and Higher-Order Accuracy for Large-Scale Interconnect Extraction." In this paper, a linear-complexity LU factorization is developed to directly solve a dense system of linear equations for the capacitance and full-wave extraction of any arbitrary shaped 3-D structure embedded in inhomogeneous materials. The paper, "Electromagnetic Modeling of Through-Silicon Via (TSV) Interconnections Using Cylindrical Modal Basis Functions," proposes an efficient method to model through-silicon via interconnections, an essential building block for the realization of silicon-based 3-D systems. In the fourth paper, "A Markov Chain Based Hierarchical Algorithm for Fabric-Aware Capacitance Extraction," a hierarchical algorithm is proposed to compute the 3D capacitances of a large number of topologically different layout configurations that are all composed from the same basic layout motifs.

The paper entitled "Physics-Based Gridding for Electrical Package Analysis Codes" describes techniques and advances for mesh generation and refinement for the analysis of electrical package structures. In the paper entitled "Random Rough Surface Effects on Wave Propagation in Interconnects," the rough surface effects in high speed interconnects on printed circuit boards and microelectronic packages are studied. This paper reviews the analytical theory, numerical simulations and experimental results based on a model that characterizes the rough surface by a stochastic random process with correlation function or spectral density. The paper, "Accurate Characterization of Broadband Multiconductor Transmission Lines for High-Speed Digital Systems," proposes the combination of both time and frequency

measurement data to mitigate the dc accuracy issue, and a new de-embedding technique to mitigate the port discontinuity issue encountered in the modeling of transmission lines from frequency domain measurements.

DAN JIAO, *Guest Editor*
School of Electrical and Computer Engineering
Purdue University
West Lafayette, IN 47907 USA

Special Section on Through Silicon Vias

IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY, VOL. 1, NO. 2, FEBRUARY 2011

Through silicon vias (TSVs) are an essential technology for 3D integration, which enables scaling of electronic system performance beyond that provided by Moore's law. TSV technology allows heterogeneous processess (CMOS, SiGe, III-V, MEMS, nanodevices, etc.) and functions (logic, memory, RF, analog, sensors, optoelectronics, etc.) to be vertically integrated on a single package, thereby reducing interconnect delays, form factors, and power consumption. It also facilitates modular design by mixing and matching existing silicon for improved time to market. In the past decade, there have been numerous feasibility demonstrations of TSV processes. As the industry is moving past the feasibility phase and into the commercialization phase of the TSV technology, it is becoming increasingly important to optimize the electrical design of TSV interconnections in order to best exploit the benefits of the technology.

This special collection of 11 papers has a twofold purpose. First, it presents a snapshot of recent progress in electrical modeling and design of TSVs by researchers from both academia and industry. It is not intended to be an exhaustive review of the work that has been done in the area, but rather an exhibition of the latest work with the hope that it will inspire further research in this exciting topic. Second, it also seeks to encourage researchers from various disciplines, including devices, circuits, and system architectures, to contribute papers on this topic to the IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY. It is envisioned that major breakthroughs toward the market success of the TSV technology will arise from close collaboration between circuit designers, package designers, and system architects.

The special section is organized into three main areas. The first group of papers deals with the electromagnetic modeling of TSVs. The paper entitled "High-Speed Design and Broadband Modeling of Through-Strata-Vias (TSVs) in 3D Integration" reviews fundamentals in characterization and modeling of a TSV structure and compares a variety of TSV shapes. The second paper, "Design and Modeling Methodology of Vertical Interconnects for 3DI Applications," presents a compact semi-analytical model taking into consideration silicon substrate induced dispersion as well as skin and proximity effects. The following paper entitled "Fast and Accurate Analytical Modeling of Through-Silicon-Via Capacitive Coupling" first introduces a simple analytical model for fast estimation of coupling capacitance between regularly placed, square-shaped TSVs, and then extends it to more general layouts with TSVs being placed Digital Object Identifier 10.1109/TCPMT.2011.2116970 irregularly, which is applicable to CAD applications such as full-chip timing analysis and layout optimization in 3D ICs. The last paper is "High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)" and presents a practical TSV model including bumps and redistribution layers. The strength of the paper lies in combining modeling with experimental results from a fabricated test vehicle.

The second group of papers is on the signal integrity and power integrity analysis of TSV interconnections. The paper entitled "Peak-to-Peak Ground Noise on a Power Distribution TSV Pair as a Function of Rise Time in 3-D Stack of Dies Interconnected Through TSVs" analyzes the waveform of power/ground switching noise for a simplified on-chip power distribution network. The second paper titled "PDN Impedance Modeling and Analysis of 3D TSV IC by Using Proposed P/G TSV Array Model based on Separated P/G TSV and Chip-PDN Models" presents a modeling approach to study the effects of TSVs on stacked power distribution networks. The next paper entitled "Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring" addresses modeling, measurement, and design issues of noise coupling problems between TSVs or between an active circuit and a TSV. Especially in the above two papers, the authors have demonstrated good model-to-hardware correlation, which has rarely been seen in recent publications on TSV modeling. The last paper, "Electrical-Thermal Co-simulation of 3D Integrated Systems with Micro-fluidic Cooling and Joule Heating Effects," discusses an electrical-thermal modeling methodology, which allows thermally-aware design of stacked chips with power dissipation that is too high for conventional solutions to work.

The third group of papers explores the system architectures and applications that might benefit from the TSV technology. The paper entitled "Low Power and Reliable Clock Network Design for Through-Silicon Via (TSV) Based 3D ICs" focuses on clock distribution which is one of the most challenging issues in 3D integrated system design. The paper proposes a smart synthesis algorithm, providing good guidance for how to design an initial clock tree in a 3D environment. The next paper entitled "TSV Technology for Millimeter-Wave and Terahertz Design and Applications" looks into the possibility of applying the TSV technology to designing passive components such as substrate integrated waveguides, filters, and antennas for millimeter-wave applications. The final paper entitled "Through-Silicon-Via (TSV) Design for a 3D-Solid-State-Drive (SSD) System with Boost Converter in a Package" presents the development of a solid-state-drive system using the TSV technology. The proposed boost converter enables charge pumps to be removed from each NAND chip, reducing area and power consumption.

DONG GUN KAM, *Guest Editor*
IBM T. J. Watson Research Center
Yorktown Heights, NY 10598 USA

JOUNGHO KIM, *Guest Editor*
Korea Advanced Institute of Science and Technology (KAIST)
Daejeon, 305-701 Republic of Korea

Conference News....

Crouching Package Hidden Silicon – Battles in the 34th IEMT 2010 in Malacca

By Shaw Fong Wong and Choong Kooi Chee

Papers from IEMT 2010 are available in IEEE Xplore at: http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5740544

Historic Malacca was the battle ground of the Portuguese, Dutch, English colonials and the local sultanates in the last millennium because of its strategic location between the east and the west. In early December this year, it was again a battle ground but this time it was for 105 electronic packaging technologists to win the best Industrial or Student paper awards of a premier semiconductor manufacturing conference. The prestigious 34th International Electronic Manufacturing Technology (IEMT) 2010 conference was held at the scenic Straits Settlement of Malacca with 300 participants from all over the world converged in the beautiful Renaissance Hotel. The technical co-sponsors of this conference were Institute of Electrical and Electronics Engineers (IEEE) and its electronic packaging society known as Component, Packaging & manufacturing Technology (CPMT).

Since 2006, the IEEE CPMT Malaysia chapter was the main driver of IEMT with its core members in the organizing committee. The members are employees of local multinational semiconductor companies such as Intel, Infineon, On Semiconductor, Freescale Semiconductor, Carsem, ST Microelectronics and national Semiconductors. The local universities members in this year's organizing committee are from Universiti Teknology Malaysia (UTM), Universiti Teknikal Malaysia Melaka (UTeM) and Multimedia University Malaysia (MMU). The whole conference was planned and run without the help of event managers.

The majority of the participants were from Malaysia and there were 25% overseas participants from seventeen countries namely Singapore, Australia, Taiwan, Europe, Japan and the United States of America. The first day of the conference was short-course workshops from technical experts and the courses were *State-of-the-art and trends in 3D IC/Si integration and WLP* by Dr. John Lau (Taiwan's Industrial Technology Research Institute), *Advanced copper wirebonding technology* by Dr. Hong Meng Ho (Semicon Fine

The IEMT 2010 organizing committee with IEEE CPMT VVIP.

The fully packed conference hall for IEMT 2010 opening address and keynote speeches.

Dr. Aschenbrenner opening address and keynote.

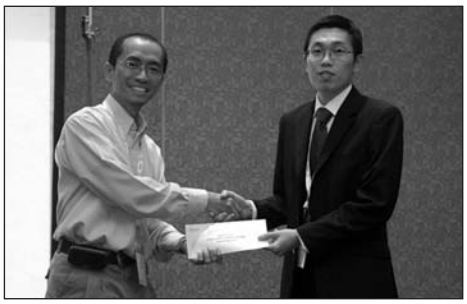
Dr. Chen, the packaging pugilist, on crouching tiger.

Dr. Knoblauch packages for vehicles.

Dr. Baraton on ST Microelectronics packages.

Souvenir presentations to Mr. Fjelstad by Mr. Shaw Fong Wong and Mr. Wagiman by Ms Fuaida Harun.

Technologists delivering important points on packaging to the audience.



Winners of IEMT2010 awards (top left clockwise): A. Haque (Student – Master), E Eid (Student – PhD), Octovia Peter (Best Poster), WL Law (Industry- Best) and both YH Lee & Ian Chin (Industry Merit).

A panel session to showcase the collaboration between Intel and local universities.

Participants having fun mingling around and building network.

Participants were entertained with cultural dance show during dinner and going on a river cruise on beautiful Malacca River after dinner.

Wire), *Past, present and future of electronic packaging* by Mr. Joseph Fjelstad (Verdant Electronics) and *Flip chip technology* by Dr. Yutaka Tsukada (Osaka University). The remaining two days comprised keynote speeches, invited talks, paper & poster presentation sessions and panel discussion session from leaders of the industry. The excellent keynotes were given by Dr. Rolf Aschenbrenner (IEEE CPMT President), Dr. William Chen (Past IEEE CPMT President), Dr. Tsukada, Dr. Andreas Knoblauch (Infineon), Mr. Fjelstad, Dr Xavier Baraton (ST Microelectronics), Mr. C. S. Liu (National Semiconductor) and Mr. Kim Hyland's representative (Cisco). All the speakers talked on the most relevant topics of the industry: 3-dimensional packaging and Through-Si-Via (TSV).

The four-track oral presentation sessions consisted of 94 papers from technologists and four invited papers. The topics of discussion ranged from wirebond to flip chip, materials to processes and simulations to reliability. The international participants contributed 40% of the papers. About 20% of the total papers were from the academia. The invited papers were from Mr. Amir Wagiman (Intel), Mr. John Hunt (ASE), Dr. Tsukada (Osaka University) and Mr. Shankar Shridhar (EQIS) on relevant topics of the industry. Poster presentations were carried out by the technologist at the main hall together with exhibitors. The conference provided an opportunity for the participants to build network in various areas of electronic packaging.

Awards were given to top presenters from the industry and university. The judges for these awards are experts in the areas of electronic packaging. The best Industry Paper Award was given to WL Law of Carsem on her paper *"A reliable low cost assembly technology for 0201 compatible QFN, X3 Thin QFN"*. Intel took two merit awards by Ian Chin and Yun Hsiang Lee for their papers on "*The very first strain range bound guidance methodology for system level shock evaluation"* and *"Alternative package coplanarity requirement and its correlation to reflow warpage"*, respectively. The two students who won the best Student Paper Award for PhD and MSc categories were Mr. E. Eid from Universite de Savoie on *"Frequency and time domain characterization of substrate coupling effects in 3D integration stack"* and Mr. A Haque from University of Malaya on *"Effect on interfacial reactions and die attach properties of Zn-Al-Mg-Ga high temperature*

Pb-free solder by introducing Ni metallization on Cu substrate", respectively. The best Poster Award went to Octovia Peter of Intel on *"Extending the technology envelope of equipment fungibility with single minute exchange die novel solutions"*. Congratulations to the winners!

A special panel session was set-up to showcase the collaboration between Intel and local universities. It was chaired by Dr. Choong Kooi Chee with panelists Mr. Dennis Chandran from Intel and Dr. Nasir Tamin from UTM. There were frank and open discussions on the industry's engagement with Malaysia's local universities. All the leaders from the industry wanted to do more to grow the technical competencies of our local universities.

On top of the serious technical discussions, the participants were treated to a river cruise along the romantic Malacca River at night and a uniquely Malacca cultural show during the conference dinner. The participants were able to savor the delicious local delicacies.

IEMT 2010 was a very successful conference with all the participants having great times learning about the latest and greatest packaging technologies and network with people with added fun and laughter. IEMT 2012 will be held in the cultural city of Ipoh. This year, Dr. Chen talked about packaging in the year of the tiger and perhaps, in 2012, he can talk about packaging in the year of the dragon. See you all in Ipoh for the 35th IEMT 2012.

EPTC 2010 Conference Report

Papers from EPTC 2010 are available in IEEE Xplore at: http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=5685177

EPTC 2010, 12th Electronics Packaging Technology Conference, was held on 8th–10th December 2010 at Shangri-La Hotel, Singapore. This premier international conference is organized by the Rel/CPMT/ED Singapore Chapter of IEEE Singapore Section and jointly sponsored by IEEE CPMT Society and Singapore Exhibition and Convention Bureau.

This 3-day event featured Keynote Addresses, Short Courses, Exhibitions, Technical Sessions and Social Networking activities. With the support across 9 technical categories and its 125 Technical Committee members, we reviewed 219 abstracts from 25 countries globally. In 5 Tracks and 35 sessions, a total of 165 papers were selected for oral presentations and 20 papers were selected for poster presentations. Papers are from, 40% Academia, 15% Research Institute and 45% Industry.

These papers covered a wide spectrum of topics includes Advanced packaging Technology, Material & Processes, Electrical Simulation & Signal Integrity, Mechanical Simulation & Structural Integrity, Interconnect Technology , Quality & Reliability and Emerging Technology, Printed electronics and package/wafer testing .

There were over 324 delegates from 25 countries, 40 Universities, 14 Research Institutes and 36 corporations attended the conference.

During the conference, we announced the EPTC/CPMT Conference Paper Awards (From 2009 to 2011). These awards were co-sponsored by IEEE CPMT Society and EPTC. These awards include Best Paper Award, Outstanding Paper Award, Best Poster Award, Best Student Paper Award and Outstanding Student Paper Award. A Best Paper Select Committee comprising of members from CPMT, EPTC Board and the EPTC 2010 Organizing Committee shall be reviewing nominated papers for the prestigious awards that will be awarded at EPTC 2011.

We were privileged to have Mr. Tom Gregorich, MediaTek, USA, and Prof. Reinhard R. Baumann, Fraunhofer Institute, Germany, to deliver keynote addresses at the opening of the conference. The conference also had 6 well attended Short Courses led by Industrial and academic experts. This year, the Tabletop Exhibition consisted of 14 companies who braved against a slow market, to share and promote their services and products at EPTC 2010. The exhibits received good exposure over the 2-day conference.

An evening banquet was organized at east coast, Thai Pan Restaurant, Civil Service Club @ Changi Village. This informal dinner with live-band, BBQ and wines, supplemented the tightly packed symposium and provided the delegates opportunities to interact and network.

We are thankful to our Sponsors, Paper Authors, Invited Speakers, Course Instructors, Technical Committee Members, Secretariat Staffs and Organizing Committee in making EPTC 10 yet another successful and memorable event.

IWASI 2011

4th IEEE International Workshop On Advances in Sensors and Interfaces 28/29 June 2011 - Savelletri, Italy

http://iwasi2011.poliba.it

Workshop Chair:

D. De Venuto (*Politecnico di Bari and INFN Bari - Italy*)

Steering Committee:

B. Courtois (*CMP Grenoble-France*)

M. Declercq (*EPFL Lausanne-Switzerland*)

G. Gielen (*Univ. Leuven-Belgium*)

B. Riccò (*Univ. di Bologna-Italy*)

C. Van Hoof (*IMEC Leuven-Belgium*)

Technical Program Committee:

L. Benini (*Univ. di Bologna-Italy*)

E. Cantatore (*Eindhoven Univ. of Technology-The Netherlands*)

S. Carrara (*EPFL Lausanne-Switzerland*)

H. Casier (*AMI Semiconductors, Bruxelles-Belgium*)

K. Chakrabarty (*Duke University-USA*)

G. De Cesare (*Univ. La Sapienza Roma-Italy*)

F. Grancagnolo (*INFN Lecce-Italy*)

M. Kayal (*EPFL Lausanne-Switzerland*)

K. Makinwa (*Delft University of Technology-The Netherlands*)

S. Mir (*TIMA Grenoble-France*)

E. Nappi (*INFN Bari -Italy*)

L. Rufer (*TIMA Grenoble-France*)

P. Siciliano (*IMM-CNR Lecce-Italy*)

A. Taroni (*Univ. di Brescia - Italy*)

L. Torsi (*Univ. di Bari-Italy*)

M. J. Ohletz (*ZMD AG-Germany*)

M. Savino (*Politecnico di Bari-Italy*)

B. Vigna (*ST Microelectronics-Cornadero-Italy*)

Local Committee:

E. Nappi (*INFN Bari - Italy*)

D. De Venuto (*Politecnico di Bari and INFN Bari-Italy*)

Sensors and Sensor Systems are an enabling factor for many applications, such as, for instance, industrial automation, robotics, vision, instrumentation, ambient intelligence. On the other hand, ever more stringent requirements force sensors and their electronics to become more and more sophisticated, and often be fabricated with advanced micro- and nano- technologies (or at least be contained in the same package). Operating conditions too represent a continuous source of challenging problems, such as, for example: systems in remote locations calling for low power consumption and energy harvesting; noisy environments (industrial environments, automobiles, space aircrafts,.) requiring suitable interfaces; applications (biomedicine, particle physics and electrochemistry,.) with critical specifications in terms of safety and/or speed; harsh environmental conditions producing fast ageing and performance degradation.

In spite of the significant advances of the last two decades, new problems are continuously encountered and must be solved with new ideas and approaches. In particular, this holds for modeling, design procedures, fabrication techniques and cost, power supply, energy management, testing, networking operation.

The IEEE International Workshop on Advances in Sensors and Interfaces provides a forum for exchange of experience among experts actively involved in research, development and evaluation of new concepts, theoretical methods and experimental characterization in the broad field of modern Sensors and Sensor Systems.

TOPICS

Papers are solicited in the following and related topics:

- Sensor interfaces
- Sensors in biomedical and environmental applications
- Automotive sensor & sensor interfaces
- New materials and new technologies for sensors
- Sensor modeling and design techniques
- Sensors for space, nuclear and particle physics
- Optoelectronic and photonic sensors
- MEMS and MOEMS-based sensors
- Post-processing electronics
- Noise reduction techniques in sensors interfaces
- Testing techniques for sensors systems
- Sensors networks

European Microelectronics and Packaging Conference (EMPC-2011) Brighton, UK, 12th–15th September 2011

EMPC-2011 features the *Building Blocks of Electronics*

The Event

IMAPS-Europe European Microelectronics and Packaging Conference EMPC is the Major Electronics packaging, interconnection and integration conference of Europe. EMPC2011 is technically co-sponsored by IMAPS-Europe and IEEE-CPMT and builds upon the successful IEEE Electronics System-Integration Technology Conference ESTC (2010, Berlin) and EMPC2009, (2009) Rimini. Each biennial event attracted over 350 delegates worldwide. EMPC-2011 is proudly hosted by IMAPS-UK chapter and will be held at the Hilton Metropole, Brighton, UK, 12th to 15th September 2011.

The Location

Brighton is one of England's loveliest and liveliest cities by the sea. It is also a great location to reach London, and many of the sights of Southern England. It's a fun, thriving, cosmopolitan city with just a touch of eccentricity. Brighton is a fantastic mixture of classical architecture, 21st century nightlife, endless shopping, top quality performing arts and the best selection of restaurants outside central London—all within easy walking distance.

The Hilton is ideally located directly on the seafront with uninterrupted sea views and immediate access to the beach. Further along the shore is Brighton Marina and the world famous Brighton Pier. Other notable sites are nearby.

Announcement

EMPC 2011 will take to Brighton the best of microelectronics packaging and interconnection technologies, thus offering top quality coverage of technological innovation in this field. The four conference days from 12th to 15th September 2011 will consist of Short Courses/ Tutorials, the Conference and an Exhibition. The event will be complemented by Poster Sessions and Social Events.

The Conference Topics include

ADVANCED PACKAGING: Single Chip and Multi Chip Packaging, Wafer Level Packaging, 3D-WLP, 3D-IC, SIP, SOP and other Systems-Integration Technologies, Embedded Passives on Wafers and Substrates, High Frequency and High Power Packaging, LTCC Technologies, PCB and BGA Substrates Design and Technologies, Laminates, Micro-Vias and Build-Up Technologies, Flex, MID.
BUSINESS ASPECTS: All business aspects of the microelectronics packaging and assembly industry and the supply chain.
INTERCONNECTION TECHNOLOGIES: Thick and Thin Film Technologies, Wire Bonding, Bumping, Flip Chip Bonding, Cu/Low-k Wafers, Through Silicon Vias, Lead-Free Soldering and Adhesive Joining.
MANUFACTURING TECHNOLOGIES AND MATERIALS: Process Development, New Equipment, Yield Improvement, Cost and Cycle Time Reduction, Green Manufacturing, Adhesives, Encapsulants, Underfills, Moulding Compounds, Lead-Free Solder Alloys, Halogen Free Materials, Dielectrics and Ceramics.
MEDICAL ELECTRONICS: Applications, Design, Development, Manufacturing that comply with complex and demanding regulations and market requirements.
MEMS PACKAGING: MEMS Based Sensors and Actuators Packaging, RF-MEMS, Optical MEMS and Bio-MEMS.
MODELLING: Electrical Modelling, Signal Integrity: TDMA and FDMAof Interconnection & Packaging, Thermal Characterisation, Cooling Solutions—Methodology for Characterisation of Advanced Packaging, Modules & Systems, Novel Cooling, Mechanical Modelling, Structural Integrity, Thermo-Mechanical Stress Analysis, Vibration & Shock Tests;
MORE THAN MOORE: The future of IC shrinkage, future options for IC packaging & interconnect, 3D.
NANO TECHNOLOGIES: Smart Materials, Interconnections, Nano-Scale Packaging.
OPTOELECTRONICS: Power LED Assembly, Packaging and Light Guiding, Packaging of Optoelectronic Modules suitable for Gb/s Fibre Optic Communication.
POWER ELECTRONICS: Application in Consumer, Telecom, Automotive, Wearable, Space and Defence.
RELIABILITY and QUALITY: Specialised topics, Component, Board and System Level Reliability Assessment, Failure Analysis, Interfacial Adhesion, and Accelerated Testing.
SMART TEXTILES: Materials, Technologies, Applications, Markets, Roadmaps.
SOLAR ENERGY & PHOTOVOLTAICS: Packaging & Interconnection, Design to improve Efficiency of Photovoltaic modules, Reliability and Qualification Approaches.

SHORT COURSES / TUTORIALS

Proposals are invited from professionals to give 3-hour or 6-hour tutorials on the topics suited to delegates to EMPC-2011. Send proposals for Short Courses to conference@empc2011.com.

OPPORTUNITY TO EXHIBIT

The exhibition is an important element of the EMPC format and compliments the Technical conference. The exhibition is based on space only or a shell scheme within the Exhibition Hall. The exhibition is positioned near the technical session rooms. Details of Exhibition Hall layout, pricing and how to book and are provided in the Exhibitor Registration Pack, which can be downloaded at www.empc2011.com. For exhibition bookings and information: exhibition@empc2011.com.

http://www.ewh.ieee.org/soc/cpmt/tc1/h2011/h2011top.html

57th IEEE Holm Conference on Electrical Contacts

Purpose

To provide a forum for the presentation and discussion of the latest developments in the field of electric contacts and the application of recent advances in materials and processes in electric, electronic and telecommunication equipment. 2011 will be an exciting conference and we expect up to 40 technical papers presented over two and a half days with extra opportunities for international networking.

For Whom

Practicing designers, engineers, physicists and research scientists—those new to the field and those experienced. The 2011 Conference will include excellent papers authored by some of the outstanding technical people in this field. The international contributors come from universities and industries in USA, Austria, Canada, Japan, China, France, Switzerland, Russia, Germany, United Kingdom and other countries. These papers will provide the attendees with up-to-date information on a wide range of subjects that makes this conference so attractive to the practicing engineer. Additionally, the joint conference will make it possible for any attendee to discuss with other international authors, on work presented by the author at the conference or any subject related to the author's field of expertise.

Background

The Holm Conference began in 1953 as a forum for the discussion of electrical contact phenomena and related fields. In 1968, the conference was named the Holm Conference in honor of Dr. Ragnar Holm. Dr. Holm, whose contributions to the field of electrical contacts spanned 50 years and form the foundation of the electrical contacts field, was the inspiration and guide of the Conference from its inception until his death in 1970. In 1985, IEEE society started sponsoring the conference as a recognition of its importance in the field of electrical engineering. In addition to the Annual Conference, the Conference Organization regularly conducts an intensive one-week course on contacts and participates in the biannual International Conference on Electrical Contacts.

Technical presentations normally also include the Ragnar Holm Scientific Achievement Award, the Dr. Morton Antler Lecture and hot topic panel workshops. They highlight the most recent electrical contact work all over the world.

Contacts Properties and Performance, Connector Contacts, Sliding Contacts, Aluminum Contacts, Arcing Contacts, Silver Metal Oxide Contacts, MEM Systems, Automotive Switches and Relays, Superconductor Contacts, and Real world Design and Applications Problems are familiar themes in the presentation. Recent activities on Arc Fault Detection, AFCI, Smart Grid, ROHS and renewable power generation are adding new themes to the technical program.

The 6th International Microsystems, Packaging, Assembly and Circuits Technology Conference IMPACT 2011 on Oct. 19–21 at NTUH International Convention Center www.impact.org.tw **IMPACT-Leading Innovation**

The 6th International Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2011) is organized by IEEE-CPMT, ITRI, i-MAPS- Taiwan, ISU, SIPO , TPCA and co-organizers by iNEMI, ICEP, SMTA and TTMA, which will take place in NTUH International Convention Center during October 19 to 21, 2011. Besides original SIPO 3D IC session, this is the first time that IMPACT organize arranges ICEP and iNEMI sessions this year. We believe IMPACT 2011 will become more splendid after their support. This great annual international event—IMPACT will extend the opportunity to bring researchers, engineers and experts engaged in such a distinguished gathering and show the strength of Taiwan and update worldwide tendencies.

IMPACT 2011 as the sixth conference and the theme is "IMPACT-Leading Innovation" which reflects the age of technology resolution. The appearance of smart phones and touch panels declare the innovation time and we highly welcome outstanding papers from all over the world to respond the theme and compete with elites overseas on the international stage. IMPACT is striving to work out the advanced paper scope and reward policy to attract extraordinary papers all around the world. IMPACT now is calling papers until June 10, 2011. More information about IMPACT 2011, please refer to the conference website, http://www.impact.org.tw, or contact with secretariat, MS. Sophia Huang (+886 3 381 5659 Ext 404).

About Paper Submission

Important Date Item	Date	Remark
Abstract Submission	June 10, 2011	400–500 words Submit on-line through conference website
Abstract Acceptance Notification	July 15, 2011	Notice sent via email
Full Paper Submission (Camera-ready Version)	August 15, 2011	4 pages including figures and tables Submit on-line through conference website
Presentation Material Submission(Oral Presentation)	October 1, 2011	15 minutes presentation plus 5 minutes Q&A Please email to the service@impact.org.tw

SCOPE OF PAPER SOLICITED

P1. Emerging Systems Packaging Technologies
P2. Advanced Packaging Technologies
P3. Interconnections & Nanotechnology
P4. Modeling, Simulation & Design
P5. Thermal Management
P6. Advanced Sensor & Microsystems Technology (MST)
P7. Advanced Materials, Process & Assembly
P8. 3D Integration [*NEW]
P9. LED & Optoelectronics Packaging [*NEW]

Secretariat

Taiwan Printed Circuit Association (TPCA)
Tel: +886 3 381 5659 #404 - Sophia
Fax: +886 3 381 5150 E-Mail: service@impact.org.tw

IEEE CPMT Society's ASTR Annual Workshops and Our 2011 ASTR Event

"The golden rule of an experiment: the duration of an experiment should not exceed the lifetime of the experimentalist"
Unknown ASTR Engineer

The IEEE CPMT Society's annual Accelerated Stress Testing and Reliability (ASTR) Workshops started in 1995 at Tandem Computers, Inc., in Cupertino, CA. The first 1995 ASTR event was sponsored by the Santa Clara Valley (SCV) CPMT Chapter, the CPMT TC-7 Technical Committee, and the SCV Chapter of the IEEE Industrial Electronics Society (IES). The incentive for "launching" the Workshops was due to the understanding that Accelerated Stress Testing (AST) had become an accepted practice when seeking ways to create high quality products, as well as to understanding that the best AST practices of the lead companies, if shared with the "reliability community", could be viewed as models upon which other companies could build their short- and long-term AST activities. The "**founding fathers**" of the first ASTRs included (in alphabetical order of the last names) Cheryl Ascarrunz, Gil Bastian, Tony Chan, Mark Gibbel, Kirk Gray, Greg Hobbs, David Horsma, Edmond Kyser, Joe Mantz, Harry McLean, Dennis Pachucki, Paul Parker, Paul Wesling. The ASTRs were created as, and still are, forums for sharing novel and useful AST methodologies, techniques and results for assemblies, packages, subsystems and systems employed in electronics engineering. These events include technical presentations, tutorials, panel discussions and trade shows, and have become highly popular among the worldwide reliability engineering communities.

The AST Workshops are intended to **share ideas** on better ways of accelerating and detecting hidden defects, flaws, and weaknesses in electronic and electro-mechanical hardware that would result in failures during usage. These techniques are focused on testing electronic hardware to destruction limits and root cause investigation to determine the physics-of-failure. The goal of AST is to produce mature products at market introduction and, in making it robust, the product can be screened for manufacturing defects with high combined stresses (beyond end-use specifications) for shorter lengths of time. Over the last few years, AST has been embraced by an ever widening array of companies seeking to reconcile the need for the highest quality product with the necessary push for early time-to-market.

The ASTR workshops held during the recent years are pursuing some particular objectives **("themes")** that the ASTR organizing committee viewed as the most crucial and the timeliest for the electronic industries. The themes of the recent ASTR events were: "Accelerated Life Testing, Its Role, Challenges, Attributes, and Interaction with Qualification Testing" (2007, College Park, MD); "Achieving Cradle to Grave Reliability Using DfR and AST" (2008, Portland, OR); "Renewable Reliability" (2009, Jersey City, NJ); "Bridging the Gap between the Test Lab and Field Failure" (2010, Denver, CO). The 2011 ASTR Workshop will be held on **September 28–30, Hyatt, San-Francisco, CA.** Its theme is "Do the Electronic Industries Need a New Approach to Qualify Their Products?" The information of the 2011 ASTR event, as well as of the previous ASTR Workshops, can be found at www.ieee-astr.org.

ASTR 2011 will provide a forum for ASTR knowledge and share ideas that address intra and inter industry endeavors to limit and eliminate field failures of products. The **focus** will be on rapidly finding design weaknesses, developing robust systems, and improving strategies to cost effectively screen defects and weaknesses in electronic and electro-mechanical hardware and structural systems while reconciling twin needs of obtaining high product quality and reliability with that of low product development and manufacturing costs and timely introduction of new products to market. The event is technically co-sponsored by the University of California at Santa Cruz, by several other-than-CPMT IEEE Societies and by some leading non-IEEE professional societies (American Institute of Aeronautics and Astronautics, American Physical Society, Materials Research Society, American Society of Mechanical Engineers, Prognostication and Health Monitoring Society, and others).

Presentations are sought in, but are not limited to, the following **major topics**: Re-Thinking and Re-Visiting Qualification Specs; ASTR in Energy Efficient Hardware; Accelerated Stress Testing & Field Failures; COTS Components in Military Hardware Systems; Failure Analysis (FA) & Prognostics and Health Management (PHM); Predictive Modeling & Field Failures; Product Robustness & Cost Control.

2011 ASTR Workshop will be an **international event**: members of the organizing committee came from all over the world. We expect that about 250 reliability engineers will participate in the 2011 event. Important deadlines are: abstract submission: March 15, 2011; final presentation (full-length paper) submission in electronic format: August 15, 2011.

See you in San-Francisco in September 28–30, 2011!

E. Suhir, 2011 ASTR General Chair

Upcoming CPMT Sponsored and Cosponsored Conferences....

Name: 2011 21st IEEE Semiconductor Wafer Test Workshop (SWTW 2011)
Dates: June 12–15, 2011
Location: San Diego, CA USA
Contact: Maddie Harwood
E-mail: maddie@cemamerica.com
URL: http://www.swtest.org/index.html

Name: 2011 4th IEEE International Workshop on Advances in Sensors and Interfaces (IWASI 2011)
Dates: June 28–29, 2011
Location: Savelletri di Fasano, Italy
Contact: Daniela De Venuto
E-mail: d.devenuto@poliba.it
URL: http://iwasi2011.poliba.it

Name: IEEE/IMAPS Workshop on Optoelectronic Packaging
Dates: June 28–30, 2011
Location: Irvine, CA USA
Contact: Jackki Morris-Joyner
E-mail: jmorris@imaps.org
URL: http://www.imaps.org/opto/

Name: 2011 7th Annual Organic Microelectronics and OptoelectronicsWorkshop
Dates: July 18–20, 2011
Location: San Francisco CA, USA
E-mail: organic_microelectronics@acs.org
URL: http://acswebcontent.acs.org/organicmicroelectronic/index.html

Name: 2011 3rd Asia Symposium on Quality of Electronic Design (ASQED 2011)
Dates: July 19–20, 2011
Location: Kuala Lumpur, Malaysia
Contact: Ali Iranmanesh
E-mail: alii@isqed.org
URL: http://www.isqed.org

Name: 2011 International Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP 2011)
Dates: August 8–11, 2011
Location: Shanghai, China
E-mail: empt-cie@sohu.com
URL: http://www.icept.org

Name: 2011 56th IEEE Holm Conference on Electrical Contacts (HOLM 2011)
Dates: September 11–14, 2011
Location: Minneapolis, MN USA
Contact: Deidre Zeigler
E-mail: d.zeigler@ieee.org
URL: http://www.ewh.ieee.org/soc/cpmt/tc1

Name: 2011 European Microelectronics and Packaging Conference (EMPC)
Dates: September 12–15, 2011
Location: Brighton, England
E-mail: conference@empc2011.com
URL: http://www.empc2011.com/

Name: 2011 17th Int'l Workshop on Thermal Investigations of ICs and Systems (THERMINIC 2011)
Dates: September 27–29, 2011
Location: Paris, France
Contact: Chantal Bénis-Morel
E-mail: chantal.benis@imag.fr
URL: http://cmp.imag.fr/conferences/therminic/therminic2011

Name: 2011 33nd Annual Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD 2011)
Dates: September 11–16, 2011
Location: Anaheim, CA USA
Contact: Lisa Pimpinella
E-mail: lpimpinella@esda.org
URL: http://www.esda.org/symposia.html

Name: 2011 IEEE/CPMT Workshop on Accelerated Stress Testing & Reliability (ASTR 2011)
Dates: October 12–14, 2011
Location: San Francisco, CA, USA
Contact: Ephraim Suhir, UC-Santa Cruz,
E-mail: suhire@aol.com
URL: www.ewh.ieee.org/soc/cpmt/tc7/ast2011/

Name: 2011 6th Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2011)
Dates: October 19–21, 2011
Location: Taipei, Taiwan
E-mail: service@impact.org.tw
URL: http://www.impact.org.tw/2011/General/

Name: 2011 20th IEEE Electrical Performance of Electronic Packaging (EPEP 2011)
Dates: October 23–26, 2011
Location: San Jose, CA USA
Contact: Mandy Wisehart
E-mail: epeps-admin@illinois.edu
URL: http://epeps.ece.illinois.edu/

Name: 2011 13th Electronics Packaging Technology Conference (EPTC 2011)
Dates: December 7–9, 2011
Location: Singapore
Contact: EPTC Secretariat
E-mail: eptc2011.secretariat@atenga.sg
URL: http://www.eptc-ieee.net/

IEEE Components, Packaging and Manufacturing Technology Society
Marsha Tickman, Executive Director
445 Hoes Lane
Piscataway, NJ 08854 USA

Getting the Most out of IEEE and CPMT Membership: eBooks

Did you know that IEEE members now have access to more than 220 eBooks from the IEEE Press collection through IEEE Xplore, including: handbooks; introductory and advanced texts; reference works; professional books.

Follow 3 simple steps:

1. Log in to IEEE Xplore http://www.ieeexplore.ieee.org/Xplore/guesthome.jsp using your IEEE Member Web account.
2. Under the "Browse" heading in the left-hand navigation, click on "Books".
3. Select the "Classics" tab from the top of the page. Under this tab you will find a listing of all the Free titles.

Here are a few examples of available books in pfd format: (more added every year)

1. *Lead-Free Electronics: iNEMI Projects Lead to Successful Manufacturing* by E. Bradley, C. Handwerker, J. Bath, R. Parker and R. Gedney; Publication Date: 2007
2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

For more information visit: http://www.ieee.org/membership_services/membership/products/ebookclassics.html