Components, Packaging, and Manufacturing Technology Society Newsletter

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President's Column....

Rolf Aschenbrenner
President, IEEE CPMT Society
Fraunhofer-Institut, Berlin, Germany
rolf.aschenbrenner@izm.fraunhofer.de

We are currently heading into another round of elections for CPMT's Board of Governors. This year, voters in Regions 1–7 and 9 (US, Canada and Central and South America) will elect four members-at-large, while Regions 8 (Europe, Middle East, Africa) and 10 (Asia, Pacific) will each elect one member-at-large. The elected representatives will join continuing members-at-large: eight in Regions 1–7 and 9 and two each in Regions 8 and 10. CPMT's Board of Governors serves as a vital part of our organizational structure by directly feeding your concerns and interests into CPMT policy and budgeting. Although the final slate of candidates is not quite finalized, I urge everyone to check the website for more information and, of course, to vote. We need as many members as possible participating to ensure that the allotted number of representatives for each region are elected and, thus, that our organizational structure reflects the geographic distribution of our membership.

Another major event in coming months will be the relaunch of CPMT website. As in our profession, Internet technologies and design conventions evolve rapidly, the time has come to update our online presence. The overhaul has been a large-scale project within the society for some time and is shaping up nicely. Our new site will make better use of recent web technologies, provide a comprehensive platform for our members and present the CPMT society to industry and the public-at-large in the best light possible. Stay tuned for more information…

Last but not least, I'd like to extend my congratulations to this year's five CPMT award winners: John Lau from the Industrial Technology Research Institute, Singapore, who received the Outstanding Sustained Technical Contribution Award; Xuejun Fan from Lamar University, USA, winner of the Exceptional Technical Achievement Award; Mark Brillhart from Cisco, who received the Electronics Manufacturing Technology Award; Muhannad Bakir from Georgia Institute of Technology¸ USA, who received the Outstanding Young Engineer Award and Paul Wesling, Santa Clara, CA, USA, who was recognized for his contribution to the Santa Clara CPMT chapter. Please see the full profile of the 2011 winners further on in the newsletter for more information about their individual contributions. We also cannot forget our former CPMT president Rao R. Tummala, who received the "2011 IEEE Components, Packaging and Manufacturing Technology Award" (also profiled in the newsletter) – I'd like to extend my congratulations on behalf of all of CPMT to you, Rao.

From bodies of work that grow slowly but steadily over time, to potentially game-changing flashes of inspiration, right through to dedicated efforts towards developing our society's programs and activities, the CPMT awards are an excellent means of acknowledging outstanding contributions to our profession. Nominations for CPMT's 2012 awards have already opened. Please visit our website at http://www.cpmt.org/awards/index.html to suggest members deserving of special recognition.

NEWSLETTER SUBMISSION DEADLINES:

1 November 2011
1 February 2012
1 May 2012
1 August 2012

Submit all material to nsltr-input@cpmt.org

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CPMT Society Newsletter

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TC-OPTO - Fiber Optics & Photonics:
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TC-SP - Systems Packaging:
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TC-Test - Electrical Test:
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Tony Mak
TC-WLP - Wafer Level Packaging:
Michael Toepper

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Membership: Eric Perfecto, perfecto@us.ibm.com
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Distinguished Lecturers

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Chapters and Student Branches

Refer to www.cpmt.org for CPMT Society Chapters and Student Branches list

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CPMT Members-Only Web
(www.cpmt.org/mem/)

Username: (see any printed
Password: copy for this info)

CPMT Society News....

Rao R. Tummala Receives 2011 IEEE Components, Packaging & Manufacturing Technology Award

The IEEE Components, Packaging and Manufacturing Technology Award, sponsored by the IEEE Components, Packaging and Manufacturing Technology Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies.

The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

The 2011 Award was present to Dr. Rao R. Tummala at the 61st Electronic Components and Technology Conference, June 2011.

Rao R. Tummala
Georgia Institute of Technology, Packaging Research Center, Atlanta, Georgia, USA

For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging

Rao R. Tummala is being recognized as the father of modern packaging innovations that have revolutionized microelectronics packaging. Dr. Tummala's pioneering inventions include the industry's first plasma display and the first ceramic and thin-film multichip packaging. He is regarded as the father of low-temperature, co-fired ceramic (LTCC) technology, an industry standard, and the father of the systems-on-package (SOP) concept as Moore's Law for system integration. His leadership made packaging an academic subject.

He was instrumental in the establishment of the first National Packaging Research Center in the United States for leading-edge research, cross-disciplinary education and global industry collaborations.

He authored the first reference, first undergraduate and first graduate textbooks that shaped the modern packaging landscape.

An IEEE Fellow, Dr. Tummala is an endowed chair professor and director of the 3D Systems Packaging Research Center at the Georgia Institute of Technology in Atlanta.

Dr. Tummala joins the following past recipients of this Award.

2010 – Herbert Reichl
"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

2009 – George G. Harman
"For achievements in wire bonding technologies."

2008 – Karl Puttlitz Sr. and Paul A. Totta
"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages"

2007 – Dimitry Grabbe
"For contributions to the fields of electrical/electronic connector technology, and development of multi-layer printed wiring boards."

2006 – C. P. Wong
"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005 – Yutaka Tsukada
"For pioneering contributions in micro-via technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004 – John W. Balde
"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www.ieee.org/awards.

Congratulations to 2011 CPMT Award Winners

The CPMT Society annually recognizes individuals for contributions to the profession through technical achievements, service to the industry and to the Society. The following individuals received their awards at the 61st Electronic Components and Technology Conference (ECTC), June 2011.

The **Outstanding Sustained Technical Contribution Award** is given to recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the CPMT Society. The 2011 recipient:

John Lau, Industrial Technology Research Institute, Singapore
For a decades-long record of developing and communicating packaging platform, material and process advancements through research and development leadership, publications and professional training.

The **Exceptional Technical Achievement Award** is given to recognize an individual, or group of individuals for exceptional technical achievement in the fields encompassed by the CPMT Society. The 2011 recipient:

Xuejun Fan, Lamar University, USA
For major contributions in the area of modeling and characterization of moisture-related reliability in IC packaging, including theoretical model development, validation, numerical implementation, test methodology development and design.

The **Electronics Manufacturing Technology Award** is given to recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society. The 2011 recipient:

Mark Brillhart, Cisco¸ USA
For developing manufacturing technologies and industry supply chain capabilities in the areas of high performance ASIC packaging, system in package, 3D and wafer level packaging of high speed memory and optics, and advanced coreless organic substrates for high reliability networking products.

The **Outstanding Young Engineer Award** is given to recognize outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation. The 2011 recipient:

Muhannad Bakir, Georgia Institute of Technology¸ USA
For contributions to the advancement of 3D electrical, optical and thermal interconnect and packaging technologies, and to the professional and publication areas of the CPMT Society.

The **Regional Contributions Award – Regions 1-7 and 9 (US, Canada and Latin America)** is given to recognize significant and outstanding leadership and contributions to the growth and impact of CPMT programs and activities at the Region level. The 2011 recipient:

Paul Wesling, Santa Clara, CA, USA
For over 35 years of continuous service to the CPMT Santa Clara Valley Chapter in numerous leadership and advisory roles, with a focus on technical/educational program development and passion for communications, that helped the Chapter grow, thrive and become a model within the CPMT Society and the IEEE.

For information on how to submit a nomination for the 2012 CPMT Awards, please see the related article in this Newsletter or go to http://www.cpmt.org/awards

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New IEEE CPMT Senior Members

The members listed below were recently elevated to the grade of Senior Member.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Individuals may apply for Senior Member grade online at: www.ieee.org/web/membership/senior-members/index.html

Ali, Hassan	Kao, C	Mathuna, Cian
Becker, Wiren	Kim, Namhoon	Mutnury, Bhyrav
Dang, Bing	Ma, Hongtao	Shah, Amip

CALL FOR NOMINATIONS FOR THE 2012 CPMT SOCIETY AWARDS

NOMINATIONS DUE BY JANUARY 31, 2012

The CPMT Society is full of highly talented professionals, and we have five awards to recognize those who have performed at an exceptional level. Do you have a friend or colleague who has made outstanding contributions to the technical fields within CPMT? Would you like him or her to receive recognition for these contributions? We would, too; you can make it happen by submitting a nomination today.

The Awards Committee is currently accepting nominations for the 2012 CPMT Awards. All nomination packages are due by January 31, 2012. Winners will be notified by March 31, 2012, and the awards will be presented at the 62nd Electronic Components and Technology Conference, May 31st–June 3rd 2011, in San Diego, California, USA. A current nomination form can be found on the CPMT web site under the Awards link at: http://www.cpmt.org/awards/. We look forward to receiving your nominations for any of the awards described below.

CPMT Society offers the following 5 awards for the purpose of recognizing outstanding service and contributions to the professional purposes of the CPMT Society.

1) **David Feldman Outstanding Contribution Award.** This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through executive or managerial directions.
   Prize: $2,500 and Certificate
   Basis for Judging: Contributions to the organization or enterprises connected with the field, to CPMT Chapter, Section or Board of Governors activities, and to the fields encompassed by the CPMT Society.
   Eligibility: Recipient must have been a member of IEEE and CPMT for the past five (5) years, including 2011.

2) **Outstanding Sustained Technical Contributions Award.** This award recognizes outstanding sustained and continuing technical contributions in fields encompassed by the CPMT Society.
   Prize: $2,500 and Certificate
   Basis for Judging: Technical contributions must be sustained and continuing over a period of at least five (5) and preferably 10 years. One major contribution will not qualify. Contributions must be documented by open literature (available to the public) publications such as papers, patents, books and reports.
   Eligibility: Must have been a member of the IEEE and CPMT Society for the past three (3) years, including 2011.

3) **Electronics Manufacturing Technology Award.** This award recognizes major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT Society.
   Prize: $2,500 and Certificate
   Basis for Judging: Contributions may include technical development of, or management (directing) of, major new electronic manufacturing processes, significantly increasing yield and/or reliability of established manufacturing processes, etc. Work in the management of CPMT conferences or its BoG may be contributory but not sufficient to receive the award.
   Eligibility: Membership in IEEE or the CPMT Society is not required.

4) **Exceptional Technical Achievement Award.** This award recognizes an individual, or a group (no more than three), for exceptional technical achievement in the fields encompassed by the CPMT Society.
   Prize: $2,500 and a Certificate.
   Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, beyond that achieved by most members. A single major contribution may qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in CPMT's field of interest. The technical contributions must be documented by open literature (available to the public) publications such as papers, patents, books, and reports. Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.
   Eligibility: Recipient(s) must have been a member of IEEE and CPMT for the past three (3) years, including 2011. There are no requirements for service to the IEEE or CPMT Society.

5) **Outstanding Young Engineer Award.** This award recognizes outstanding contributions to the fields encompassed by the CPMT Society through invention, technical development, publications, or new product implementation.
   Prize: $1,500 and Certificate plus one year free membership in CPMT with all CPMT Transactions.
   Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the CPMT Field of Interest. Contributions could include significant new product introduction or implementation of major new electronic manufacturing processes, significantly increasing yield and/or reliability of established manufacturing processes, etc, and may encompass management (directing). Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.
   Eligibility: Must have been a member of the IEEE and CPMT (member grade or above) for the past three (3) years, including 2011, and must be 35 years of age, or younger, on December 31st, 2011. Please provide Date of Birth (Month/Year) to ensure eligibility.

Guidelines for Nominators:

- Minimum **three** reference letters must be submitted in support of all nominations. Reference letters can be provided by IEEE/CPMT members and non-members.
- Past recipients of an award are not eligible to receive that same award. For list of past awardees, see the CPMT Society Home page (http://www.cpmt.org/awards).
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- It is the responsibility of the nominator to provide quality documentation to assist the Awards Committee in evaluating the candidate.
- Please send nominations to CPMT Society Director, Awards by e-mail or mail:

Patrick Thompson
Texas Instruments, Inc.
MS940, PO Box 655012
Dallas, TX 75265 USA
Phone: +1-214-567-0660
Email address: Patrick.thompson@ti.com

Notification of CPMT Society Bylaw Changes

In 2010, IEEE leadership, following legal advice, had requested that staff complete a review of the governing documents for those Societies with IEEE staff that provide support to Society activities. The purpose of this review was to ensure that all IEEE governing documents comply with the IEEE Constitution, Bylaws and Policies, all IEEE Human Resources policies, and other legal requirements.

Required changes after the review:

1) Removal of all sections of the Society Constitutions and Bylaws that relate to staffing.
2) Removal of all sections of the Society Constitutions and Bylaws that relate to volunteer supervision of IEEE staff.
3) Removal of all sections of the Society Constitutions and Bylaws that relate to volunteer committees with the functions of staff supervision, hiring, compensation and other HR-related functions.
4) Use only of the term "oversight" (and derivatives) when referring to staff and staff issues.

As a result, all IEEE Societies with staff were required to modify their governing documents to ensure that the IEEE approved standard wording is incorporated.

In response, the CPMT Board of Governors approved the following changes to the Society Bylaws at its June 2011 meeting.

DELETE (current wording):

Society Executive Office - Under the supervision of the Society Executive Director, the Executive Office functions to coordinate and carry-out the day-to-day operations, policies and procedures concerning all aspects of the Society's business. The Society President exercises oversight of the Executive Office in coordination with the IEEE Managing Director for Technical Activities. The Executive Office staff shall be paid staff of IEEE. Additions to staff shall be approved by the BoG.

ADD (standard wording required by IEEE):

Subject to compliance with all applicable IEEE Bylaws and Policies, the Society may create an Executive Office supported by IEEE staff. The Society's Executive Office functions to coordinate and carry-out the day-to-day operations, policies and procedures concerning all aspects of the Society's business. The Office also maintains corporate memory and provides ongoing and ad hoc management reports/documents. In addition, the Society's Executive Office serves as one of the Society's primary points of contact for both members and IEEE staff.

Subject to compliance with all applicable IEEE Bylaws and Policies, the Society may determine the budget for the Executive Office. The staff is hired by the IEEE and all conditions of employment will be based upon IEEE Bylaws, staff policies and practices and all applicable laws and regulations. Office organization, job descriptions, IEEE staff policies and employment practices are available from the IEEE Human Resources Department.

The Society Executive Director is the most senior position on the IEEE staff that supports the Society, and as such, he/she manages and develops, personally and through subordinate management staff, the paid IEEE staff members that support the Society's operations and activities. The Society Executive Director supports the Society President, officers and volunteer leadership to achieve the Society goals. This Society Executive Director reports through the Managing Director, Technical Activities, to the IEEE Executive Director.

In accordance with the CPMT Constitution, requiring publication of the changes in the Society Newsletter or Transactions, the changes will become effective 30 days following publication.

CPMT Distinguished Lecturer Dongkai Shangguan at BME

Dr. Dongkai Shangguan, Ph.D., MBA, IEEE Fellow, a distinguished lecturer of IEEE Components, Packaging and Manufacturing Technology Society visited the Budapest University of Technology and Economics on the 6th of May, 2011.

The IEEE-CPMT Hu&Ro (Hungary and Romania) Joint Chapter and The Department of Electronics Technology of BME hosted the lecture of Dr. Shangguan about Electronics Product Miniaturization and Reliability. The presentation reviewed advanced packaging and assembly technologies for miniaturization; and outlined the scope of development for complete assembly capability, including PCB design; solder alloy; process optimization; equipment technology; reliability, etc. Several critical reliability issues in lead-free solder interconnects were also discussed. It was also pointed out that miniaturization, functional densification and integration, along with environmental compliance, fast time to market, low cost and high reliability continue to represent the leading trend for electronics products.

After his presentation, a visit was organized for Dr. Shangguan by Prof. Gábor Harsányi, Prof. Gábor Stépán, Prof. Tibor Czigány and Prof. József Karger-Kocsis to the laboratories of the Department of Electronics Technology, the Department of Applied Mechanics and the Department of Polymer Engineering, respectively

Dr. Shangguan is currently Vice President with Flextronics, a leading EMS (Electronics Manufacture Service) provider, who has

four plants in Hungary and several others in the surrounding countries. Flextronics is also a gold level sponsor of BME.

Dr. Shangguan currently serves on the IEEE CPMT Society Board of Governors, on the IPC Board of Directors, on the first Board of Directors for the Solar Engineering & Manufacturing Association (SEMA), on the Advisory Board of the Sustainable Electronics Manufacturing (SEM) Working Group, and on several editorial/advisory boards of technical journals.

2011 CPMT Society Distinguished Lecturer Program

The CPMT Society Distinguished Lecturer (DL) program currently has 33 DL's covering key packaging technology areas. These 33 DL's are 'Fellow Caliber' members of our technical community, 24 are located in the US, 7 in Asia/Japan and 2 in Europe. The goal is to utilize DL's to give talks in various CPMT (co)-sponsored venues. In 2011, the focus has been to get a more even distribution between chapter and conference events funded. This year there have been 6 Chapter/Workshop Requests and 8 Conference Requests.

Anyone receiving DL assistance is expected to note that the presentation is, in part, supported by CPMT DL funding on either the front page or the last page of their presentation. This is considered a requirement for the receipt of future funding.

While the budget is limited tough decisions have to be made on which request will or will not be supported. The travel assistance is limited to a maximum of $1000 per request, and no more than 2 requests from the same DL. Typically the budget covers 12 to 14 events.

To schedule a Distinguished Lecturer, contact the Distinguished Lecturer directly or contact the Program Director, Kitty Pearsall, and CPMT VP of Education. (The DL him/herself should report all DL talks to Kitty Pearsall and Marsha Tickman – whether or not travel assistance was requested/granted – for our annual report.)

CPMT Chapter News....

Memorial Day to Fourth of July – The Birth Story of a New CPMT Chapter

Eric Perfecto, CPMT Chapter and Membership Director, interviews Sam Karikalan, the new CPMT Orange County Chapter Chair

Background: CPMT membership is growing; there is a real opportunity to organize new chapters to address the needs of local members by providing technical growth and networking.

Eric: What inspired you to organizing a CPMT chapter?

Sam: First of all, my sincere thanks to you, Eric, for giving me this opportunity to tell everyone this Birth Story of our new CPMT Chapter in Orange County, California.

The most important thing that inspired me to work on organizing this new CPMT Chapter is my personal experience of the benefits that regional technical meetings can bring to individual members. These local meetings are different from the annual conferences, in the sense that they are focused on one particular topic at a time, need only an hour or two of your time and do not need you to travel for enjoying the technical enrichment and networking benefits of CPMT. Also, these local meetings happen more frequently, which helps members to remain in touch with their community all the time.

While living in Arizona, until mid-2009, I had the opportunity to interact with the large CPMT community in the Phoenix area. The CPMT Phoenix Chapter and the IEEE Phoenix Section were very vibrant, with many meetings, workshops and banquets, and I had the honor of serving on the Executive Committees of both these great organizations, in several different capacities such as the Program Chair and the Publicity Chair. When I had to relocate to Orange County, California for work related reasons in 2009, the absence of a local CPMT chapter and its monthly technical meetings in Orange County area seemed to push me in a professional networking vacuum. This made me to start seriously thinking about forming a new chapter of CPMT in Orange County. I thought there might be many people in this area who might be feeling the same way that I did.

Eric: Why not just create an affiliate CPMT chapter to an existing IEEE Society chapter in Orange County?

Sam: The first thing that I did, with this chapter formation effort, was to obtain the list of current CPMT members in the Orange County area from Marsha Tickman, the Executive Director of CPMT. I was elated to see that we had four IEEE Fellows, four Life Members and three Senior Members on that list, which immediately boosted my confidence on the possibility of having our own Chapter. With a membership that is so well accomplished and with many semiconductor companies in the area with large

and small Package Engineering groups of their own, I never even thought of an affiliate chapter and started working straightaway on the petition for a separate CPMT chapter, here in Orange County. I always had the feeling that this Chapter has the potential to grow into a very big and active Chapter of CPMT and play an important role at the national and international level as well, for supporting CPMT's mission.

Eric: How far away was the nearest CPMT chapter, before the CPMT OC Chapter became a reality?

Sam: The nearest CPMT chapter for us was about 90 miles away in San Diego, CA. Driving to the meetings of that chapter every time might have been challenging and discouraging for those in the Orange County area.

Eric: Can you describe the process and issues that you encountered in certifying the new IEEE CPMT chapter?

Sam: Sure. As any chapter of a Technical Society of the IEEE is attached to a particular IEEE Section at the Regional level and is governed by the by-laws of that Section, we had to submit a petition to the Orange County Section of the IEEE and the IEEE Membership and Geographic Activities (MGA) Board on the formation of our IEEE CPMT OC Chapter. The following are the key milestones in this petition and approval process for us:

1) **Gather our members:** The petition (http://www.ieee.org/documents/chapter_petition.doc) to form a new CPMT Chapter needed to be signed by at least 12 members of CPMT Society, affiliated to the Orange County Section, with "Member" Grade or above. So, the first step for me was to send an e-mail to the existing CPMT membership in the OC Section, presenting the idea of starting our own Chapter and asking them to co-sign the petition. It may also help to ask around at one's work place in person and recruit new members, if needed, as this might expedite the process of reaching the magic number of 12.
2) **Petition paper work:** E-mails are accepted by the IEEE MGA as proof of signature on the petition. So, there is no need for every single petitioner to physically sign the petition form. Instead, an e-mail with the details such as the Member name, IEEE Member number, the IEEE Section name and the proposed IEEE Chapter's name, along with a statement such as "I, as a member of the above Society and Section, hereby petition for approval to form a Chapter in the Section indicated above", from a petitioner is sufficient. The full name of the petitioner and contact address needs to be added to that e-mail as a signature. All these e-mail signatures need to be recorded on the petition form, with a note such as "E-mail attached" in the "Signature" Column, along with the signatures that were physically obtained on the petition form, before submitting it to the local IEEE Section's Executive Committee for approval.
3) Once the local IEEE Section Executive Committee approves the petition, it is taken up by the IEEE MGA for verification of the signatures and submitted for approval by the respective Region Director of the IEEE and the President of the Technical Society.
4) Upon receiving all such approvals, the MGA Administration will communicate the formation of the new Chapter to the person identified as the "Organizer of the Chapter" on the petition form.

We were fortunate not to encounter any major issues in this entire process. Marsha Tickman, the Executive Director of the CPMT, was always there to guide us through, including bringing our petition to the attention of some of the key members of our community and asking for their signatures on the petition. Alvin Joseph, the IEEE OC Section Chair, was very supportive of our efforts on this Chapter formation, and helped us to move the petition through the Section's approval chain quickly. In your position as the CPMT Chapter and Membership Director, Eric, you were such a great inspiration and help as well, through this entire process.

Eric: Thanks, Sam. How long did the whole process take?

Sam: My first exploratory e-mail to our membership went out on the Friday before the Memorial Day Weekend this year. With support e-mails flowing in almost immediately in reply, we had 15 signatories for the petition by June 10th and we submitted our petition to the IEEE OC Section Executive Committee on the same day. In the mean time, the 61st ECTC in Lake Buena Vista, FL, also helped me to meet with Don Frye and Prof. Chin C Lee from UCI, my fellow petitioners, and other like-minded people in person and gather their support as well.

With the IEEE OC Section approval in our hand on June 13th, Marsha Tickman forwarded the paperwork to the IEEE MGA on the same day. After the signature verifications were done, Joe Hale, the Geographic Unit Support Administrator at the MGA, forwarded the formation request to Edward Perkins, the Region 6 Director of the IEEE, and Rolf Aschenbrenner, the CPMT President, on June 21st. Edward and Rolf, were kind to give their approvals quickly, such that we received the note on the final approval of this new chapter from Cecilia Jankowski, the Managing Director of the IEEE MGA, on June 29th. The effective date of the formation of our Chapter was June 24, 2011.

So, everything on this new Chapter formation process unfolded so quickly and the approval process was executed so efficiently at the IEEE OC Section, CPMT and the MGA, such that the whole process took only about five weeks. What started by the Memorial Day Weekend all ended in a Very Happy note for all of us at the IEEE CPMT OC Chapter, by the Fourth of July Weekend.

Eric: What support have you received from CPMT and the IEEE section?

Sam: Besides being the guiding force through the formation phase of our Chapter, the CPMT and the IEEE OC Section have also promised seed funding to our baby chapter, to get started with our technical activities. With their support, we already have had two administrative meetings, elected our own Executive Committee, have an Activity Plan in place and are ready to start with our monthly Technical Meeting series in September this year. All this wouldn't have been possible without the strong support that we received from the CPMT and the IEEE OC Section.

Eric: Do you have a chapter web page?

Sam: Yes, we do. Our URL is http://sites.ieee.org/ocs-cpmt. This site is still evolving and our Publicity Chair is working hard to keep this site up to date and informative. We also have a LinkedIn

Group, called "IEEE CPMT OC Chapter. (http://www.linkedin.com/groups?gid=3996387&trk=hb_side_g), where we invite non-IEEE members also to join and stay informed on our activities.

Eric: Are you planning to take advantage of the Distinguished Lecture program?

Sam: Yes. Thanks to you, Eric, for introducing us to Kitty Pearsall, the Distinguished Lecture (DL) Program Coordinator and VP of Education at CPMT. The DL Program (http://www.cpmt.org/education/dl.html) has an impressive list of experts who can be invited by us for technical talks at our meetings and their travel expenses may be covered by the CPMT, if needed. This is a great service by the CPMT to the local chapters and we will definitely take advantage of this program.

IEEE CPMT OC Chapter Executive Committee: From Left to Right: Jianjun Li (Secretary), Mehdi Saeidi (Technical Program Co-chair), Wei Koh (Technical Program Chair), Don Frye (Vice-Chair), Tim Chaudhry (Treasurer), Sam Karikalan (Chair), Larry Williams (Workshop Chair), Michael Alderete (Membership Chair) and Jianfeng Xu (Publicity Chair).

Eric: Any other comments that can help regional members that are considering establishing a new CPMT chapter?

Sam: The new chapter formation effort was a very pleasant experience for us, due to the efficiency and professionalism with which the petition process was handled at the IEEE.

To those of my colleagues at CPMT Society worldwide, who are thinking about starting their own chapters at the local level, I would like to say "Congrats! You have taken the right first step in making full use of your IEEE membership and bringing all its benefits to you and fellow members in your region."

For those who are wondering on how to gather the 12 signatures needed for the petition, my recommendation would be "Go out and talk or e-mail to your fellow members in your section. You will be surprised to see there are so many of them who are feeling the same way as you do on the lack of technical activities at the local level".

My final advice would be "Feel free to ask for help from the CPMT and your local Section. They will be very glad to support in whatever way they can".

I also have a request to all of them and all the Chapters that already exist. Our IEEE CPMT Orange County Chapter needs your help, to keep our Technical Program active and vibrant. Kindly contact me at samkarikalan@ieee.org, if you have any advice, feedback or proposals for joint activities. We are also looking for experts to speak at our technical meetings. So, if you happen to be in the Orange County, California area or in the Greater Los Angeles area, and have the time to visit us, please let me know. We will invite you for a technical talk to our membership.

Eric: Thank you for agreeing to this interview - to me it shows the power of one person.

Sam: Thanks for the kind words, Eric. I would rather call this the power of team work. I was fortunate to have the immediate support of my fellow petitioners and I would like to recognize them individually in this interview. Thanks to Mehdi Saeidi, Pen Jin, Jianjun Li, Fan Yeung, Tim Chaudhry (all from Broadcom), Christoph Luechinger (K&S), Chuck Hirbour (Technic), Robert Warren (Conexant), Ralph W. Farrington (RWF Consulting), Jianfeng Xu (International Rectifier), Prof. Chin C Lee, Prof. Frank G. Shi (both from UCI), Wei Koh (Pacrim Technologies) and Don Frye (Henkel) for taking the initiative to sign the petition and be the founding members of our Chapter.

I am also grateful to the Executive Management of my company, Broadcom Corporation, for their kind support to our Chapter and their approval to use the company premises for our meetings.

Finally, I am blessed to have a wonderful team at our Executive Committee which, I believe, can pull off great feats together.

Thanks to you, again, for the opportunity to tell everyone our story!

Publication News....

Have You Read Them? The Most Downloaded CPMT Transactions Papers

What might you be missing in the CPMT literature? Following is a list of most downloaded papers in July 2011. Subscribers can access these and other papers on IEEE Xplore.

From the *Transactions on Components, Packaging and Manufacturing Technology:*

Modeling and Analysis of Through-Silicon Via (TSV) Noise Coupling and Suppression Using a Guard Ring

Jonghyun Cho; Eakhwan Song; Kihyun Yoon; Jun So Pak; Joohee Kim; Woojin Lee; Taigon Song; Kiyeong Kim; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Minsuk Suh; Kwangyoo Byun; Joungho Kim; **Issue Date:** Feb. 2011 Page(s): 220–233

In three-dimensional integrated circuit (3D-IC) systems that use through-silicon via (TSV) technology, a significant design consideration is the coupling noise to or from a TSV. It is important to estimate the TSV noise transfer function and manage the noise-tolerance budget in the design of a reliable 3D-IC system. In this paper, a TSV noise coupling model is proposed based on a three-dimensional transmission line matrix method (3D-TLM). Using the proposed TSV noise coupling model, the noise transfer functions from TSV to TSV and TSV to the active circuit can be precisely estimated in complicated 3D structures, including TSVs, active circuits, and shielding structures such as guard rings. To validate the proposed model, a test vehicle was fabricated using the Hynix via-last TSV process. The proposed model was successfully verified by frequency- and time-domain measurements. Additionally, a noise isolation technique in 3D-IC using a guard ring structure is proposed. The proposed noise isolation technique was also experimentally demonstrated; it provided −17 dB and −10 dB of noise isolation between the TSV and an active circuit at 100 MHz and 1 GHz, respectively.

PDN Impedance Modeling and Analysis of 3D TSV IC by Using Proposed P/G TSV Array Model Based on Separated P/G TSV and Chip-PDN Models

Jun So Pak; Joohee Kim; Jonghyun Cho; Kiyeong Kim; Taigon Song; Seungyoung Ahn; Junho Lee; Hyungdong Lee; Kunwoo Park; Joungho Kim; **Issue Date:** Feb. 2011 Page(s): 208–219

The impedance of a power-distribution network (PDN) in three-dimensionally stacked chips with multiple through-silicon-via (TSV) connections (a 3D TSV IC) was modeled and analyzed using a power/ground (P/G) TSV array model based on separated P/G TSV and chip-PDN models at frequencies up to 20 GHz. The proposed modeling and analysis methods for the P/G TSV and chip-PDN are fundamental for estimating the PDN impedances of 3D TSV ICs because they are composed of several chip-PDNs and several thousands of P/G TSV connections. Using the proposed P/G TSV array model, we obtained very efficient analyses and estimations of 3D TSV IC PDNs, including the effects of TSV inductance and multiple-TSV inductance, depending on P/G TSV arrangement and the number of stacked chip-PDNs of a 3D TSV IC PDN. Inductances related to TSVs, combined with chip-PDN inductance and capacitance, created high upper peaks of PDN impedance, near 1 GHz. Additionally, the P/G TSV array produced various TSV array inductance effects on stacked chip-PDN impedance, according to their arrangement, and induced high PDN impedance, over 10 GHz.

High-Frequency Scalable Electrical Model and Analysis of a Through Silicon Via (TSV)

Joohee Kim; Jun So Pak; Jonghyun Cho; Eakhwan Song; Jeonghyeon Cho; Heegon Kim; Taigon Song; Junho Lee; Hyungdong Lee; Kunwoo Park; Seungtaek Yang; Min-Suk Suh; Kwang-Yoo Byun; Joungho Kim; **Issue Date:** Feb 2011 Page(s): 181–195

We propose a high-frequency scalable electrical model of a through silicon via (TSV). The proposed model includes not only the TSV, but also the bump and the redistribution layer (RDL), which are additional components when using TSVs for 3-D integrated circuit (IC) design. The proposed model is developed with analytic *RLGC* equations derived from the physical configuration. Each analytic equation is proposed as a function of design parameters of the TSV, bump, and RDL, and is therefore, scalable. The scalability of the proposed model is verified by simulation from the 3-D field solver with parameter variations, such as TSV diameter, pitch between TSVs, and TSV height. The proposed model is experimentally validated through measurements up to 20 GHz with fabricated test vehicles of a TSV channel, which includes TSVs, bumps, and RDLs. Based on the proposed scalable model, we analyze the electrical behaviors of a TSV channel with design parameter variations in the frequency domain. According to the frequency-domain analysis, the capacitive effect of a TSV is dominant under 2 GHz. On the other hand, as frequency increases over 2 GHz, the inductive effect from the RDLs becomes significant. The frequency dependent loss of a TSV channel, which is capacitive and resistive, is also analyzed in the time domain by eye-diagram measurements. Due to the frequency dependent loss, the voltage and timing margins decrease as the data rate increases.

Design, Modeling, and Evaluation of a Multiband MIMO/ Diversity Antenna System for Small Wireless Mobile Terminals

Qinjiang Rao Wilson, K. P.; **Issue Date:** March 2011 Page(s): 410–419

A new multiband diversity antenna is presented, which is suitable for multiband diversity and multiple-input multiple-output antenna systems for small wireless mobile terminals. The antenna consists of two branches of folded monopoles, at least one of which is terminated with a rectangular patch. By slightly tuning the width of the patch, the antenna can simultaneously achieve a flexible frequency ratio and a desired bandwidth. An example design is presented for most application bands, from 890 MHz through

6 GHz, which operates in a real-world cellular phone environment, including near-field interactions with other phone components and a model of a human head (the SAM phantom). The simulated and experimental results, including S-parameters, radiation patterns, signal correlations and mean effective gain, have validated the proposed antenna design as useful for compact mobile devices.

Low Phase Noise and Low Power Consumption VCOs Using CMOS and IPD Technologies

Yuan-Chia Hsu; Hwann-Kaeo Chiou; Hsien-Ku Chen; Ta-Yeh Lin; Da-Chiang Chang; Ying-Zong Juang; **Issue Date:** May 2011 Page(s) 673–680

This paper presents two voltage controlled oscillators (VCOs) operating at 5.42 and 5.76 GHz implemented in 0.18-μm complementary metal-oxide semiconductor (CMOS) technology with integrated passive device (IPD) inductors. One IPD inductor was stacked on the top of the active region of the 5.76-GHz VCO chip, whereas the other IPD inductor was placed on the top of the 5.42-GHz VCO CMOS chip but far from the its active region. The high-quality IPD inductors reduce the phase noise of the VCOs. The measurements of the two VCOs indicate the same phase noise of −120 dBc/Hz at 1 MHz offset frequency. These results demonstrate a 6-dB improvement compared to the VCO using an on-chip inductor. This paper also presents the effect of the coupling between the IPD inductor and the active region of the chip on the phase noise performance.

From the *Transactions on Components and Packaging Technologies:*

Dynamic Lithium-ion Battery Model for System Simulation

Lijun Gao; Shengyi Liu; Dougal, R. A.; **Issue Date:** Sep. 2002 Page(s): 495–505

Presents here a complete dynamic model of a lithium ion battery that is suitable for virtual-prototyping of portable battery-powered systems. The model accounts for nonlinear equilibrium potentials, rate- and temperature-dependencies, thermal effects and response to transient power demand. The model is based on publicly available data such as the manufacturers' data sheets. The Sony US18650 is used as an example. The model output agrees both with manufacturer's data and with experimental results. The model can be easily modified to fit data from different batteries and can be extended for wide dynamic ranges of different temperatures and current rates.

Power and Life Extension of Battery-ultracapacitor Hybrids

Dougal, R. A. Liu, S. White, R. E.; **Issue Date:** Mar. 2002 Page(s): 120–131

The performance of a battery-ultracapacitor hybrid power source under pulsed load conditions is analytically described using simplified models. We show that peak power can be greatly enhanced, internal losses can be considerably reduced, and that discharge life of the battery is extended. Greatest benefits are seen when the load pulse rate is higher than the system eigenfrequency and when the pulse duty is small. Actual benefits are substantial; adding a 23 F ultracapacitor bank (3 × 7 PC10 ultracapacitors) in parallel with a typical Li-ion battery of 7.2 V and 1.35 A hr capacity can boost the peak power capacity by 5 times and reduce the power loss by 74%, while minimally impacting system volume and weight, for pulsed loads of 5 A, 1 Hz repetition rate, and 10% duty.

From the *Transactions on Advanced Packaging:*

Noise Isolation in Mixed-Signal Systems Using Alternating Impedance Electromagnetic Bandgap (AI-EBG) Structure-Based Power Distribution Network (PDN)

Jinwoo Choi Govind, V. Swaminathan, M. Bharath, K.; **Issue Date:** Feb. 2010 Page(s): 2–12

This paper presents efficient noise isolation and suppression method in mixed-signal systems using alternating impedance electromagnetic bandgap (AI-EBG) structure-based power distribution network (PDN). Currently, split planes are used for isolation in mixed-signal systems for isolating sensitive RF/analog circuits from noisy digital circuits. However, split planes show good isolation only at low frequencies due to electromagnetic coupling through the gap. The AI-EBG structure-based PDN presented in this paper provides excellent isolation (−80 dB ~ −100 dB) in the frequency range of interest by suppressing almost all possible electromagnetic modes. The AI-EBG structure has been integrated into a mixed-signal test vehicle to demonstrate the isolation level achievable. The ability of the AI-EBG structure to suppress switching noise has been quantified in this paper. The AI-EBG structure provided greater than 100 dB of isolation in passive S-parameter measurement and suppressed in-band noise down to −88 dBm of isolation in a functional test.

Defect Detection of Flip Chip Solder Bumps With Wavelet Analysis of Laser Ultrasound Signals

Jin Yang Ume, I. C. Lizheng Zhang; **Issue Date:** Feb. 2010 Page(s): 19–29

Microelectronics packaging technology has evolved from through-hole and bulk configuration to surface-mount and small-profile ones. In surface mount packaging, such as flip chips, chip scale packages, and ball grid arrays, chips/packages are attached to the substrates/printed wiring board (PWB) using solder bump interconnections. Solder bumps hidden between the chips/packages and the substrate/board are no longer visible for inspection. A novel solder bump inspection system has been developed using laser ultrasound and interferometer techniques. This system has been successfully applied to detect solder bump defects including missing, misaligned, open, and cracked solder bumps in flip chip packages, chip scale packages and land grid arrays. The system uses a pulsed Nd:YAG laser to induce ultrasound in the thermoelastic regime and the transient out-of-plane displacement response in nanometer scale on the package surface is measured using the interferometer technique. In this paper, wavelet analysis of laser ultrasound signals is presented and compared to previous signal processing methods, such as error ratio and correlation coefficient. The results show that wavelet analysis increases measurement sensitivity for inspecting solder bumps in electronic packages. Laser ultrasound inspection results are also compared to X-ray results. In particular, this paper discusses defect detection for a 6.35 mm ?? 6.35 mm ?? 0.6 mm PB18 flip chip package and flip chip package (??SiMAF??) with 24 lead-free solder bumps. These two types of flip chip specimens are both nonunderfilled.

From the *Transactions on Electronics Packaging Manufacturing:*

Acid Decapsulation of Epoxy Molded IC Packages With Copper Wire Bonds

Murali, S. Srikanth, N.; **Issue Date:** July 2006 Page(s): 179–183

Epoxy molded IC packages with copper wire bonds are decapsulated using mixtures of concentrated sulfuric acid (20%) and fuming nitric acid in an automatic decapping unit and, observed with minimal corrosion of copper wires (0.8-6 mil sizes) and bond interfaces. To attain maximum cross-linking of the molded epoxies, the post mold cured packages (175 °C for 4 h) were further, aged at high temperature of 150 °C for 1000 h. These packages are decapsulated using mixtures of higher ratio of concentrated sulfuric acid (40%) along with fuming nitric acid. The shear strength of copper wire bonds with 1 mil (25 mum) diameter of the decapsulated unit is higher than 5.5 gf/mil^2. The present study shows copper stitch bonds to Au, Cu, Pd, and Sn alloy plated surfaces are less affected on decapping, with a few grams of breaking load on stitch pull test, while stitch bonds on silver plated surfaces reveal lifting of wire bonds on decapping.

Printed circuit board recycling: a state-of-the-art survey

Jianzhi Li Shrivastava, P. Zong Gao Hong-Chao Zhang; **Issue Date:** Jan. 2004 Page(s): 33–42

This survey is done with an intention of providing a clear and comprehensive review of current practices and recent developments in the area of printed circuit board (PCB) recycling. The aim of this paper is to be a reference for research and implementation for the PCB recycling process. Original information is collected from the companies engaged in the PCB recycling industry and articles published after 1990. The paper gives an overview of the PCB structure, material composition and different recycling processes.

Conference News....

61st 2011 Electronic Components and Technology Conference (ECTC): had an outstanding conference

The 61st ECTC in Lake Buena Vista, FL, USA, was a spectacular year with more than 621 abstracts received matching the abstract submission record of 2008. Of the abstracts submitted 51% were from educational institutions, 38% from corporations, and 11% from research institutes. With 342 technical papers presented in 36 oral and 5 poster sessions including student posters, ECTC continues to be the prime technical conference in the electronic packaging industry. This year, the Executive Committee formed a 3D/TSV Work Group led by John Knickerbocker of IBM and comprised of members from all subcommittees to create 8 TSV-related sessions that would be co-sponsored by various subcommittees. This decision helped to consolidate all the TSV abstracts into topical sessions like 3D Interconnections, Integration, Applications, Materials, and Manufacturing. The 3D sessions were the highest attended with over 200 attendees per session.

With over 1000 attendees (compared to 844 in 2010), the semiconductor industry proved to be in a strong year. The 386 (compared to 345 in 2010) Professional Development Course (PDC) attendees, 61 exhibitors, and 26 sponsors were further proof of the strength of ECTC as a premier technical packaging conference. The conference also included luncheons, raffle drawings, evening receptions, and best paper awards.

In addition to technical sessions, there were invited speakers at four additional sessions:

- ECTC Panel Discussion chaired by Rolf Aschenbrenner of Fraunhofer IZM and co-chaired by Keyun Bi of the Electronic Manufacturing and Packaging Technology Society of China,
- Plenary Session chaired by Henning Braunisch of Intel,
- CPMT Seminar chaired by Kishio Yokouchi of Fujitsu Interconnect Technologies
- Special session on “Impact of manufacturing limitations on electronic package performance and reliability” on Tuesday morning chaired by Lei Shan of IBM.

On Tuesday, 386 attendees attended 16 professional development courses (PDCs). The courses were organized by the PDC Committee chaired by Kitty Pearsall of IBM. .The ITRS Assemblies and Packaging Technology Committee meeting took place in parallel to PDCs.

In the evening, students attended the ECTC Student reception hosted by Eric Perfecto of IBM, where they had an opportunity to learn about how the technical subcommittees work to select the abstracts.

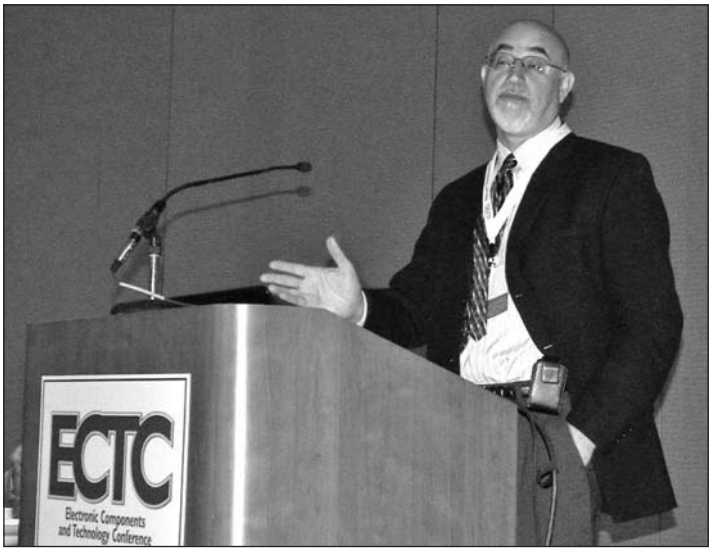
Session chairs and speakers, on the other hand, got together at the General Chair’s Speakers Reception.

At night, ECTC Panel Discussion on “ECTC Spotlight on China” chaired by Rolf Aschenbrenner of Fraunhofer IZM attracted a lot of attention. As Chinese industry has been growing very fast in electronic products manufacturing and has become the major consumer of integrated circuits products, the panel session of the ECTC 2011 focused upon the development of the packaging industry in China. Ed Pausa presented the latest economic data from PricewaterhouseCoopers while Ricky Lee’s presentation was concentrated on the R&D development in China and Bill Chen documented the point of view of a US based industry enterprise with strong business relations in China. The two Chinese panelists,

ECTC Spotlight on China Panel.

Eric Perfecto IBM, instructing on Flip Chip Fabrication and Interconnection.


ECTC Program Chair Wolfgang Sauter, IBM at Speakers Breakfast.



Nasser Grayeli, Intel – Speaking at luncheon.

Inside the Technology Corner.

Plenary Session: Power Efficiency Challenges and Solutions.

Rao Tummala (center) receiving award from CPMT President Rolf Aschenbrenner (right) and Past CPMT President William Chen (left).

Bill Li and Wenhui Zhu, described the state-of-the-art of the Chinese electronic manufacturing industry.

Technical sessions started on Wednesday, and ran through Friday, 8:00 AM to 5:00 PM every day. Speakers and session chairs met at breakfast to prepare for the sessions.

Dr. Nasser Grayeli, Intel Vice President of the Technology and Manufacturing Group and Director of Intel's Corporate Quality Network spoke on the challenges and opportunities ahead at the ECTC Luncheon. His presentation is posted at the ECTC web site (www.ectc.net).

In the evening, the exhibitor reception provided another opportunity for networking and exchanging information among the conference attendees.

ECTC General Chair Rajen Dias of Intel, hosted the program subcommittee chairs and assistant chairs in his suite and thanked them for their leadership in selecting the 342 technical papers out of 621 abstracts which matched the abstract submission record from 3 years ago.

In the evening, a Plenary Session "Power Efficiency Challenges and Solutions: From Outer Space to Inside the Human Body" was held, chaired by Henning Braunisch of Intel. The power efficiency theme was highlighted in the areas of space exploration (Greg Cardell, JPL), supercomputing (Hans Jacobson, IBM), data centers (Randy Mooney, Intel), consumer electronics (Raj Master, Microsoft), and medical implants (Sayfe Kiaei, Arizona State).

The CPMT Society presented its 2011awards at the Thursday luncheon. Rao Tummala of Georgia Institute of Technology, a leader in packaging research worldwide, was among the ones that were honored for their contributions to the industry. He received 2011 IEEE CPMT Award. Also, CPMT ECTC Sustained Contribution awards were presented to ECTC volunteers such as Joe Soucy and Harry K. Charles who have served 25 years and Steve Bezuk, Sharad Bhatt, Swapan Bhattacharya, Steve Dvorak, Mahadevan Iyer, Quinn Tong, Dongji Xie, and Charles Zhang who have served 10 years.

Sixty-one exhibitors took part in the Technology Corner Exhibit which continued through Thursday. Ten exhibitors were new for this year.

In addition to technical sessions that ran throughout the day, the 62nd ECTC Program Committee chaired by the 62nd ECTC Program Chair Senol Pekin met to prepare for 2012, where CPMT Representative C. P. Wong announced that Dr. Beth Keser of Qualcomm will serve as the Assistant Program Chair in 2012.

Thursday evening's Gala Reception was held outside at the Lake Terrace at the Swan. The weather was beautiful and the presenters, attendees, and conference volunteers had a wonderful time

ECTC General Chair Rajen Das (standing, center).


Chris Bower, Semprius - winner of "Introduction to System-on-Package," written and donated by R.Tummala.

discussing the success of the conference while eating good food (and desserts).

On Friday, Technical sessions continued till 5 PM. At the luncheon, General Chair Rajen Dias of Intel received the ECTC General Chair award from CPMT Representative C. P. Wong.

Conference attendees never feel sad at the last day of the conference thanks to the raffle drawings announced by ECTC Treasurer Tom Reynolds at the luncheon.

The First Call for Papers for 62nd ECTC is already out and can be found at www.ectc.net. You are invited to submit an abstract by October 10, 2011. In addition to abstracts for papers, proposals are solicited from individuals interested in teaching educational professional development courses.

See you at the 62nd ECTC in San Diego, CA next year!

2011 IEEE Semiconductor Wafer Test Workshop

Submitted by Jerry Broz, Ph.D., General Chair of IEEE SW Test and IEEE Senior Member

San Diego, CA: Wafer level test and probe technologists from around the world met in San Diego, CA, from June 12 to 15, 2011 for 21th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) at the Rancho Bernardo Inn in San Diego, CA. This annual IEEE / CPMT sponsored workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. SW Test 2011 began with a Sunday tutorial from Intel Corporation on the basics of statistical analysis with applicability to wafer level sort and data analysis. Starting Monday morning, the next three days were filled with a broad technical program; 5-hours of supplier exhibits (which did not compete with the technical sessions), and a San Diego Safari Park Social Networking Event.

SW Test 2011 had a total of 305 attendees from 15 countries with 30% of the attendees from outside the US to make the 2011 Workshop a truly global gathering of leading probe technologists. As always, there was a great mix of end-users (~31%) and suppliers / vendors (~69%) that were in attendance during the three day event. This unique workshop provides for plenty of time for informal interaction to discuss problems and promotes a friendly networking environment between colleagues as well as new attendees.

On Sunday night, Dr. William Chen, Sr. Advisor at ASE Group and former President of CPMT, made a thought provoking Keynote Presentation entitled, "*From Backend to Front End*".

Dr. William Chen began with a perspective into device packaging / assembly development that will likely affect wafer level test technologies. He reminded the attendees that Moore's Law is NOT a Law of Nature; it is however, an "expectation of continuity for innovation and invention" and a "promise of innovation and creativity for the semiconductor industry".

Dr. Chen discussed that overall society life experience improvements have been achieved through key product cycles within computing (personal computing), communication (wireless and wired), information (virtual sociality), and life sciences (medical and biotechnologies).

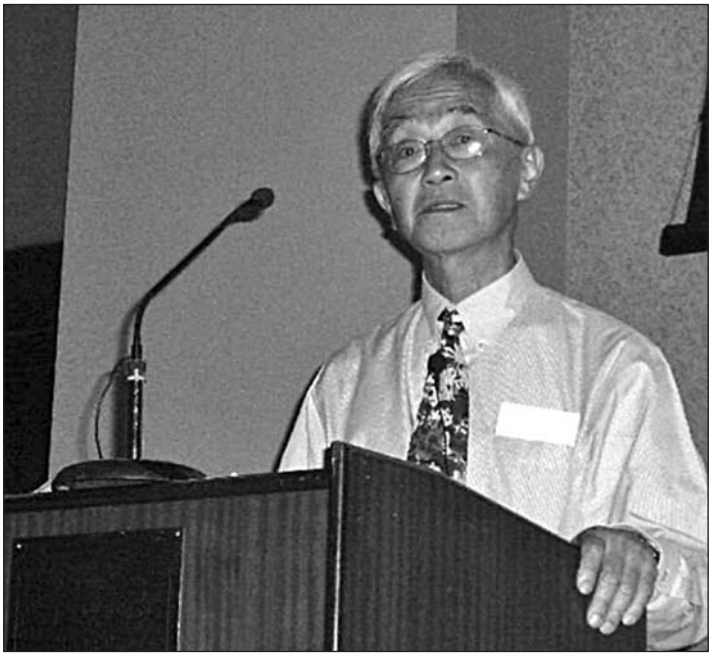
The changing landscape for packaging technologies to support future product life cycles will be driven by the critical integration of an increasing number of semiconductor device types within various electronics. According to Dr. Chen, the concepts of "More Moore" and "More than Moore" are the major trends that are currently driving semiconductor devices and packaging developments and architecture innovation.

"More Moore" can be described by continued shrinking of physical feature sizes of the digital functionalities in order to improve density and performance. It is, however, necessary to move past "More Moore", which works well for the digital world, but not for interfacing with the actual physical world. The "More-than-Moore" approach allows for the non-digital functionalities to

migrate from the system board-level into the package (SiP) or onto the chip (SoC). Incorporation of such functionalities does not scale according to "Moore's Law", but does have potential to provide substantial value to the end user in different ways.

In his opinion, Dr. Chen believes that one of the important trends in packaging includes the incorporation of system level integration through System in Package (SiP). This technology enables equivalent scaling through functional diversification of embedded active and passive components as well as integration of more functionality. The advent of 3D packaging will provide a fundamental paradigm change that will be based upon technology and infrastructure from flip chip and wafer level packaging and test. The speed and power advantages of 3D-TSV allow for a faster circuit speed with reduced power consumption. As an example, standby power can be reduced by 75% when compared to PoP and MCP packages and with a smaller physical size.

Dr. Chen discussed that with current practices, wafer level testing test can clearly identify whether a semiconductor die is "probably good" prior to packaging. Backend test can then determine whether the device is still good after packaging. However, with the advent of 3D packaging and stacked die complexity, it becomes more and more difficult to properly determine if the die has "gone bad" or if the packaging has created a "defective device". Dr. Chen concluded that in our industry the backend (wafer test and package test) will be coming to the forefront of the technology supply chain. He then challenged the wafer test community at SW Test to further promote academic participation, "Without academic participation, where is the future knowledge and innovation for needed for wafer test and packaging going to come from?" To help support academic attendance, Dr. Jerry Broz worked closely with the IEEE Foundation in 2010 for the establishment of the William R. Mann Student Travel Grant for eligible student that are IEEE members.



Dr. William Chen
Sr. Advisor, ASE Group
SW Test 2011 Keynote Presentation

The complete version of Dr William Chen's keynote presentation is available for download on the SW Test website (http://www.swtest.org).

On Monday morning, Dr. Jerry Broz, SW Test General Chair, welcomed the attendees to the 21st Annual SW Test Workshop. Dr. Broz reviewed a number of SIA statistics as well as iSuppli information which showed a general rebound in the semiconductor industry. Not surprisingly, the year of semiconductor sector recovery was reflected in the VLSI Research probe card market overview that had been released in May, 2011. The report showed that total probe card revenue was up in 2010, a gain of ~28% (from ~$750M in 2009 to ~$1040M in 2010). The top three revenue generating probe card suppliers remained unchanged – (1) FormFactor; (2) Micronics Japan (MJC), and (3) Japan Electronic Materials (JEM) – and all three companies experienced increased revenues. Of the top three, MJC was reported to have the greatest percentage of growth.

After the Chairman's Welcome to Attendees, the technical program kicked-off and the excellent podium presentations covered various facets of the wafer test process from *Critical Probe Challenges and Cost of Ownership* to *Methods and Strategies for Addressing Extreme Current Challenges.*

Individual highlights from the program included a discussion of new probe technologies for various bump materials by Amy Leong (MicroProbe). Steven Ortiz (Avago Technologies) discussed probe to pad placement error correction for wafer level S-Parameter measurements. Gert Hohenwarter, Ph.D., (Gatewave Northern) outlined that power delivery network analysis and made a case for true 3D simulations. Wafer probing on fine-pitch micro-bumps for 2.5D- and 3D-SICs was presented by Erik Jan Marinissen, Ph.D., (IMEC Research Institute – Belgium). The importance of a WSP (wafer socket probe) for flip chip applications was detailed by Brandon Mair (Texas Instruments). Marc Knox (IBM) discussed his team's efforts for the development of a flexible and efficient chip thermal imaging capability. Technical hurdles experienced for in the electromechanical design of spring pin based WLCSP contact engine and its effect on signal fidelity were addressed by Mike Fredd (Cascade Microtech). Innovations for wafer map and pad stepping to reduce test time were reviewed by Kevin Fredriksen (SPA GmbH – Germany). Takashi Sugiyama (Hitachi Chemical Co. Ltd. – Japan) discussed high density and high speed approach for probe card PCBs. Doron Avidar (Micron – Israel) introduced the concept of "Ghosting" for touchdown reduction using alternate site sharing. Seenew Lai (MPI – Taiwan) detailed the complex challenges associated with development of high bandwidth (>2.5 Gbps) and fine pitch ($<30\ \mu$m) cantilever probe cards.

Overall, the technical program had 32 podium presentations with 55% from suppliers, 18% from semiconductor manufacturers, and 27% collaborative presentations from both manufacturers and suppliers. All the presentations from SW Test 2011 as well as previous workshops (1993 to 2010) are available at the SW Test website (http://www.swtest.org).

The committee recognized the best podium presentations and Rey Rincon (Technical Program Chair) awarded the authors …

- Best Presentations *(awarded jointly)*:
  1) *Identification, Analysis, and Control of High Temperature on Wafer Test Process*

IEEE SW Test Committee 2011
Front: Fred Taber, Jan Martens, Jerry Broz, Ph.D. (General Chair), Rey Rincon (Program Chair), John Caldwell; Middle: Mark Ojeda, Amy Leong, Roy Swart, Tatsuo Inoue, Darren James, Patrick Mui; Back: Boyd Daniels, Michael Huebner, Ph.D., Gunther Boehm.

Marcel BLEYL and Jan MARTENS (NXP Semiconductors – Germany)
Darren JAMES (Rudolph Technologies – USA)

2) *Contact Formation in Wafer Probing: Fritting, Breakdown, Damage and Conduction*
Jörg SEEKAMP and Gunther BöHM (Feinmetall – Germany)
Jan MARTENS (NXP Semiconductors)
Marcel MITTAG (Fraunhofer Institut für Werkstoffmechanik – Germany)

- Best Data Presented
  Use of Harsh Wafer Probing to Evaluate Various Bond Pad Structures
  Stevan HUNTER, Troy RUUD, Bryce RASMUSSEN and Vail MCBRIDE (ON Semiconductor – USA)
- Most "Inspirational" Presentation
  Novel Carbonaceous Film with High Electrical Conductivity and Super High Hardness for Semiconductor Test Probes
  Teruyuki KITAGAWA, Ph.D. (Nomura Plating Co., Ltd. – Japan)
- Best Presentation, Tutorial in Nature *(awarded jointly)*
  1) *Electromagnetic Analysis and Verification of Probe Card Performance for First Pass System Success*
  Cristian GOZZI (TechnoProbe – Italy)
  2) *Key Design Parameters to Maximize Probe Current Carrying Capability*
  January KISTER (MicroProbe – USA)

After a multi-year hiatus, the infamous "*Golden Wheelbarrow Full of Crap for the Poorest Disguised Sales Pitch*" was awarded this year; however, the committee decided to protect the guilty and will keep "*what happens at SW Test AT SW Test*".

During the SW Test Technology EXPO, 35 full size exhibits showcased products for the wafer sort industry and the associated critical infrastructure. The exhibitors represented probe card vendors, major prober equipment manufacturers, probe card analyzer and probe process metrology companies, companies specializing in probe card cleaning, micro-pogo pin suppliers, and a variety of other probe related service providers. SW Test 2011 also had five Corporate Supporters - Acme Technology, Advanced Probing Systems, International Test Solutions, JEM America, Micronics Japan (MJC), and T.I.P.S. Messtechnik.

The 21st Annual IEEE SW Test Workshop and Tech EXPO will be held on *June 12 to 15, 2011* at the Rancho Bernardo Inn, San Diego, CA (http://www.ranchobernardoinn.com). Abstract submission for the technical program and exhibitor registration for the Tech EXPO are already open.

2011 International Symposium on Advanced Packaging Materials (APM 2011)
October 25–28, 2011, Xiamen, China

http://apm2011.xmu.edu.cn/

International Symposium on Advanced Packaging Materials (APM) is not only the biggest event on micro-electronic packaging materials all over the world but also an international premier technical event on electronic packaging materials. The symposium mainly focuses on advanced semiconductor materials, micro-nano electronic packaging materials, advanced electronic packaging technologies included package reliability, thermal solutions and so on. Attendees in the past have included academic researchers, developers, producers, and users of packaging materials from all over the world. The symposium is also a major packaging materials forum, providing opportunities to network and meet leading experts and exchange up-to-date packaging knowledge in the field.

APM conferences have been held in United States since 1996 and APM 2010 was held in United Kingdom. APM 2011 is scheduled for October 25 to 28, 2011, Xiamen, China, organized by the IEEE's Components Packaging and Manufacturing Technology (CPMT) Society and Xiamen University (XMU), undertaken by College of Materials at XMU, Darbond Technology Co., Ltd., Beijing Faith Information Consulting Co., Ltd. It is estimated that more than 300 researchers, producers, developers from all over the world will attend this international premier technical event.

Symposium Topics

- Nano-functional Materials and Nano Devices
- Advanced packages: 3D/TSV, WLP, MEMS, NEMS Materials
- Underfill, Encapsulant, adhesives and Thermal Materials, die attach, electrically or thermally conductive, thermal management
- Materials for Interconnection and bonding, solders reliability etc.
- High Density Substrate/boards and embedded actives and passives
- Emerging materials: flexible/printed electronic, LED, FPD, Microwave/RF, Photo-electronics, biomedical, renewable energy, PV, and battery

Directed by: Ministry of Education of the People Republic of China
National Natural Science of Foundation of China
Chinese Institute of Electronics
Xiamen Municipal Government

Sponsored by: Xiamen University IEEE-CPMT

Organized by: College of Materials at Xiamen University
Yantai Darbond Technology Co., Ltd.
Beijing Faith Information Consulting Co., Ltd.

Supported by: Engineering & materials Science Division, National Natural Science of Foundation of China
Science and Technology Bureau of Xiamen City
Branch of Manufacturing and Packaging Technology, Chinese Institute of Electronics
Xiamen Investment Promotion Agency

Conference Chair: Ying Zhang, Vice President of Xiamen University

Conference Executive Chair: Tim Chen, General Manager of Yantai Darbond Technology Co., Ltd.

Conference Co-Chairs: Tianchun Ye, Director of Institute of Microelectronics, Chinese Academy of Sciences
Xingjun Liu, Dean of College of Materials at Xiamen University
Jie Xue, R&D Director of Cisco Systems, Inc.
Johan Liu, Director of Sino-Sweden Microsystem Integration Technology (SMIT) Center at Shanghai University

IEEE, CPMT, IMAPS, iNEMI and SEMI
Global Interposer Technology (GIT) 2011 Workshop

November 14-15, 2011 • Georgia Tech • Atlanta GA • USA

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Student Poster Session


Saumya Gandhi
GEORGIA TECH


Vijay Sukumaran
GEORGIA TECH

GIT 2011 OVERVIEW

The GIT 2011 Workshop is intended to compare and contrast the wide variety of interposer approaches being developed as well as promote and disseminate revolutionary and evolutionary advances in emerging silicon, glass and other interposer technologies, by bringing together academic and industry researchers, technology developers, users and manufacturers from around the world. Such a technology is seen as not only for packaging of ICs and 3D ICs but also act as a better alternative to 3D ICs with TSV, and eventually providing a path for entire systems.

The first of its kind, the GIT 2011 Workshop will bring together industry experts, global academic researchers, and student leaders to share leading-edge interposer technology research, development, applications, markets and manufacturing infrastructure. It is a must-attend event for those highly interested in interposer technology advances for the future.

Technical Sessions on Interposer Technology will feature technical leaders in the following topics:

1. Electrical Design
2. Mechanical Design
3. Silicon Interposers
4. Glass Interposers
5. Chip Level Interconnections
6. Board Level Interconnections
7. Applications and Markets
8. Manufacturing Infrastructure

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KEYNOTE SPEAKERS


Subramanian Iyer
IBM Fellow,
Chief Scientist
IBM


Jerome Baron
Market & Technology
Analyst
YOLE


Rao R. Tummala
Director, Packaging
Research Center
GEORGIA TECH

REGISTRATION

Workshop Registration includes access to all technical sessions and includes all meals.
Registration Fees – EARLY Registration ends October 15, 2011. *Register early – space is limited.*

Sponsoring Society Non-Member $400
Sponsoring Society Member $300
Committee, Advisor or Speaker $250
Student $100

www.prc.gatech.edu/git2011/registration.html

CALL FOR PAPERS – TITLES for PRESENTATIONS AND POSTERS

Submit TITLE for Technical Sessions listed above.

- Oral presentations will be made by Industry, Academic, and Research Faculty
- Posters will be presented by Students

Deadline for **TITLE** submission is **October 2, 2011.** Notification of acceptance by **October 15, 2011.**

www.prc.gatech.edu/git2011/papers.html

HOTEL ACCOMMODATIONS

Discount GIT 2011 Hotel Rates: *Register early – space is limited.*
Georgia Tech Hotel and Conference Center – US$125
Marriott Renaissance Atlanta Midtown – US$144

www.prc.gatech.edu/git2011/travel.html

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www.prc.gatech.edu/git2011

Advance Announcement

The Institute of Electrical and Electronics Engineers, Inc.
Components, Packaging and Manufacturing Technology Society
Orange County Chapter

Presents an All-Day Workshop on

3D Integrated Circuits: Technologies Enabling the Revolution

Date: **Friday, December 9, 2011**
Time: **9:00 am to 4:00pm**
Location: **Jazz Semiconductor Auditorium, 4311 Jamboree Road, Newport Beach, CA 92660**

This one-day topical workshop will provide a comprehensive examination of the technologies, materials, manufacturing processes, equipment, test methodology, and design tools that are enabling three-dimensional integrated circuits (3DICs). Join us at this unique event that brings together experts in all of the above areas to discuss the promise of 3D Integration.

Featured Speakers

Dr. Phil Garrou
Microelectronic Consultants of North Carolina

Dr. Muhannad Bakir,
Georgia Tech – Integrated 3D Systems Group

Ted Tessier,
Chief Technical Officer, Flip Chip International

Dr. Suresh Ramalingam
Sr. Director, Adv. Pkg Design & Development, Xilinx

Rose Guino, Betty Huang, Kevin Becker
Henkel Corporation

Dr. Yeong Lee,
Director, STATS ChipPAC

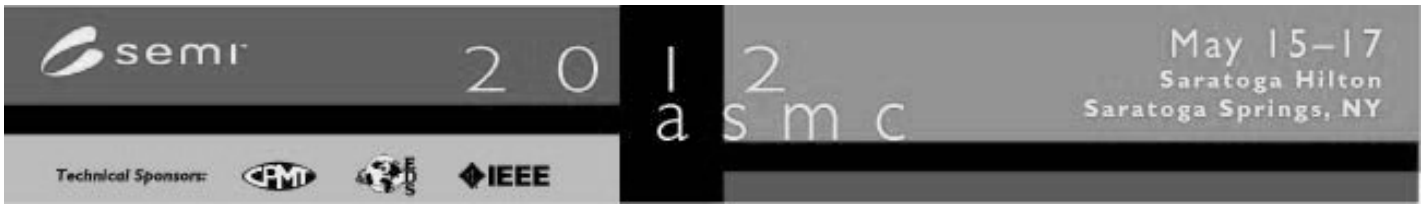
…and many others.

Registration Details at http://meetings.vtools.ieee.org/meeting_view/list_meeting/8019. For more information please contact

General Information & Sponsorship:
Dr. Lawrence Williams at l.williams@ieee.org

Vendor Exhibition:
Mark Kuhlman at Mkuhlman@semtech.com

IEEE CPMT OC Chapter Website: http://sites.ieee.org/ocs-cpmt ***Follow us on LinkedIn.***



ASMC 2012 Call for Papers

www.semi.org/asmc2012

Abstract Deadline—October 24, 2011

Semiconductor Equipment and Materials International (SEMI), IEEE Electron Devices Society (EDS), and IEEE Components, Packaging, and Manufacturing Technology Society (CPMT) invite microelectronics professionals at all levels of experience from around the world to submit abstracts for **SEMI Advanced Semiconductor Manufacturing Conference 2012.**

ASMC continues to be one of the leading international technical conferences for discussing solutions that improve the collective manufacturing expertise of the semiconductor industry. Solving the challenges presented by semiconductor manufacturing has been a combined effort by device makers, equipment and materials suppliers and academics. ASMC provides an unparalleled platform for semiconductor professionals to network and learn the latest in the practical application of advanced manufacturing strategies and methodologies. Papers selected for presentation at ASMC 2012 may be considered for the IEEE Transactions on Semiconductor Manufacturing special section.

Papers are peer reviewed and are selected based on a clear outline of problem, analysis, solution/results and conclusion. Presentations on original, non-commercial and non-published works are being solicited in topic areas:

- AM: Advanced Metrology
- AEM: Advanced Equipment and Materials Processes
- AP/DFM: Advanced Patterning / Design for Manufacturability
- APC: Advanced Process Control
- CFM: Contamination Free Manufacturing
- DM: Data Management and Data Mining Tools
- DI: Defect Inspection and Reduction
- ER: Equipment Reliability and Productivity Enhancements
- ET / ID: Enabling Technologies and Innovative Devices
- FA: Factory Automation
- GF: Green Factory
- IE: Industrial Engineering
- LM: Lean Manufacturing
- 3D/TSV: Packaging and Through Silicon Via
- YE: Yield Enhancement/Learning
- YM: Yield Methodologies

Author Instructions

Papers co-authored by a device manufacturer, equipment or materials supplier, and/or academia that demonstrate innovative, practical solutions for advancing semiconductor manufacturing are highly encouraged. Original, non-commercial and non-published works are being solicited in specific categories. Peer-reviewed papers are selected based on a clear outline of problem, analysis, solution/results and conclusion. Authors are requested to provide an extended abstract of no more than one page of text (max. of 1000 words, MS Word or PDF) with an additional page including supporting data and figures. For templates and further instructions, visit our web site: **www.semi.org/asmc2012**

Important Dates *(subject to change)*

- **Abstracts Due:** October 24, 2011
- **Author Notification:** December 16, 2011
- **Preliminary Manuscripts Due:** March 7, 2012
- **Final Manuscripts Due:** April 25, 2012
- **Presentations Due:** May 7, 2012
- **Conference Dates:** May 15-17, 2012

For additional information, visit **www.semi.org/asmc2012** or email mkindling@semi.org

16th IEEE Workshop on Signal and Power Integrity

Supported by
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Naples

Title history: (1997-2011) Workshop on Signal Propagation on Interconnects

13-16 MAY 2012, SORRENTO (ITALY)

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— Technically co-sponsored by IEEE Electromagnetic Compatibility Society

MeMo

website, www.spi2012.org
run, 13-16 May, 2012
venue,
Grand Hotel Parco dei Principi, Sorrento, Italy

deadlines,
Submission of manuscripts:
January 31st, 2012
Notification of acceptance:
February 28th, 2012

16th IEEE Workshop on Signal and Power Integrity

CALL FOR PAPERS

During the last fifteen years, this Workshop on Signal Propagation on Interconnects has been developed into a forum of exchange where world class developers and researchers will share and discuss leading edge results in the field of interconnect modeling, simulation and measurement at chip, board, and package level. The workshop is also meant to bring together developers and researchers from industry and academia.

In view of the last years success, the Committee is looking forward to the 16th Edition, convened at the Grand Hotel Parco dei Principi in Sorrento, with extraordinarily stunning views of the sea. The symposium will include both oral and poster sessions. A number of prominent experts will be giving tutorials on areas of emerging interest.

TOPICS

- Signal Integrity
- High-speed interconnects and high-speed channels
- Power Integrity/ Ground Noise
- Power Distribution Networks
- Electronic packages and Microsystems
- 3D technologies for ICs and packages
- RF, Microwave packaging and mixed signal systems
- Nano-Interconnects and nano-structures
- Electromagnetic Theory and Modeling
- Transmission Line Theory and Modeling
- Macro-Modeling, reduced-order models
- Advanced Simulation Tools for Signal and Power Integrity
- Electromagnetic Compatibility
- Coupling Effects on Interconnects
- Radiation & Interference
- Testing & Interconnects
- Time and Frequency Domain Measurement Techniques

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Upcoming CPMT Sponsored and Cosponsored Conferences....

Name: 2011 IEEE/CPMT Workshop on Accelerated Stress Testing & Reliability (ASTR 2011)
Dates: October 12–14, 2011
Location: San Francisco, CA, USA
Contact: Ephraim Suhir, UC-Santa Cruz
E-mail: suhire@aol.com
URL: www.ewh.ieee.org/soc/cpmt/tc7/ast2011/

Name: 2011 6th Int'l Microsystems, Packaging, Assembly and Circuits Technology (IMPACT 2011)
Dates: October 19–21, 2011
Location: Taipei, Taiwan
E-mail: service@impact.org.tw
URL: http://www.impact.org.tw/2011/General/

Name: 2011 20th IEEE Electrical Performance of Electronic Packaging (EPEP 2011)
Dates: October 23–26, 2011
Location: San Jose, CA USA
Contact: Mandy Wisehart
E-mail: epeps-admin@illinois.edu
URL: http://epeps.ece.illinois.edu/

Name: 2011 Int'l Symposium on Advanced Packaging Materials (APM)
Dates: October 25–28, 2011
Location: Xiamen, China
Contact: Fenghua Gan
E-mail: faithsh@chinaepe.com.cn

Name: 2011 13th Electronics Packaging Technology Conference (EPTC 2011)
Dates: December 7–9, 2011
Location: Singapore
Contact: EPTC Secretariat
E-mail: eptc2011.secretariat@atenga.sg
URL: http://www.eptc-ieee.net/

Name: 2011 Global Interposer Technology (GIT) 2011 Workshop
Dates: November 12–14, 2011
Location: Atlanta, GA, USA
Contact: Karen May
E-mail: karen.may@ece.gatech.edu

Name: 2011 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)
Dates: December 12–14, 2011
Location: Hangzhou, China
Contact: EDAPS Service Center
E-mail: service@edaps2011.org

Name: 2012 IEEE Semiconductor Thermal Measurement, Modeling and Management Symposium (SEMI-THERM)
Dates: March 18–22, 2012
Location: San Jose, CA USA
Contact: Tom Tarter
E-mail: ttarter@semi-therm.org

Name: 2012 Int'l Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)
Dates: April 16–18, 2012
Location: Lisbon, Portugal Abstracts Due October 30, 2011
Contact: Olivier de Saint Leger
E-mail: olivier.desaintleger@astefo.com

IEEE Components, Packaging and Manufacturing Technology Society
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3. Select the "Classics" tab from the top of the page. Under this tab you will find a listing of all the Free titles.

Here are a few examples of available books in pfd format: (more added every year)

1. *Lead-Free Electronics: iNEMI Projects Lead to Successful Manufacturing* by E. Bradley, C. Handwerker, J. Bath, R. Parker and R. Gedney; Publication Date: 2007
2. *Magnetic Actuators and Sensors* by J. Brauer; Publication Date: 2006
3. *Multigrid Finite Element Methods for Electromagnetic Field Modeling* by Y. Zhu and A. Cangellaris; Publication Date: 2006
4. Silicon *Germanium: Technology, Modeling, and Design* by R. Singh, H. Oprysko and D. Harame; Publication Date: 2004
5. *Integrated Passive Component Technology* by R. Ulrich and L. Schaper; Publication Date: 2010

For more information visit: http://www.ieee.org/membership_services/membership/products/ebookclassics.html