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Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Avram Bar-Cohen, PhD, Principal Engineering Fellow, Raytheon—Space and Airborne Systems, Arlington, VA

EPS—From Humble Beginnings to a Bright Future

As we enter 2019, signs of the resurgence of packaging science and technology are everywhere. The attendance at EPS Conferences and Symposia around the world are booming and for the first time in more than a decade EPS membership and the number of active Student Sections are growing. In the research agencies and the electronic industry, packaging is transitioning into a new role as a "value creator" and product differentiator—defining new packaging paradigms, including 3D chip stacks, glass substrates, and functionally-enhanced laminated printed circuit boards, that are driving change and innovation in the industry. Against this background, I thought I'd take a few minutes to review our history as a Professional Society and the technical challenges ahead.

The Electronic Packaging field was born at the very dawn of the Information Age in the 1940's, with Mauchly and Eckert's Elec-tronic Numerical Integrator and Computer (ENIAC)—the first pro-grammable computer. In the early years of the Information Age, the United States and Japan led the development of packaging technol-ogy, but in more recent decades, engineers and scientists in Singa-pore, Korea, Taiwan, and then China provided major breakthroughs in packaging, including innovative component manufacturing, inte-gration, and assembly technologies that together have sustained the Moore's Law cadence of new product introductions for some 50 years. The 1950 "Symposium of Improved Quality Electronic Components" attended by some 150 in Washington, D.C, and jointly sponsored by the AIEE, IRE, and RMA, marked the public emergence of Packaging and was followed by a second Sympo-sium in 1952. Our 67 subsequent annual meetings, long known as the Electronic Components Conference (ECC), and which later became known as the Electronic Components and Technology Conference (ECTC), sponsored jointly by IEEE and EIA since 1962 and solely by EPS since 2012, owe their origin to this 1950 Symposium. The first ECTC was held in 1990 in Las Vegas.

The successful Symposia in 1950 and 1952 led to the creation in 1954 of the Professional Group on Production Techniques of the Institute of Radio Engineers (IRE), the first professional society for Packaging in the US, to be followed in 1963 by the IRE's Professional Technical Group on Components Parts. Some 15 years later, this Group merged with IEEE's Manufacturing Technology to form the IEEE Components, Hybrids, and Manufacturing Technology Society, a name many of us still remember fondly, and in 1994 the now familiar, IEEE Compo-nents, Packaging, and Manufacturing Technology Society. In 2017, at the request of the BOG of your Society, the IEEE Board approved the change in the name of the Society to the IEEE Elec-tronics Packaging Society.

In the 1990's CPMT worked in technical and/or financial cooperation with its nascent Sections in Region 10 to develop local Packaging Conferences, leading to the organization of EPTC in Singapore and ICEPT in China in 1998, EMAPS in Hong Kong in 1990, with a broader R10 presence in later years, ICEP and ICSJ in Japan in 2001, IMPACT in Taiwan in 2005, and SPI, EMPC, and IWASI since 2006. Parallel effortts in Europe (R8) involved co-sponsorship of ESTC starting in 2006 in Dresden, Therminic—fi rst held in1994, EuroSime—fi rst held in 1999, and NordPac, starting in 2017 in Oulu, Finland. In 2004 EPTC was designated the Region 10 EPS Flagship Conference, to be followed by a similar designation for ESTC in Region 8. In 2018, for the first time in its history, the full Board of Governors of EPS held an official meeting outside the US, joining in the celebration of the 20th anniversary of the Asia-Pacific flagship Conference, EPTC. In the near future, it is expected that the BOG will also travel to Region 8 and help celebrate the upcoming 8thth anniversary of ESTC, thus expanding the EPS footprint and influence across the globe.

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15 June 2019 for Summer issue 2019

1 December 2019 for Winter issue 2020

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Lecturers: Mudasir Ahmad, Muhannad Bakir, Ph.D., Avram Bar-Cohen, Ph.D., Karlheinz Bock, Ph.D., Bill Bottoms, Ph.D., Chris Bower, Ph.D., Moises Cases, William T. Chen, Ph.D., Xuejun Fan, Ph.D., Paul D. Franzon, Ph.D., Philip Garrou, Ph.D., R. Wayne Johnson, Ph.D., Beth Keser, Ph.D., John H. Lau, Ph.D., Ning-Cheng Lee, Ph.D., S. W. Ricky Lee, Ph.D., Johan Liu, Ph.D., Ravi Mahajan, PhD., James E. Morris, Ph.D., Kyung W. Paik, Ph.D., Mervi Paulasto-Kröckel, Ph.D., Michael Pecht, Ph.D., Eric D. Perfecto, Karl J. Puttlitz, Ph.D., Dongkai Shangguan, Ph.D., Nihal Sinnadurai, Ph.D., Ephraim Suhir, Ph.D., Rao Tummala, Ph.D., Walter Trybula, Ph.D., E. Jan Vardaman, Paul Wesling, CP Wong, Ph.D., Jie Xue, Ph.D., Kishio Yokouchi, Ph.D.

Chapters and Student Branch Chapters

Refer to eps.ieee.org for EP Society Chapters and Student Branch Chapters list

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SFI Logo

Ephraim Suhir Receives 2019 IEEE Electronics Packaging Award

Professor, Portland State University, Portland, Oregon, USA

"For seminal contributions to mechanical reliability engineering and modeling of electronic and photonic packages and systems."

The IEEE Electronics Packaging Award, sponsored by the IEEE Electronics Packaging Society, recognizes meritorious contributions to the advancement of components, electronic packaging or manufacturing technologies. The technical field for this award includes all aspects of device and systems packaging, including packaging of microelectronics, optoelectronics, RF/wireless and micro-electro-mechanical systems (MEMS), enhancement of technology, impact on the relevant technical community and the profession, benefit to society, and the quality of the nomination.

The 2019 Award will be presented to Dr. Ephraim Suhir at the 69th Electronic Components and Technology Conference (ECTC), May 2019.

With over 40 years of pioneering work in modelling and reliability engineering, Ephraim Suhir has enabled electronic packaging engineers to analytically predict stress in advanced packaged components for the design of more reliable devices. He was one of the earliest researchers to introduce the use of rigorous mechanics principles in electronic systems. His closed-form solutions have provided the electronics industry with invaluable tools for achieving reliability and cost savings during the design process by eliminating errors early in the design process. He has applied his techniques to advanced components and packaged structures such as microelectronic, photonic, photo-voltaic, and thermoelectronic modules. The efforts of many mechanics practitioners and researchers in the electronics packaging field have been influenced by Suhir's groundbreaking contributions.

Ephraim Suhir joins the following past recipients of this Award.

2018—William Chen
"For contributions to electronic packaging from research and development through industrialization, and for his leadership in strategic roadmapping."

2017—Paul Ho and King-Ning Tu
"For contributions to the materials science of packaging and its impact on reliability, specifically in the science of electromigration."

2016—Michael Pecht
"For visionary leadership in the development of physics-of-failure-based and prognosticsbased approaches to electronic packaging reliability."

2015—Nasser Bozorg-Grayeli
"For contributions to the advancement of microelectronic packaging technology, manufacturing, and semiconductor ecosystems."

2014—Avram Bar-Cohen
"For contributions to thermal design, modeling, and analysis, and for original research on heat transfer and liquid-phase cooling."

2013—John Lau
"For contributions to the literature in advanced solder materials, manufacturing for highly reliable electronic products, and education in advanced packaging."

2012—Mauro J Walker
"For advancing electronic manufacturing, technology and packaging worldwide through technical innovation and cooperative leadership in industry, government, academia, and professional organizations."

2011—Rao R. Tummala
"For pioneering and innovative contributions to package integration research, cross-disciplinary education and globalization of electronic packaging."

2010—Herbert Reichl
"For contributions to the integration of reliability in electronics systems, and leadership in research and education in electronics packaging."

2009—George G. Harman
"For achievements in wire bonding technologies."

2008—Karl Puttlitz Sr. and Paul A. Totta
"For pioneering achievements in flip chip interconnection technology and for semiconductor devices and packages."

2007—Dimitry Grabbe
"For contributions to the fields of electrical/electronic connector technology, and development of multilayer printed wiring boards."

2006—C. P. Wong
"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."

2005—Yutaka Tsukada
"For pioneering contributions in microvia technology for printed circuit boards, and for extending the feasibility of the direct flip-chip attachment process."

2004—John W. Balde
"For lifetime contributions to tantalum film technology and the introduction of new electronic packaging technology to development and manufacturing."

For additional information on this and other IEEE Technical Field Awards and Medals, to view complete lists of past recipients or to nominate a colleague or associate for IEEE Technical Field Awards and Medals, please visit http://www.ieee.org/awards

New Appointments for 2019

At the December 8, 2019 EPS Board of Governors meeting at EPTC, the following appointments were made for 2019.

PRESIDENT ELECT

CHRIS BAILEY is Professor of Computational Mechanics and Reliability at the University of Greenwich, London, United Kingdom. Chris received is PhD in Computational Modelling from Thames Polytechnic in 1988, and an MBA in Technology Management from the Open University in 1996. Before joining Greenwich in 1991, Chris worked for three years at Carnegie Mellon University (USA) as a research fellow in materials engineering.

One of Chris's main achievements with regards to EPS was helping to establish the Region 8 flagship conference ESTC (Electronics System-integration Technology Conference). He was the Program Chair for the first conference held in Dresden, and was the General Chair for the 2008 conference in London. In 2007 he was the local chair for the IEEE EPS sponsored EuroSime conference held in London, and since 2009 has worked with the EuroSime team as co-editor of the proceedings and track chair for multi-physics modelling.

Since 2010 Chris has served as a member of the EPS Board of Governors and as VP-Conferences from 2014–2018. During his first term on the BoG, he also took on the role of Strategic Director for Student Programs with the aim of supporting students involved in EPS activities worldwide. Particular achievements include arranging financial support for student attendees at the International Spring Seminar on Electronics Technology (ISSE) as well as promoting student membership at events such as ECTC, EPTC and ESTC.

As VP-Conferences he has expanded the resource materials for organizers, including a handbook and reference timeline. As Chair of the EPS Conferences Functional Team, he has brought forward several initiatives to the Board, including expanding the EPS flagship conference in Region 10 (EPTC) and possible conference exhibitor packages.

Other EPS activities that Chris has been involved with include membership of technical committees for EPTC (Singapore), Eurosime (Europe), ISSE (Europe) and ICEP/HDP (China) where he is a regular attendee and presenter. He has also worked closely with others in Europe to help promote closer co-operation between EPS and IMAPS for the benefit of the whole community.

Since his research has resulted in over 250 publications. He is currently an Associate Editor for the EPS Transactions and has been a guest editor on the journal of Soldering and Surface Mount Technology. He is also a committee member of the Innovative Electronics Manufacturing Research Centre (IeMRC) in the UK and has participated in a number of UK Government sponsored overseas missions to promote collaboration and review electronic packaging technologies. Recently he became a member of the working group writing a new IEEE standard for Prognostics and Health Management for Electronic Systems.

As President-Elect, Chris will support and augment the current EPS President, Avi Bar-Cohen's, efforts and has accepted responsibility for developing the EPS Strategic Plan for 2018–2023.

VICE PRESIDENT CONFERENCES

BETH KESER, Ph.D., a recognized global leader in the semiconductor packaging industry with over 19 years of experience, received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. from the University of Illinois at Urbana-Champaign. Beth's excellence in developing revolutionary electronic packages for semiconductor devices has resulted in 15 patents, 8 patents pending, and over 40 publications in the semiconductor industry. Recently, Beth lead the Wireless Packaging Solutions Department at Intel Corporation in the iCDG Business Unit, in Munich, Germany.

Previously, Beth led Qualcomm's Fan-Out and Fan-In Wafer Level Packaging Technology Development and NPI Group for over 7 years where her team qualified and shipped technology products consumers around the world enjoy in cell phones today.

Before joining Qualcomm in 2009, Beth led the Wafer-Level Chip Scale packaging team at Motorola and had earlier served as the lead technologist and manager of the Redistributed Chip Packaging Technology (RCP).

Beth has been IMAPS Device Packaging Conference Technical Chair 2006–2009, IMAPS Flip Chip/CSP Sub-committee member 2000–2009 and chair 2005–2008, and SMTA's International WLP Conference WLP Track Chair 2010–2011. Beth has taught a highly-successful EPS Professional Development Course on Fan-Out Wafer Level Packaging at conferences since 2015.

Beth is an IEEE Senior Member whose volunteer activities and professional society responsibilities include: EPS VP-Education 2016–2018, EPS BoG member 2012–2015, ECTC Executive Committee 2010–17, ECTC Advanced Packaging Sub-committee member 2000-present. Beth is also an IEEE EPS Distinguished Lecturer who chaired IEEE EPS's 65th Electronic Component and Technology Conference.

VICE PRESIDENT EDUCATION

JEFFREY C. SUHLING received a B.S. degree in Applied Mathematics and Physics, and M.S. and Ph.D. degrees in Engineering Mechanics from the University of Wisconsin, Madison, WI. He joined faculty of the Department of Mechanical Engineering at Auburn University in 1985, where he currently holds the rank of Quina Distinguished Professor. Dr. Suhling co-established the NSF Center for Advanced Vehicle and Extreme Environment Electronics (CAVE3) in 1998, and served as Center Director from 2002–2008. CAVE3 is a government and industry sponsored research center involving over 20 member companies, 15 faculty, and 35 graduate students that specializes in reliability of electronic packaging in harsh environments. In 2008, he was appointed Department Chair of the Department of Mechanical Engineering, which is the largest program at the University with over 1000 undergraduate students and 150 graduate students. He was selected "Outstanding Mechanical Engineering Faculty Member" by the undergraduate students during 1990, received the College of Engineering Birdsong Superior Teaching Award in 1994, and received the College of Engineering Senior Research Award in 2001.

He has advised 75 graduate students at Auburn University, including 27 Ph.D. students and 48 M.S. students.

Dr. Suhling has been an active researcher in electronic packaging for over 25 years. His general areas of interest are in the mechanics and reliability of packaging. Specializations include silicon sensors for packaging stress and temperature measurements, stress effects in silicon devices, test chips, mechanical characterization of packaging materials including solders and polymers, solder joint reliability and aging effects, and finite element modeling. He has authored or co-authored over 375 technical publications, including 6 books and book chapters, 55 journal articles, and 325 conference proceedings papers. Six of his conference papers have been selected as the Best of Conference. These include Best Session Paper Awards at the 2005 and 2010 ECTC Conferences, as well as Best Paper Awards at the 1998 and 2002 IMAPS Annual Conferences, 2008 SMTA International, and 2013 InterPACK Conference. In addition, he and his co-authors have received Best Poster awards at the InterPACK 2007, InterPACK 2009, and InterPACK 2013 conferences.

Dr. Suhling is a member of IEEE/EPS, ASME, IMAPS, and SMTA. In IEEE, he has served on the ECTC Applied Reliability program committee for the past 10 years. He was appointed to the ECTC Professional Development Course (PDC) program committee in 2006, and has served as Assistant Chair. He has also been active in the IEEE/EPS ITHERM Conference series, serving on the program committee for over 10 years. In ASME, Dr. Suhling served as Chair of the Electrical and Electronic Packaging Division (EPPD) during 2002–2003, and was on the EPPD Executive Committee from 1998–2003. Dr. Suhling was the Technical Program Chair of the InterPACK '07 Conference, and General Chair of the InterPACK '09 Conference. He was elected a Fellow of ASME in 2009, and was recognized with the ASME-EPPD Mechanics Award for outstanding contributions to electronic packaging research. Jeff has served as a member of the EPS Board of Governors since 2014 and as Program Director- Membership Programs from 2016–2018.

VICE PRESIDENT MEMBERSHIP

ALAN HUFFMAN (M: 2005, SM: 2007) is currently the Director of Engineering for Micross Advanced Interconnect Technology in Research Triangle Park, NC. He received the B.S degree in physics from The University of North Carolina at Chapel Hill in 1994. From 1994 to 2005 he was a Member of the Technical Staff at MCNC Research & Development Institute working on development and implementation of wafer level packaging technologies, reliability and failure mode analysis of flip chip devices, and optoelectronic and MEMS packaging. In 2005, he joined RTI International and was a Senior Research Engineer and Program Manager for WLP technology with RTI's Electronics and Applied Physics Division. His technical interests include wafer level packaging and flip chip process technology and fine pitch bump interconnect, 2.5D and 3D integration technology, characterization and process development for electronic materials used in WLP. He has authored or co-authored numerous papers and presentations on a number of advanced packaging topics, particularly on high density interconnect technologies and characterization of polymer material processes.

Alan is an IEEE Senior Member whose activities include, member of ECTC Interconnects technical sub-committee from 2005–2013, Chaired multiple ECTC technical sessions during this period, member of ECTC Executive Committee 2011-present, 2016–17— Jr. Past General Chair, 2015–16—General Chair, 2014–15—Vice General Chair, 2013–14—Program Chair, 2012–13—Asst. Program Chair, 2011–12—Web Administrator. Alan was appointed to the EPS Board of Governors in 2016 and has been a contributing member of the Board through various adhocs including Branding Change, Membership and Conference Functional Teams.

President's Column (*Continued from page 1*)

We, as the members of the Electronic Packaging Society, are heirs to a rich history of leading and supporting successive revolutions in component and packaging technology, experimental and analytical tools, and predictive modeling techniques. But, to maintain and grow our "brand" will require that EPS stay at the forefront of technology and emerging market opportunities for "packaged" electronic products. Heterogeneous Integration—whether with embedded chips and chiplets in and on organic laminates, or with silicon and wide bandgap chip stacks and interposers—has created broad new product and system opportunities. But, to satisfy market and consumer demands, will require implementation of, heretofore, unavailable packaging materials, thermomechanical failure models, thermal management strategies, co-design tools, and precision fabrication and assembly processes. Other packaging breakthroughs will be needed to support the development of low-cost, yet highly reliable sensors and effectors, along with growing computational needs, at the edge of the cloud, for new 5G and the broader IoT networks. The expected introduction of neuromorphic computing—to support greater utilization of Artificial Intelligence, of photonic IC's and switches - to support constantly growing data transfer rates, and of quantum devices for network security and, ultimately, high performance computation - will again push packaging science and technology well past its present envelope of skills, techniques, and tools.

As the preceding makes abundantly clear, EPS has risen from humble beginnings—the 1950 "Symposium on Improved Quality Electronic Components" and the IRE's1954 *Professional Group on Production Techniques*—to become a major player in Packaging Science and Technology on the world stage. The coming decades offer the possibility of continued growth and success. Working together—established practitioners, young professionals, academics, and students—we can make the coming decades every bit as successful and impactful as our past history.

Leadership Transition—EPS Fellows Evaluation Committee

The IEEE Electronics Packaging Society would like to extend its deep appreciation and gratitude to Dr. C.P. Wong, who has chaired the EPS Fellows Evaluation Committee since 2003. During his tenure, 72 EPS members were elevated to Fellows. In 2006, C.P. was the recipient of the IEEE Electronics Packaging Award (formerly CPMT Award) *"For contributions in advanced polymeric materials science and processes for highly reliable electronic packages."*

C.P. is also the recipient of multiple major Society Awards; 1995 recipient of the Outstanding Sustained Technical Contribution Award, 2002 recipient of the Exceptional Technical Achievement Award and 2009 recipient of the David Feldman Award.

C.P. is an IEEE Life Fellow who has served the Electronics Packaging Society for many years as a Member of the Board of Governors, including VP-Technology and President. Dr. Wong was elected to the US National Academy of Engineering in 2000. The Society would like to thank Dr. Wong for his dedication to the IEEE and EPS.

John Lau has graciously accepted the position of the EPS Fellows Evaluation Committee Chair for the next two years.

Newly-Elected and Appointed Members of the Electronics Packaging Society Board of Governors

In 2018, EPS members elected new Members-at-Large to the EPS Board of Governors for the three-year term of 1 January 2019 through 31 December 2021.

REGIONS 1-6, 7 & 9

PHILLIP GARROU (M'88-SM'92-F'00) retired from Dow Chemical in 2004 as Global Director of Technology for their Advanced Electronic Materials business unit. He is now contributing editor and blogger (IFTLE "Insights from the Leading Edge") for Solid State Technology, a subject matter expert (SME) for DARPA and runs his consulting company Microelectronic Consultants of NC in the RTP area.

Phil is an IEEE Fellow and has served as Technical VP and President of EPS. He has edited several microelectronic texts including McGraw Hill's "Multichip Module Handbook" and Wiley VCH's "Handbook of 3D Integration".

He has won the Milton Kiver Award for Excellence in Electronic Packaging (1994); the Fraunhoffer International Adv. Packaging Award (2002); the IEEE CPMT Sustained Technical Achievement Award (2007), the IMAPS Ashman Award (2000) and most recently the American Chemical Society Award for Team Innovation (2017).

PRADEEP LALL (S'90-M'93-SM'08-F'12) is the MacFarlane Endowed Professor in the Department of Mechanical Engineering and the Director of NSF Center for Advanced Vehicle and Extreme Environment Electronics at Auburn University. He serves on the Technical Council and Governing Council of NextFlex Manufacturing Institute. Dr. Lall is author and co-author of 2-books, 14 book chapters, and over 500 journal and conference papers in the field of electronics reliability, safety, energy efficiency, and survivability. Dr. Lall, a fellow of IEEE, fellow of the ASME, and fellow of the Alabama Academy of Sciences. Dr. Lall is recipient of the NSF's Alex Schwarzkopf Award for Technology Innovation, Alabama Academy of Science Wright A, Gardner Award, IEEE Exceptional Technical Achievement Award, ASME-EPPD Applied Mechanics Award, SMTA's Member of Technical Distinction Award, Auburn University's Creative Research and Scholarship Award, SEC Faculty Achievement Award, Samuel Ginn College of Engineering Senior Faculty Research Award, Three-Motorola Outstanding Innovation Awards, Five-Motorola Engineering Awards, and Twenty Best-Paper Awards at national and international conferences. Dr. Lall has served in several distinguished roles at national and international level including serving as member of National Academies Committee on Electronic Vehicle Controls, Member of the IEEE Reliability Society AdCom, IEEE Reliability Society Representative on the IEEE-USA Government Relations Council for R&D Policy, Chair of Congress Steering Committee for the ASME Congress, Member of the technical committee of the European Simulation Conference EuroSIME, and Associate Editor for the *IEEE Transactions on Components and Packaging Technologies*. He received the M.S. and Ph.D. degrees in Mechanical Engineering from the University of Maryland and the M.B.A. from the Kellogg School of Management at Northwestern University.

ERIC PERFECTO (M'95-SM'01-F'17) has 36 years of experience working in microelectronics. First at IBM working in the development of multi-level Cu-polyimide advanced packages for high-end systems, followed by the development of the UBM and Pb-free solder processes and yields for flip chip in 2D and 3D packages. As part of the IBM Microelectronics Division divestiture, Eric was a PMTS at GLOBALFOUNDRIES. His technical interests include 3D interconnects, chip-package interaction, electromigration, Silicon photonics and design for manufacturing. He holds a M.S. in Chemical Engineering from the University of Illinois and a M.S. in Operations Research from Union College.

An author of more than 75 technical papers and two book chapters, Eric received two Best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CPMT Trans. on Adv. Packaging. He holds 55 US patents and has been honored with two IBM Outstanding Technical Achievement Awards: one for the development and implementation of Cu-Polyimide structures, and the other for the development and implementation

of 150 um pitch Pb-Free C4 technology; and an IBM Outstanding Contribution Award for the development of 3D wafer finishing process (2014). He is a participating member of SRC.

Eric served as the 57th ECTC General Chair, the 55th ECTC Program Chair, the ECTC Materials and Processes Subcommittee Chair ('02-'03). He is the current ECTC Publicity chair. For the last 7 years, Eric's popular Flip Chip Fabrication and Interconnection course have been given at ECTC to great reviews. He is an IEEE Fellow and has achieved IMAPS and SPE senior membership. He is also a SMTA and SHPE member.

Since 2008, Eric has been elected three times BoG member to the IEEE Electronics Packaging Society (EPS, previously CPMT). For 3 years he served as the EPS Strategic Director of Global Chapters and Membership where he focused on enhancing the EPS membership value. Through his efforts, the CPMT Transactions are now part of the EPS membership. He also highlighted the importance of technical content in the EPS members-only page, where now webinars and presentations can be found. He is an Associate Editor for the CPMT Transactions, an EPS Distinguish Lecturer in the area of Flip Chip, and member of the EPS Technical Committee on Materials and Processes. Since 2014, Eric has chaired the EPS Awards Committee, which is responsible for the EPS Mayor Awards, the Regional Awards, the ECTC Student Travel Awards and the ECTC Volunteer Award. At a local level, Eric is the membership Chair of the Mid-Hudson IEEE Section.

REGION 10

CHIH-PIN (C.P.) HUNG (M'17) is a member of both IEEE and EPS. He received his Ph.D. degree from the Department of Electrical and Electronic Engineering, University of Paisley (now, University of the West of Scotland), United Kingdom. Dr. Hung has been with ASE group for about 20 years. He is currently the Vice President, Corporate R&D of ASE Group. He leads the R&D teams developing the next-generation products and technology to be rolling out at the various ASE manufacturing sites. The products and technologies developed featuring integrated design technologies, advanced chip package, and system integration solutions. Dr. Hung has been involved with different management positions at ASE including VP of Corporate Design, VP of Central Engineering & Business Development, and VP of Logistic Services Integration. He has been also enthusiastically contributing his industry experiences in academic education by offering courses in various universities in Taiwan. In addition, Dr. Hung also has aggressive contributions to professional Societies. He has been Chair of PKG & TEST Committee, SEMICON Taiwan since 2013. He is currently the Co-Chair of 2018 IMPACT to be help in October 2018 in Taipei, Taiwan. He was also a member of ECTC Component & RF Committee during 2013–2015. Dr. Hung also served as peer reviewer for *IEEE Trans. Advanced Packaging* published by CPMT (now EPS). Through the years of research activities, Dr. Hung holds 72 patents and published over 49 conference and journal papers in the area of electronic packaging. His achievements have been well recognized which wan him Outstanding Youth Creative Award of 13th Industrial Technology Development Award (2005) from the Ministry of Economic, Taiwan.

C. ROBERT KAO (AF'11-M'11-SM'11) main research interests include electronic, optical, and MEMS packaging with a main thrust on the thermodynamics and kinetics of materials interactions within packages. He is a BoG member of IEEE EPS from 2016 to 2018, and a long-time committee member of EPS Materials and Processing Technical Committee. He helped organize more than 20 international symposia on solders and soldering technology for TMS and ASM. He has served as guest editors for *Journal of Electronic Materials* and *Microelectronic Reliability*, and currently is a Principal Editor for *Journal of Materials Research* and Editor for *Journal of Materials Science—Materials in Electronics*. Kao received his Ph.D. in Materials Science from University of Wisconsin-Madison in 1994. He joined National Central University (Taiwan) in 1995 as an assistant professor. He became the first director for the newly established Graduate Institute of Materials Science & Engineering at National Central University. In 2006 he returned to his alma mater, National Taiwan University, became a University Distinguished Professor in 2008, served as the Department Head of Materials Science and Engineering from 2010 to 2013, and is an Associate Dean of College of Engineering since 2017. His past administrative experience also includes serving the program manager of Materials Engineering in Ministry of Science and Technology of Taiwan.

Kao is a Fellow of the ASM and MRS-Taiwan. In 2014, he received the Brimacombe Medalist Award from TMS. He is a High Impact Research Icon of University of Malaya, Kuala Lumpur. He has authored over 140 referred journal papers, five of which reached the status of Highly Cited Papers according to Web of Science Essential Science Indicators. He has an h-index of 47. He holds 11 US and Taiwan patents. Kao is considered the leading experts on the metallurgical reactions for electronic packaging applications, and has given more than 30 invited or keynote lectures in international conferences. He presented an invited talk at the Gordon Research Conference (Plymouth State College, July 23–28, 2000), and served as a discussion leader for the same conference in 2006. In addition to his teaching and research activities, Professor Kao was an independent board member of LOTES (2006–2010), and served as consultants for many industry leading corporations, including ASUS and VIA Technologies.

KISHIO YOKOUCHI (M'02-SM'16) is now a Head of Japan Jisso-Interconnect Solutions Laboratory (J2IS). Also he is a Visiting Professor of Kanto Gakuin University.

He has been leading on development of high-end electronics interconnect technologies and thermal management technologies field on 38 years. He has been also contributing on world major societies of electronics packaging technologies, such as IEEE EPS, IMAPS, and JIEP.

He received his Master's degree in applied chemistry from Yokohama National University on 1979. And he received his Ph. D. in thermal management engineering from the Osaka University on 2008.

In 1979, Dr. Yokouchi joined FUJITSU Laboratories Ltd., where he has been mainly engaged in R&D on high-density and high-speed signal transmission interconnect technologies based on material science. During this period, he developed the world's first copper

conductor co-fired 60-layer 8-inch ceramic circuit board (the world's first LTCC), Ultra-fine pitch thin film circuit boards with low-k polymer for multi-chip modules (the world's first 2.5D packaging) for supercomputers/enterprise-servers. Also, he has been involved with development of phase change liquid cooling technologies, such as direct immersion boiling cooling applied perfluorocarbons, liquid nitrogen for HEMT super-computer, and liquid helium for Josephson device.

From 2000 to 2004, Dr. Yokouchi was the director of the Advanced Optoelectronics Technology Dept. of FUJITSU Laboratories of America Inc., where he directed R&D work on optical monolithic integrated devices and optical interconnection technologies.

From 2005, he has been Vice president, the Device & Materials Laboratories, FUJITSU Laboratories.

In 2007, He joined FUJITSU Interconnect Technologies, Ltd. (FICT) as a Vice president. In 2017, Dr. Yokouchi founded Japan Jisso-Interconnect Solutions Laboratory (J2IS).

He is also contribute as a Visiting Professor of Materials & Surface Engineering Research Institute, Kanto Gakuin University. He is the author or co-author of 55 technical presentations and publications, and invented or co-invented 72 U.S. and 100 Japanese patents. He co-authored three technical books.

PATRICK MCCLUSKEY (M: 1985, SM: 2015) (B.S.('84) Lafayette College; M.S.('86) and Ph.D. ('91), Materials Science and Engineering, Lehigh University) is a Professor of Mechanical Engineering at the University of Maryland, College Park and the Mechanical

Engineering Department's Division Leader for Electronic Products and Systems. He has over 25 years of research experience in the areas of thermal management, reliability, and packaging of electronic systems for use in extreme temperature environments and power applications. Dr. McCluskey has published three books and over 125 peer-reviewed technical articles with over 2000 citations, including over 40 articles in IEEE journals and major EPS conferences, such as ECTC and iTHERM. He has also served as technical program or general chair of IEEE conferences on high temperature electronics and integrated power electronic packaging, as well as being the organizer of the President's panel session on Power Module Integration at ECTC 2016, and panel sessions at ITHERM and ITEC. Dr. McCluskey has provided a short course on integrated thermal packaging of power electronics at ECTC and iTHERM since 2013, along with short courses at IWIPP and 3D-PEIM. He is an associate editor of the IEEE Transactions on Components, Packaging, and Manufacturing Technology, and of Microelectronics Reliability. He is a senior member of IEEE and the chair of the EPS Technical Committee on Energy and Power Electronics. He has also served as IEEE EPS representative to the Future Car Workshop. He is a fellow of IMAPS and a member of ASME and TMS/AIME.

Patrick's term will be January 1, 2019—December 31, 2020 to fill a vacated position.

New IEEE EPS Senior Members

The members listed below were elevated to the grade of Senior Member between June and November 2018.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

Takaaki Ishigure, Tokyo Section
Sukeshwar Kannan, Schenectady Section
Samuel Graham, Atlanta Section
Ikechi Ukaegbu, Kazakhstan Subsection
Florian Solzbacher, Utah Section
Wen-Sheng Zhao, Zhejiang Subsection
Irfan Ashiq, Santa Clara Valley Section
Gabor Harsanyi, Germany Section
Jonas Jonsson, Weden Section
Cherish Bauerreich, Red River Valley Section
Gerard Cummins, United Kingdom and Ireland Section
Zhongliang Deng, Beijing Section
Yew Hoong Wong, Malaysia Section
Shay Kaplan, Israel Section
Damien Lambert, France Section

Individuals may apply for Senior Member grade online at: https://www.ieee.org/membership/senior/

Congratulations to the 2019 newly elevated IEEE Fellows

Listed below are new IEEE Fellows who are members of the EPS. See a list of all EPS members who are IEEE Fellows in the IEEE Fellows Directory.

The grade of Fellow recognizes unusual distinction in the profession and shall be conferred by the Board of Directors upon a person with an extraordinary record of accomplishments in any of the IEEE fields of interest. (Bylaw I-104:11) Nominees shall:

- have accomplishments that have contributed importantly to the advancement or application of engineering, science and technology, bringing the realization of significant value to society;
- hold Senior Member or Life Senior Member grade at the time the nomination is submitted;
- have been a member in good standing in any grade for a period of five years or more preceding 1 January of the year of elevation.

The year of elevation to the grade of Fellow is the year following approval by the Board of Directors conferring the grade of Fellow. Members elevated to the Fellow grade may use the title immediately following approval by the Board of Directors.

The IEEE Fellows, an elite global group with international recognition are called upon for guidance and leadership as the world of electrical and electronic technology, continues to evolve.

Xuejun Fan, Region 5 Beaumont Section
for contributions to the modeling and characterization of electronic packaging design

Bruno Michel, Region 8 Switzerland Section
for contributions to energy efficiency for computers and solar systems

Arifur Rahman, Region 6 Santa Clara Valley Section
for leadership in 2.5- and 3-dimensional integrated circuits for field programmable gate arrays

In Memorium

The Electronics Packaging community mourns the loss of Dr. Nasser Grayeli

Our dear friend and colleague Dr. Nasser Grayeli passed away after a nearly 10-month battle against brain cancer on January 7, 2019. Nasser had an amazing 33-year career at Intel, beginning in December 1983. During this time, he made many remarkable contributions to Assembly and Packaging technology while helping shape the field and influencing the careers of countless engineers.

Nasser led the development of many of Intel's breakthrough technologies, including 6 inch wafer gold bumping and 90/70 micron Tape Automated Bonding that enabled the thinnest packages for Intel products. He was a major driving force behind the industry transition from ceramic area array packages to the more advanced, cost effective, and performance optimized organic flip-chip substrates. He also championed the removal of hazardous materials from packaging materials, making Intel the first company to eliminate lead and halogens from all of its products. Nasser led Intel's Assembly, Packaging and Test Technology Development organization for nearly a decade, establishing a highly innovative and knowledge-driven organization that ensured the development of diverse packaging technologies.

Throughout his career, Nasser was actively engaged with academia and industry forums for the advancement of Assembly, Packaging, Board, and Test technology development. He was Chairman of the Board of Directors of the International Electronic Manufacturing Initiative (INEMI), an influential member of the SRC Technical Advisory Board, and a member of SEMATECH Assembly and Packaging. Nasser received many industry-wide recognitions, including the highest award of the IEEE Components, Packaging and Manufacturing Technology (CPMT) society "for contributions to the advancement of microelectronic packaging technology, manufacturing, and semiconductor ecosystems" in 2015.

While he will be remembered as a giant in the industry, the more enduring legacy he leaves behind is his personality and the lasting positive impact he has had on many generations in our community. Nasser was a deeply empathetic, kind, and caring individual who cared about people. He was a leader who, with his unique personality, brought out the best in everyone, encouraged diverse groups to collaborate effectively, and inspired innovation. Nasser will be remembered as a great leader and will be missed by the many whose lives he influenced.

Deadline for EPS Major Awards Extended to February 8, 2019

A series of EPS Major Awards, recognizing technical contributions and service, is administered by the EPS Awards Committee:

- Outstanding Sustained Technical Contribution Award
- Electronics Manufacturing Technology Award
- David Feldman Outstanding Contribution Award
- Exceptional Technical Achievement Award
- Outstanding Young Engineer Award
- Regional Contributions Award

Guidelines for Nominators:

- An individual may submit only one nomination per award but may submit nominations for more than one award.
- An individual may submit only one endorsement per award but may submit endorsement for more than one award.
- It is the responsibility of the nominator to ensure quality documentation to assist the Awards Committee in evaluating the candidate.
- Outstanding Sustained Technical Contribution Award is designed for the "practitioner", while the Electronics Manufacturing Technology Award intended for "Corporate Leadership".
- Complimentary material, such as CV, list of publications and/or patents should be submitted separate from the award nomination.
- Self-nominations will not be considered.

Please visit the EPS Awards page for more information: https://eps.ieee.org/awards.html

PUBLICATION NEWS

New Letters Section within T-CPMT

The IEEE Transactions on Components, Packaging and Manufacturing Technology will now include a ***Letters*** section within the publication. Papers will be a maximum of 4 pages and relate to the research and application on modeling, design, building blocks, technical infrastructure, and analysis underpinning electronic, photonic and MEMS packaging, in addition to new developments in passive components, electrical contacts and connectors, thermal management, and device reliability; as well as the manufacture of electronics parts and assemblies, with broad coverage of design, factory modeling, assembly methods, quality, product robustness, and design-for-environment. The intent of the ***Letters*** section is to enable the rapid dissemination of the latest information in topics of interest to the readership of the IEEE Transactions on Components, Packaging and Manufacturing Technology and thus improve dialog across the community.

The technical content of papers must be both new and significant.

Manuscript Length: The standard length for an accepted manuscript must not exceed 4 pages. **The 4th page is reserved exclusively for references** in order to accommodate a comprehensive reference list of pre-published and to-be-published articles with full authors' names, title, and DOI (where available).

When submitting your Letters into ScholarOne, select "Letters" as paper type.

Most Popular Articles According to the November 2018 Xplore® Statistics

3-D Printed Metal-Pipe Rectangular Waveguides
Mario D'Auria; William J. Otter; Jonathan Hazell; Brendan T. W. Gillatt; Callum Long-Collins; Nick M. Ridler; Stepan Lucyszyn
Publication Year: 2015, Page(s):1339–1349

Inkjet Printing of Wideband Stacked Microstrip Patch Array Antenna on Ultrathin Flexible Substrates
Wen Tao Li; Yong Qiang Hei; Peter Mack Grubb; Xiao-Wei Shi; Ray T. Chen
Publication Year: 2018, Page(s):1695–1701

Flexible Hybrid Electronics Technology Using Die-First FOWLP for High-Performance and Scalable Heterogeneous System Integration
Takafumi Fukushima; Arsalan Alam; Amir Hanna; Siva Chandra Jangam; Adeel Ahmad Bajwa; Subramanian S. Iyer
Publication Year: 2018, Page(s):1738–1746

Electronics Thermal Management in Information and Communications Technologies: Challenges and Future Directions
Suresh V. Garimella; Tim Persoons; Justin A. Weibel; Vadim Gektin
Publication Year: 2017, Page(s):1191–1205

Die Attach Materials for High Temperature Applications: A Review
Vemal Raja Manikam; Kuan Yew Cheong
Publication Year: 2011, Page(s):457–478

Fan-Out Wafer-Level Packaging for Heterogeneous Integration
John H. Lau; Ming Li; Margie Li Qingqian; Tony Chen; Iris Xu;Qing Xiang Yong; Zhong Cheng; Nelson Fan; Eric Kuah; Zhang Li; Kim Hwee Tan; Yiu-Ming Cheung; Eric Ng; Penny Lo; Wu Kai; Ji Hao; Koh Sau Wee; Jiang Ran; Cao Xi; Rozalia Beica;Sze Pei Lim; N. C. Lee; Cheng-Ta Ko; Henry Yang; Yu-Hua Chen; Mian Tao; Jeffery Lo; Ricky S. W. Lee
Publication Year: 2018, Page(s):1544–1560

Warpage and Thermal Characterization of Fan-Out Wafer-Level Packaging
John H. Lau; Ming Li; Dewen Tian; Nelson Fan; Eric Kuah; Wu Kai; Margie Li; J. Hao; Yiu Ming Cheung; Zhang Li; Kim Hwee Tan; Rozalia Beica; Thomas Taylor; Cheng-Ta Ko; Henry Yang;Yu-Hua Chen; Sze Pei Lim; Ning Cheng Lee; Jiang Ran; Cao Xi; Koh Sau Wee; Qingxiang Yong
Publication Year: 2017, Page(s):1729–1738

A Low-Cost and High-Gain 60-GHz Differential Phased Array Antenna in PCB Process
Tao Zhang; Lianming Li; Haiyang Xia; Xujun Ma; Tie Jun Cui
Publication Year: 2018, Page(s):1281–1291

Aerosol-Printed Highly Conductive Ag Transmission Lines for Flexible Electronic Devices
Marvin Abt; Aljoscha Roch; Jubaid A. Qayyum; Svenja Pestotnik; Lukas Stepien; Atef Abu-Ageel; Brian Wright; Ahmet Cagri Ulusoy; John Albrecht; Lee Harle; John Papapolymerou; Thomas Schuelke
Publication Year: 2018, Page(s):1838–1844

A Filtering Dual-Polarized Antenna Subarray Targeting for Base Stations in Millimeter-Wave 5G Wireless Communications
Hui Chu; Yong-Xin Guo
Publication Year: 2017, Page(s):964–973

EDUCATION/CAREER NEWS

New EPS Certificate Program

In order to further the education of Electronics Packaging Society (EPS) members, the EPS is now offering a Certificate Program. The goal of this program is to give members new to electronics packaging an opportunity for further packaging education, offer continuous education in electronics packaging to existing members, and also to offer students electronics packaging training if they are in a University program that does not include packaging education.

As we approach the 3rd decade of the 21st century, with rapidly changing electronics packaging technology now a value creator and product differentiator across the electronic industry, the EPS Certificate will help distinguish the unique skills and knowledge of our members in this critical domain of science and technology," said Avram Bar-Cohen, president, IEEE Electronics Packaging Society. "The new certificate program will help ensure that IEEE EPS members are up-to-date on the latest technological advancements and the practical applications found within the electronics packaging space, while opening the door to continuous education through course studies and active participation within the Society."

Criteria: Must be an IEEE Electronics Packaging Society Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of the following:

1) IEEE EPS Webinar (1 PDH)—must complete PDH evaluation
2) Professional Development Courses—must complete survey and CEU credit form. Previous PDCs from the last 10 years can be used towards this if the CEU application was completed at the time of the course.
   - Electronic Components and Technology Conference (USA) = 4 PDHs
   - Electronic Systems-Integration Technology Conference (Europe) = 3 PDHs
   - Electronic Packaging Technology Conference (Asia) = 4 PDHs

3) Author of IEEE T-CPMT and/or EPS conference paper(s) (5 PDHs)—paper must be published in IEEE Xplore within the last 5 years.
4) Reviewer for IEEE T-CPMT (3 Reviews = 5 PDH) within the last 5 years.

Once you have completed any combination of the above and received 15 PDHs, please go to the EPS Education website - https://eps.ieee.org/education.html - and complete the form to request your Electronics Packaging Society Certificate.

Nomination Period Extended to February 8, 2019 for New EPS PhD Fellowship

Description/Objective
To promote, recognize, and support PhD level study and research within the Electronics Packaging Society's field of interest.

Prize
A plaque and a single annual award of US$5,000, applicable towards the student's research.

Eligibility
Candidate must be an IEEE EPS member, at the time of nomination, and be pursuing a doctorate degree within the EPS field of interest on a full-time basis from an accredited graduate school or institution. The candidate must have studied with her/his advisor for at least 1 year, at the time of nomination, to be eligible.

A Student who received a Fellowship award from another IEEE Society, within the same year, or is a previous EPS Fellowship winner is ineligible.

Schedule
- On-Line application available by September 15
- Complete application packages are due by February 8
- Recipients will be notified by March 15
- Formal award presentations will take place at the IEEE EPS luncheon at ECTC at the end of May.
- Monetary awards will be given by June 15 (or at ECTC)

Selection/Basis for Judging
Demonstration of his/her significant ability to perform independent research in the fields of electronic packaging and a proven history of academic excellence, as documented in:
- Nomination by an IEEE EPS Member. Only one nomination per member per year.
- Two-page (maximum) statement by the student describing his or her education and
- Research interests, accomplishments, and impact on the electronics package industry.
- Proof of contributions to the community may consist of open literature publications (preferred) such as papers, patents, books, and conference presentations and reports (available to the public).
- At least one letter of recommendation from someone familiar with the student's work
- Student resume

Go to the EPS Award page for additional information or submit a nomination online

Young Professional Event at ICEPT

The IEEE Young Professional and Graduate Student Survey in 2016 showed that networking and education are top improvement opportunities among Young Professionals (YP)—likely due to being in the early stages of their career. Based on the survey results, EPS focuses on improving networking opportunity for YP members.

EPS is planning different types of YP meet up events like panel discussion, seminars, and receptions in conferences as well as

local sessions. On August 8, 2018, the first Young Professionals Panel and Reception took place at the International Conference on Electronic Packaging Technology (ICEPT) in Shanghai, China. Dr. Xiaoliang Zeng, from Shenzhen Institute of Advanced Technology, Chinese Academy of Sciences, hosted this event. There were 33 attendees who joined this event, including ICEPT young professional registrants. One panelist, Dr. Guoping Zhang (General Manager, Shenzhen Samcien Semiconductor Materials CO., Ltd) shared his career development advice for young professionals based on his experiences and achievements in industry. This event was very informative and well received. We would like to thank the funding support from IEEE Young Professionals, as well as the great support from IEEE EPS and IEEE Shanghai Chapter.

Yan Liu
IEEE EPS Young Professional Representative

CONFERENCE NEWS

HETEROGENEOUS
INTEGRATION ROADMAP

IEEE Heterogeneous Integration Roadmap (HIR) Symposium

2nd Annual, intro to HIR v1.0, overviews, integration, working groups, participation …
HIR v1.0 Roadmap Release

Co-hosted by EPS Santa Clara Chapter & SEMI

When: February 21 - 22, 2019
Where: SEMI Headquarters, 673 South Milpitas Blvd, Milpitas, CA
Cost: $25 IEEE/ASME members, students, unemployed; $40 non-members. ($10 more after Feb. 10th) (includes lunch)
Registration waived for HIR Technical Working Group (TWG) members

Register Now: http://www.cpmt.org/scv/?p=818

Thursday, February 21, 2019: HIR Symposium
Time: 8:30 AM – 6:00 PM
Who Should Attend: Open to the General Public
Speakers: Chairs of Working Groups (from Intel, Boeing, Fraunhofer, NASA, Infineon, Google, Advantest, StatsChipPaC, Dow, ASE, ITRI, SEMI, more)

Friday, February 22, 2019: HIR Technical Working Meeting and Open House
Time: 8:30 AM – 4:00 PM
Who Should Attend: All HIR Technical Working Group members and anyone interested in participating or learning more about the Heterogeneous Integration Roadmap.
The purpose is to provide a forum for interaction, collaboration and feedback.

Information: http://www.cpmt.org/scv/?p=818

Summary: *Heterogeneous Integration* will be the key technology direction going forward, for device and subsystem integration. It is the "low hanging fruit" for initiating a new era of technological and scientific advances to continue and complement the progression of Moore's Law scaling into the distant future. Presentations from HIR Technical Working Group chairs. Corporate sponsorships/ exhibits available. The agenda for Roadmap Symposium follows:

IEEE HIR ROADMAP MORNING Program Thursday Feb 21, 2019

8:30 – 9:00 am **REGISTRATION & COFFEE**
9:00 – 9:15 am **SYMPOSIUM OPENING: William Chen** (HIR)
Welcome: Ajit Manocha, President & CEO SEMI; Nicky Lu, CTO and Founding Chairman, Etron Technology Inc, Executive Director, Taiwan Semiconductor Industry Association

Session 1
Chair: Bill Bottoms 3MTS
9:15–10:50 am **Heterogeneous Integration for High Performance**
- High Performance Computing & Data Center: Kanad Ghose (Binghamton University), Dale Becker (IBM)
- 3D & Interconnect: Ravi Mahajan (Intel)
- WLP (fan in and fan out): Rozalia Beica (DOW), John Hunt (ASE)
- Thermal Management: Madhu Iyenger (Google), Azmat Malik (Acuventures)
- Integrated Photonics: Amr Helmy (University of Toronto), Bill Bottoms (3MTS)
- Test: Dave Armstrong (Advantest)

10:33–10:50 am Q&A
BREAK

Session 2
Chair: Ravi Mahajan, Intel
11:05–12:40 pm **Heterogeneous Integration for Consumer & Industrial Applications**

- Emerging Devices: Meyya Meyyappan (NASA Ames)
- Medical and Health & Wearables: Mark Poliks (Binghamton U), Nancy Stoffel (GE)
- SiP & Module: Rolf Aschenbrenner (Fraunhofer IZM), Klaus Pressel (Infineon)
- Single Chip and Multi Chip Integration: William Chen (ASE), Annette Teng (Promex)
- Integrated Power Package: Doug Hopkins (NCSU), Patrick McCluskey (UMD)
- IoT: Robert Lo (ITRI Taiwan)

12:23–12:40 pm Q&A
12:40–1:40 pm **LUNCH**
1:40–2:25 pm **PLENARY PRESENTATION**
Invited Speaker: Babak Sabi, Corporate Vice President, General Manager of Assembly & Test Development, Intel Corporation

Session 3
Chair: Tom Salmon, SEMI
2:25–3:45 pm **Heterogeneous Integration for Special Applications**

- Aerospace & Defense: Tim Lee (Boeing)
- 5G in RF and Analog Mixed Signal: Tim Lee (Boeing), Herbert Bennett (Alta Tech)
- Cyber Security: Sohrab Aftabjahani (Intel)
- Simulation: Chris Bailey (University of Greenwich), Xuejun Fan (Lamar University)
- MEMS & Sensor Integration: Shafi Saiyed (ADI)

3:25–3:45 pm Q&A
BREAK

Session 4
Chair: Amr Helmy, Univ of Toronto
4:00–5:15 pm **Heterogeneous Integration Applications, Materials & Simulation**

- Automotive: Urmi Ray (STATS ChipPAC), Rich Rice (ASE)
- Mobile: William Chen (ASE)
- Materials & Emerging Research Materials: Bill Bottoms (3MTS)
- Supply Chain: Tom Salmon (SEMI)

4:48–5:15 pm Q&A
5:15–5:30 pm Information on Release of HIR version 1.0: Download & Roadmap Use
5:30 pm **WRAP UP: Nicky Lu, CTO and Chairman, Etron Technology Inc. Executive Director, Taiwan Semiconductor Industry Association**
SYMPOSIUM CLOSING

Ajit Manocha is the president and CEO of SEMI. Headquartered in Milpitas, California, SEMI is the global industry association serving the electronics manufacturing supply chain. Manocha, an industry leader has over 35 years of global experience in the semiconductor industry.

Manocha was formerly CEO at GLOBALFOUNDRIES, during which he also served as vice chairman and chairman of the Semiconductor Industry Association (SIA). Earlier, Manocha served as EVP of worldwide operations at Spansion. Prior to Spansion, Manocha was EVP and chief manufacturing officer at Philips/NXP Semiconductors. He began his career at AT&T Bell Laboratories as a research scientist where he was granted several patents related to microelectronics manufacturing.

Today, there is a much broader scope for SEMI to help foster collaboration and fuel growth than we could have ever imagined at SEMI's inception in 1970. This has to be accomplished without compromising the strong foundation of SEMI comprising of Equipment Suppliers and Materials makers. Given our ecosystem is rapidly expanding due to the massive explosion of applications based on the Internet and mobile devices, biomedical devices, defense, social media, artificial intelligence/machine learning, autonomous vehicles e-commerce, the Internet of Things, etc., Manocha feels it is the right time for us to evolve as the space around us evolves.

Additionally, Manocha has served on the President's committees for "Advanced Manufacturing Partnerships" and the President's Council of Advisors on Science & Technology (PCAST) during the last 4+ years.

Babak Sabi is a corporate vice president and general manager of the Assembly Test Technology Development. Since 2009, he has been responsible for the company's packaging, assembly process, packaging materials, enabling technology, and test technology development. Sabi joined Intel in 1984.

Prior to leading ATTD, Sabi led the Corporate Quality Network within Intel's Technology and Manufacturing Group from 2002 to 2009. He led a company-wide network of quality and reliability organizations responsible for product reliability, customer satisfaction and quality business practices. Previously, Sabi managed technology development quality and reliability, and was responsible for silicon technology certification, assembly, test and board processes.

Sabi received his Ph.D. in solid state electronics from The Ohio State University in 1984. He has written 10 papers on reliability physics and has received five Intel Achievement Awards. He currently holds two patents.

Nicky Lu is the CEO and Founding Chair of Etron Technology, Inc. since 1991, and co-founded several successful IC companies including Ardentec and Global Unichip. He received his B.S. in Electrical Engineering from National Taiwan University and M.S. and Ph.D. from Stanford University. He worked for IBM and won numerous IBM recognition awards including an IBM Corporate Award. He holds over 27 U.S. patents and published over 50 technical papers. He received an IEEE Solid-State Circuits Field Award for his contributions in high speed DRAM cell/array technologies and chip designs. Dr. Lu is an IEEE Fellow, a Member of the National Academy of Engineering of U.S.A.

ECTC Highlights

The IEEE EPS 69th Electronic Components and Technology Conference will be held from May 28–31, 2019 at The Cosmopolitan of Las Vegas, Las Vegas, NV. The conference will start on Tuesday, May 28th with morning and afternoon professional development courses. Special sessions will feature invited panelists to discuss the some of the most exciting topics and trends in our industry including: Transient Electronics—A Green Revolution for Packaging; Photonics on the Cutting-Edge of Technology Evolution; and Sensor Packaging for Autonomous Driving. The EPS President's Panel invites young professionals to describe the future path of packaging science and technology and propose possible scenarios for 2025. The Thursday night IEEE EPS session will feature experts to outline and discuss the Roadmap of IC Packaging materials to Meet Next-Generation Smartphone Performance Requirements. The conference will feature 36 oral sessions, four interactive presentation sessions and a student poster session. Topics of the oral sessions include: Wafer Level Fan-Out Process Integration, RDL and Additive Manufacturing, Advancements in Automotive and Power Devices, Emerging Flexible Hybrid Electronics, Technologies Enabling 3D and Heterogeneous Integration, High Bandwidth 3D and Photonic Integration, MEMS, Sensors, IoT, 5G, mm-Wave & Antenna-in-Package, RF & Power Components and Modules, and Advanced Biosensors and Bioelectronics. Also planned are student and young professional receptions, and a ECTC/ITherm Women's Panel and Reception focused on Unleashing the Power of Diversity in our Workforce. All the latest details about the 69th ECTC, conference and hotel reservations can be found at www.ectc.net.

Mark Poliks,
2019 ECTC General Chair

5G Forum in iMPACT 2018

This 5G Forum took place in Taipei, Taiwan on 10/26/2018 during the iMPACT 2018. It is a joint event of IEEE EPS Taiwan, IEEE MTTS Taiwan, and ITRI, and is sponsored by ASE. We are very happy to have IEEE EPS Taiwan honorable chair Dr. Fu, ShenLi, and IEEE MTTS Tainan Chair Dr. Jason Horng part of the organizing committee.

The speakers of the forum includes IEEE EPS Fellow Prof. Lih-Tyng Hwang from National Sun Yat-Sen University on 'Packaging Solutions and Hardware Technology for 5G Mobility', and IEEE MTTS Fellow Prof. Tian-Wei Huang from National Taiwan University on "The High-Throughput CMOS Front End for 5G mmWave Links" In addition, Miss Emilie JOLIVET from Yole talked about "5G's impact on RF Front End SiP", Dr. Wen-Chiang Chen from ITRI talked about "5G mmWave Radio Access Challenges and Development Trend", Mr. Jonathan Cho from ASE Corp R&D talked about "Organic substrate mmWave characterization", and last but not least Mr. Rong-Chung Liu CEO of WavePro talked about "5G mmWave chamber measurement". This forum is hosted by Dr. Hsin-Chin Chang from ASE Corp R&D, member of both IEEE EPS and MTTS.

Harrison Chang,
EPS Representative to the IEEE 5G Initiative

EDAPS 2018

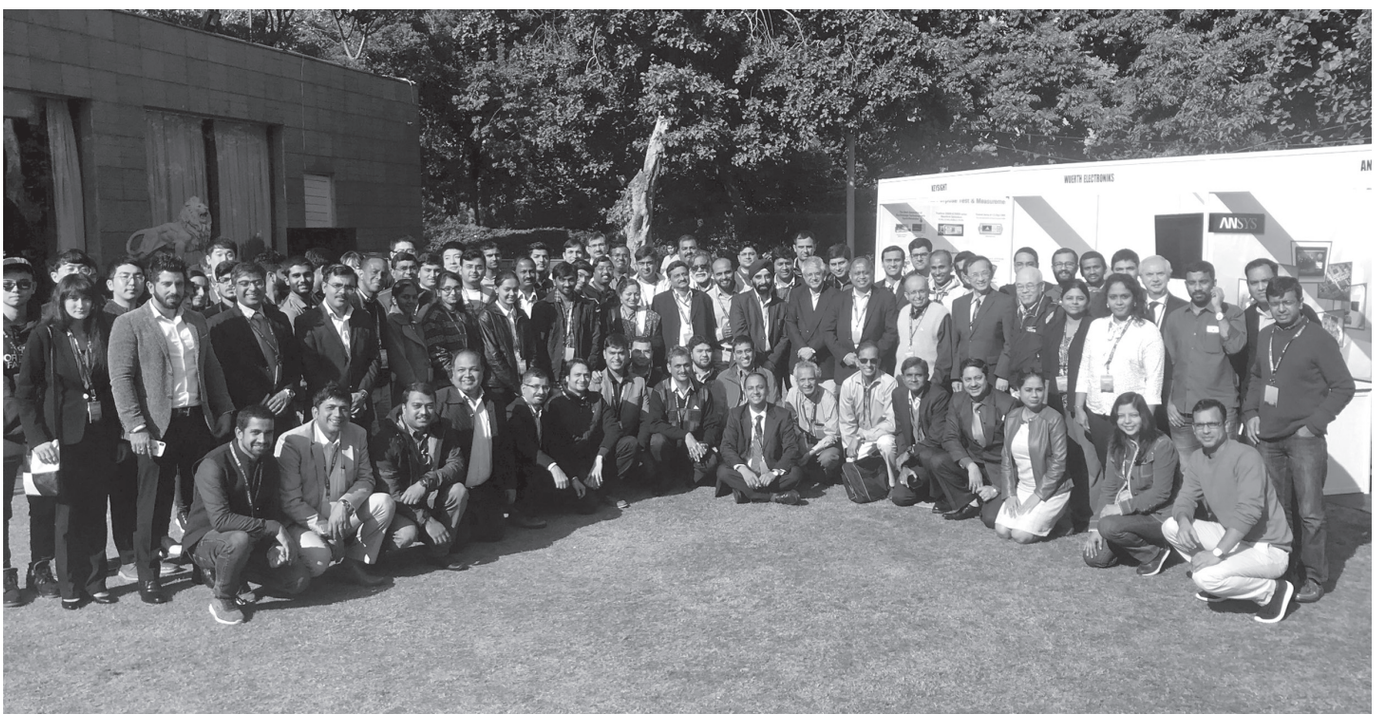
The IEEE Electrical Design of Advanced Packaging and Systems (EDAPS) conference was held at Taj Chandigarh from 16th–18th December. EDAPS is a premier packaging conference in the Asia-Pacific and it technically sponsored by the IEEE Electronic Packaging Society. This was the first time that the conference was held in North India with an aim to boost the packaging ecosystem of the region.

The conference saw tremendous participation from industry and academia with papers and posters from several countries in North America, Europe and Asia-Pacific. The conference included 3 keynotes by Ram Viswanath (Intel), M. M. Nayak (IISc, Bangalore) and L. T. Hwang (NSYSU, Taiwan). The three-day conference had four dedicated tutorial sessions from 11 leading experts from academia and industry. The tutorials focused on *Power integrity and Jitter analysis*; *Machine Learning for hardware design*; *DDR5* and *PDN design*. This year more than 50 papers and posters were presented with more than a third foreign and more than half industry participation. The technical papers and posters were organized into 9 sessions that generated tremendous participation and discussions. As a first in EDAPS, a panel discussion on Emerging Technologies and an Industry session were some of the key events during this conference.

One of the key highlights of this conference included attractive student travel grants to participating students. A record number of 14 sponsors supported this conference that included Ansys, Keysight Technologies, Tektronix, Wurth Electronics, IIT Ropar, SCL, Mohali, Intel, Cadence, Dell Technologies, Synopsys, Mathworks, IIT Mandi and the Center for Co-Design of Chip, Package, System.

A unique highlight of this year's EDAPS included a mesmerizing cultural programme by *Sitar* maestro Nayan Ghosh in jugalbandi with Ishaan Ghosh on *Tabla*. The organizing committee of the conference undertook a green initiative by no use of plastics during the entire conference.

Rohit Y. Sharma,
EDAPS 2018 Conference Chair



Call for Papers & Proposals has been Extended! Registration is now Open.

The 2019 IEEE 5th World Forum on IoT (WF-IoT 2019) will be held on the spectacular parkland setting of the University of Limerick 15–18 April 2019. The historic city of Limerick is located in the heart of the beautiful mid-west region of Ireland, on the magnificent Wild Atlantic Way. We look forward to extending a very special Irish welcome. and invite you to join us in 2019 for a truly memorable event

The broad-reaching program at WF-IoT attracts industry practitioners, government regulators, public-sector executives, as well as researchers and academics interested in the latest developments, new standards, technical innovations, and first-hand experiences with commercial offerings. This year's theme is "IoT and the Digital Revolution."

Call for Papers and Proposals
We are seeking submissions for original technical, vertical and doctorial symposium papers, as well as proposals for workshops, special sessions, and tutorials relating to IoT technologies and applications.

For details on the areas and topics of interest, please click on the links below:

Call for Technical Papers—NEW DEADLINE: December 14
- IoT Enabling Technologies and Vertical IoT Applications & Services
- Technical Vertical and Topic Areas
- Papers for Doctorial Symposium
- Papers for Workshops

Call for Proposals—NEW DEADLINE: November 30
- Special Sessions
- Workshops

Call for Proposals—NEW DEADLINE: December 14
- Vertical and Topical Areas
- Industry Forum
- Tutorials
- Entrepreneurship and Innovation Workshops

Advanced Registration is Now Open!
Participants will gather to present research results, share visions and ideas, obtain updates on latest technologies and expand professional and social networking. This 4-day event includes a diverse technical program for practitioners, policy makers, and executives delivered by distinguished experts from industry, academia and the public sector. All conducted in a relaxing environment accompanied by industry exhibition and an excellent social program which includes an entertaining banquet to be held at the world-famous Thomond Stadium, home of Muster Rugby.

Go to the WF-IoT website for more details: http://wfiot2019.iot.ieee.org/

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IEEE invites you to showcase your organization, products, and services to a global audience of nearly 1,000 key industry decision makers, public sector administrators, and renowned researchers, creating the Internet of Things. Both sponsorship and exhibit opportunities are available.

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Martin Hayes martin.j.hayes@ul.ie
Karen Pannullo k.pannullo@comsoc.org

For more information, visit the WF-IoT 2019 website

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The Holm Conference Organization Announces the

65th IEEE Holm Conference on Electrical Contacts

15-18 September 2019
The Pfister Hotel
Milwaukee, WI, USA

Sponsored By:

The Electronics Packaging Society of The Institute of Electrical and Electronics Engineers, Inc.

IEEE EPS

65TH IEEE HOLM CONFERENCE ON ELECTRICAL CONTACTS

IEEE Meeting & Conference Management
445 Hoes Lane
Piscataway, NJ 08855, USA

Visit us on the Web at: www.ieee-holm.org

2019 Call for Papers
Technical Areas

AUTOMOTIVE

Hybrid/Electric Power	Hot Plugging
Switching &Connectors	Environmental Effects

ELECTRONIC CONNECTORS

High Frequency	High-Speed Data
Telecommunications	Lubricants
Corrosion Inhibitors	

POWER CONNECTORS

Crimp Connections	Bolted Connections
Plating/Lubricants	Glowing Contacts
Degradation Effects	

CONTACT MATERIALS

Air and Vacuum	High Frequency Relays
Ultra Miniature Relays	Carbon Fiber
Degradation Mechanisms	Reed Relays
Material Development	Switching Performance
Electroplating	Lead Free

DEGRADATION MECHANISMS

Switching Performance	Environmental Effects
Welding	Reliability
Breakdown	Diagnostics
Fretting	

ARC INTERRUPTION

DC/AC Switching	Circuit Breakers
Vacuum Interrupters	Hybrid Switching
Micro-Arcing	

MODELING

Fundamentals	Dielectric Breakdown
Arc Simulation	Dynamic/Static Welding

NEW TECHNOLOGY

MEMS	Micro Switches
RF Connectors	Arc Fault/Safety
Nanotechnology	Superconductors
Higher DC Voltage Switching	

HOLM 2019

The 65th IEEE Holm Conference on Electrical Contacts will be held from September 15-18, 2019 at the Pfister Hotel, Milwaukee, WI, USA.

IEEE uploads the Holm Conference Proceedings to all relevant databases including the Engineering Index. Prospective authors should submit a brief abstract (200 words maximum) online before February 8, 2019. For abstract submissions and the latest information regarding the conference, please visit the Holm Conference Website at:

www.ieee-holm.org

IMPORTANT DATES

February 8, 2019	Abstract Deadline
February 22, 2019	Notification of Acceptance
April 19, 2019	Completed Paper Deadline
September 15, 2019	Conference Begins

CORRESPONDENCE ADDRESS

IEEE Meeting & Conference Management
65th IEEE Holm Conference (2019)
445 Hoes Lane
Piscataway, NJ 08854
tel: +1 800 810 4333 or
fax: +1 732 465 6447
email: holmreg@ieee.org

22nd EUROPEAN MICROELECTRONICS AND PACKAGING CONFERENCE & EXHIBITION

www.empc2019.org

The Structures of Microelectronics

Pisa, the charming city in the famous Tuscany region, is a visitors' paradise. The International Airport "Galileo Galilei" is only 2.7 km away from the Conference Centre and it has become one of the main Italian airports with flights to over 74 destinations all around Europe and globally. It is also a hub for low-cost airlines (www.pisa-airport.com). The venue is easy to access also via public transportation, railway and car.

EMPC-2019 in Pisa offers the best of microelectronics packaging and interconnection technologies, providing top quality coverage of technological innovation in this field. The four days will comprise Tutorials/Short Courses and the Conference and Exhibition during 16th to 19th September at the Palazzo Dei Congressi, an ideal venue which includes excellent lecture auditoria, exhibition space and a great social venue. The event will be complemented by social events for which IMAPS has a great tradition. Pisa, where tradition, art, culture and business meet harmoniously, is ideal also to extend your visit.

Researchers and innovators in industry and academia are cordially invited to submit papers on the range of Microelectronics Technologies and Photonics Technologies, for oral or poster presentation at the Conference. All oral and poster presentations will be assessed to the same standard and accorded the same value. The full papers presented as oral or posters will be eligible for inclusion in IEEE Xplore and IMAPS Source.

Please visit **https://www.conftool.org/empc2019** to set up an account and upload your Abstract

Sponsored by iMAPS Europe

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In collaboration with AEIT 1897, Fondazione INPHOTEC

CALL FOR ABSTRACTS

TOPICS

ADVANCED PACKAGING: Single Chip and Multi Chip Packaging, Wafer Level Packaging, 3D-WLP, 3D-IC, CoB, SiP, SoC, Systems-Integration Technologies, Embedded Passives on Wafers and Substrates, High Frequency and High Power Packaging, LTCC Technologies, Micro-Vias and Build-Up Technologies, Lab-on-Chip, Lab-on-Substrate, Molecular Electronics.

SUBSTRATE TECHNOLOGIES: Inorganics, Organics, Co-fired, Flexibles, HD PCBs, Laminates, Printed, Microfluidics, Substrates Design and Technologies.

INTERCONNECTION TECHNOLOGIES: Thick and Thin Film Technologies, Wire Bonding, Bumping, Flip Chip Bonding, Cu/Low-k Wafers, Through Silicon Vias, Advances in Soldering, Adhesive Joining, Connectors.

MORE THAN MOORE: The future of IC shrinkage, the future options for IC packaging.

MEMS: MEMS Based Sensors and Actuators Packaging, RF-MEMS, Optical MEMS, Bio-MEMS, WiFi modules

OPTOELECTRONICS: Silicon Photonics, Power LED Assembly, Packaging and Light Guiding, Packaging of Optoelectronic Modules suitable for Gb/s Fibre Optic Communication, LiFi modules.

SOLAR ENERGY & PHOTOVOLTAICS: Packaging Design to improve Efficiency of Photovoltaic modules, Reliability and Qualification Approaches.

NANO TECHNOLOGIES: Smart Materials, Interconnections, Nano-Scale Packaging: Applications and Reliability.

GREEN ELECTRONICS: Recovery and Recycling, Base material technologies.

MEDICAL ELECTRONICS: Applications, Design, Development, Manufacturing that comply with complex and demanding regulations and market requirements.

POWER ELECTRONICS: Application in Consumer, Telecom, Automotive, Wearable, Space and Defence, Fuel Cells, Battery Technologies.

SMART TEXTILES: Wearables, Materials, Technologies, Applications, Markets, Reliability.

MANUFACTURING TECHNOLOGIES AND MATERIALS: Process Development, New Equipment, Clean Room Technologies, Yield Improvement, Cost and Cycle Time Reduction, Green Manufacturing, Micromachining, Dispensing, Printing, Deposition, Adhesives, Encapsulants, Underfills, Moulding Compounds, Advanced Solder Alloys, Halogen Free Materials, Dielectrics, Ceramics.

MODELLING: Electrical Modelling and Signal Integrity: Time and Frequency Domain Analysis of Interconnection and Packaging Technologies, Thermal Characterisation and Cooling Solutions, Modelling and Simulation Methodology for Characterisation of Advanced Packaging, Modules and Systems, Novel Cooling Techniques, Mechanical Modelling and Structural Integrity, Thermo-Mechanical Stress Analysis, Vibration and Shock Tests.

THERMAL MANAGEMENT: Techniques, Heatsinks, Heat pumping.

RELIABILITY and QUALITY: Specialised topics, Components, Counterfeits, Board and System Level Reliability Assessment, Failure Analysis, Interfacial Adhesion, Accelerated Testing, Reliability Engineering, Inspection and Test, Obsolescence Engineering, Prognostics.

COMPUTING: Ambient Intelligence methods and products, Circuits and Systems, Touch Screen technologies.

APPLICATIONS: Medical, Bio-Tec, Telecoms, Mobile, Smart Phones, RFID, Automotive, Aerospace, Robotics, Consumer, Structural.

BUSINESS ASPECTS: Electronics and Photonics, In-house or Outsource?, Markets, Supply Chain, Distribution, Microelectronics packaging and assembly industry.

EMPC 2019 Committee

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Executive & Exhibition Chair	Luigi Calligarich	Electron Mec
Financial Chair	Luca Agostoni	GestLabs

Venue: Conference and Exhibition will be held at Palazzo dei Congressi, Pisa - Italy - www.palazzodeicongressi.pisa.it
Abstract submission opening: June 2018
Deadline for abstract submission: January 15th 2019
Deadline for paper submission: June 30th 2019
A copy of the full paper must be submitted to be included in the event Proceedings and databases.

Organizing Secretariat EMPC 2019: IMAPS ITALY c/o Pragma Congressi srl
C.so Mazzini, 14 - 27100 Pavia – Italy Tel. +39 0382 309579 - Fax: +39 0382 304892 - info@empc2019.org - www.empc2019.org

EMAP 2018

The 2018 20th International Conference on Electronic Materials And Packaging (EMAP 2018) was a great success. It was organized by IEEE EPS Hong Kong Chapter, the Hong Kong University of Science and Technology (HKUST) and co-organized by Center for Advanced Microsystems Packaging (CAMP). Established in 1999, EMAP is an annual international conference which rotates among major countries and regions in Asia. The purpose of the conference is to promote awareness of new advances in materials, design and simulations, fabrication, reliability, and thermal management of microsystem/MEMS packages. It was the fourth EMAP held in Hong Kong and there were 150 attendees came to celebrate the 20th anniversary of EMAP.

In the four-day program, we have had 2 short courses, 8 keynotes speeches, 14 invited talks and more than 50 technical presentations. Professors, researches, students and expertise from the US, Europe, Japan, Korea, China, Taiwan, Malaysia and Hong Kong shared their ideas and experiences with us.

EMAP 2018 emphasized on interactive discussion. Speakers of each regular paper first gave a 5-minute presentation in the technical session. They then discussed with others face-to-face in front of posters in the interactive sessions. This arrangement provided a valuable platform for us to share our experiences and thoughts with each other. After the technical sessions, we had our banquet gathering at the Hong Kong Jockey Club. Horse racing is one of the most popular sports in Hong Kong. On the last day of the program, we went to Hong Kong UNESCO Global Geopark and had a technical site visit to ASM.

EMAP 2018 had brought us together, allowed us to reconnect with the old friends and make new ones at the same time. Everyone enjoyed their stay in Hong Kong and looked forward to meeting again in the coming conferences.

Top Conference Papers based on 2018 Usage

Electronic Components and Technology Conference (ECTC), 2018 IEEE 68th

(held on May 29 2018–June 1, 2018)

A 77 GHz Antenna-in-Package with Low-Cost Solution for Automotive Radar Applications
Cheng-Yu Ho; Sheng-Chi Hsieh; Ming-Fong Jhong; Chen-Chao Wang; and Chun-Yen Ting

Heterogeneous Integration Technology Demonstrations for Future Healthcare, IoT, and AI Computing Solutions
John Knickerbocker; R. Budd; B. Dang; Q. Chen; E. Colgan; L.W. Hung; S. Kumar; K. W. Lee; M. Lu; J.W. Nah; R. Narayanan; K. Sakuma; V. Siu; B. Wen

Mm-Wave Antenna in Package (AiP) Design Applied to 5th Generation (5G) Cellular User Equipment Using Unbalanced Substrate
Ying-Wei Lu; Bo-Siang Fang; Hsuan-Hao Mi; Kuan-Ta Chen

A Compact 27 GHz Antenna-in-Package (AiP) with RF Transmitter and Passive Phased Antenna Array
Mei Xue; Mei Xue; Mei Xue; Liqiang Cao; Liqiang Cao; Qidong Wang; Qidong Wang; Delong Qiu; Delong Qiu; Jun Li; Jun Li

Cryogenic Qubit Integration for Quantum Computing
Rabindra Das; Jonilyn Yoder; Danna Rosenberg; David Kim; Donna-Ruth Yost; Justin Mallek; David Hover; Vladimir Bolkhovsky; Andrew Kerman; William Oliver

Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm), 2018 17th IEEE Intersociety Conference on

(held on May 29–June 1, 2018)

Thermal Performance Comparison of Advanced 3D Packaging Concepts for Logic and Memory Integration in Mobile Cooling Conditions
Herman Oprins; Vladimir Cherman; Eric Beyne

The Heat Conduction Renaissance
Aditya Sood; Eric Pop; Mehdi Asheghi; Kenneth E. Goodson

Analysis of Thermal Characteristics of Gallium Oxide Field-Effect-Transistors
Jialuo Chen; Zhanbo Xia; Siddharth Rajan; Satish Kumar

Artificial Neural Network Based Prediction of Temperature and Flow Profile in Data Centers
Jayati Athavale; Yogendra Joshi; Minami Yoda

Thermal Management Strategies for a High-Frequency, Bi-Directional, On-Board Electric Vehicle Charger
Kshitij Gupta; Carlos Da Silva; Miad Nasr; Amir Assadi; Hirokazu Matsumoto; Olivier Trescases; Cristina H. Amon

Electronic System-Integration Technology Conference (ESTC), 2018 7th

(held on September 18–21, 2018)

Roles and Requirements of Electronic Packaging in 5G
Ivan Ndip, Klaus-Dieter Lang

Embedding and Interconnecting of Ultra-Thin RF Chip in Combination with Flexible Wireless Hub in Polymer Foil
Golzar Alavi; Sefa **özbek**; Mahsa Rasteh; Markus Grözing; Manfred Berroth; Jan Hesselbarth; Joachim N.Burghartz

Silver Sintering in Power Electronics: The State of the Art in Material Characterization and Reliability Testing
Marco Schaal; Markus Klingler; Bernhard Wunderle

Curved Full-Frame CMOS Sensor: Impact on Electro-Optical Performances
Bertrand Chambion; Stephane Caplet; Jan Martin Kopfer; Aurelie Vandeneynde; Wim Diels; Alexandre de Kerckhove; Patrick Peray; David Henry

Future Interconnect Materials and System Integration Strategies for Data-Intensive Applications
Pushkar Apte; Tom Salmon; Richard Rice; Mark Gerber; Rozalia Beica; Jeff Calvert; Dave Hemker; Yezdi Dordi; Manish Ranjan; Suresh Ramalingam; Jaspreet Gandhi; Alireza Kaviani; Subhasish Mitra; Philip Wong; Vincent Lee Stanford; Mohamed El-Sabry

Electronics Packaging Technology Conference (EPTC), 2017 IEEE 19th

(held on December 6–9, 2017)

Integration benefits and challenges on Fan-Out to enable system in package for IoT/Wearable Devices
Humi Tang; Max Lu; Jensen Tsai; Jase Jiang; Honda Cheng; Terrence Lu; Yu-Po Wang

2.5D Silicon optical interposer for 400 Gbps electronic-photonic integrated circuit platform packaging
Do-Won Kim; K. Y. Au; Hong Yu Li. Xianshu Luo; Yong Liang Ye; Surya Bhattacharya; Guo Qiang Lo

Reliability of wearable electronics—Case of water proof tests on smartwatch
Yuk-ngang Zita Yip; Ze Zhu; Yan-cheong Chan

128 x 128 silicon photonic MEMS switch package using glass interposer and pitch reducing fibre array
How Yuan Hwang; Padraic Morrissey; Jun Su Lee; Peter O'Brien; Johannes Henriksson; Ming C. Wu; Tae Joon Seok

Chip-to-Wafer (C2W) flip chip bonding for 2.5D high density interconnection on TSV free interposer
Sharon Pei-Siang Lim; Mian Zhi Ding; Masaya Kawano

Upcoming EPS Sponsored and Cosponsored Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the EPS sponsors and supports a number of global and regional conferences, workshops and other techical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through IEEE Xplore.

Name: 2019 20th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)
Location: Hannover, Germany
Dates: Mar 24, 2019–Mar 27, 2019

Name: 2019 IEEE International Workshop on Integrated Power Packaging (IWIPP)
Location: Toulouse, France
Dates: Apr 24, 2019–Apr 26, 2019

Name: 2019 30th Annual SEMI Advanced Semiconductor Manufacturing Conference (ASMC)
Location: Saratoga Springs, NY USA
Dates: May 6, 2019–May 9, 2019

Name: 2019 IEEE 69th Electronic Components and Technology Conference (ECTC)
Location: Las Vegas, NV USA
Dates: May 25, 2019–Jun 2, 2019

Name: 2019 18th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)
Location: Las Vegas, NV USA
Dates: May 29, 2019–May 31, 2019

Name: 2019 IEEE 8th International Workshop on Advances in Sensors and Interfaces (IWASI)
Location: Otranto, Italy
Dates: Jun 13, 2019–Jun 14, 2019

Name: 2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI)
Location: Chambéry, France
Dates: Jun 18, 2019–Jun 21, 2019

Name: 2019 IEEE Holm Conference on Electrical Contacts
Location: Milwaukee, WI USA
Abstract Submission Date: Feb 8, 2019
Dates: Sep 14, 2019–Sep 18, 2019

Name: 2019 22nd European Microelectronics and Packaging Conference & Exhibition (EMPC)
Location: Pisa, Italy
Abstract Submission Date: Jan 15, 2019
Dates: Sep 16, 2019–Sep 19, 2019

What Engineers Do

Introduction

I was invited to author a series of articles for the IEEE EPS Newsletter. I plan to write in the spirit of a former Librarian of Congress, Daniel Boorstin (1914–2004), who begins one of his books with the line "my hero is man the discoverer." To this end, I will provide a series of vignettes. Each of these will sketch what, at first glance, appears to be a trivial contribution to the art of electronics, but I will show that these contributions, in total, enabled the development (viz., discovery) of modern electronics technology. To me, these sorts of contributions are the essence of the work done by the membership of the Electronics Packaging Society. As Henry Petroski wrote, "Though ours is an age of high technology, the essence of what engineering is and what engineers do is not common knowledge". So in addition to elucidating often underappreciated innovations, I also aim to unzip the social fabric in which engineering is pursued.

We might describe engineering as product design in the context of business (viz., economics), and we might use popular business quips such as engineering "contributes to the bottom line" or provides "value added". These descriptions make the presumption that there is a market for the product. Even the quest of whether there is a market for a product assumes that there is a market.

The market system, as we know it, began during the 18th century. Trade existed back in antiquity but was not embodied in our elaborate market system of land, labor, and capital. One of the kingpins of the market system is the legal structure under which regulations derive. Without a market system, there can be no engineering, at least as we know engineering. Those who regulate engineering must be informed about engineering, and, per Petroski, regulators likely know less about engineering than engineers. Therefore, economics should be included in these stories.

I feel that engineering parallels the ancient parable of the blind men and the elephant. In that parable, an elephant walks into a village and is approached by a group of blind men. Each blind man touches one part of the elephant and proclaims his observations. The moral of the parable is that there is only one elephant but many viewpoints. As professionals, we should keep the elephant, the "truth", in clear focus as we perform each of our assignments, whether that assignment is circuit design, manufacturing, board layout, firmware, chassis design, integration, agency compliance, warrantee determination or any of the other engineering tasks.

Daniel Donahoe
IEEE Senior Member

Permanent Magnets

Naturally occurring minerals with magnetic properties were discovered by humans in prehistory, and were known as "lodestones". The first syllable is a word taken from Old English word for "journey". The simple compass may be the first electronic product. Therefore, I thought that permanent magnets (PMs) would be an appropriate starting choice for a series of short articles on electronics packaging.

To describe PM performance, it is helpful to begin with a brief summary of the most important performance metrics, which includes coercivity, magnetic energy, Curie point and price. The first two of these parameters are defined as points along the hysteresis loop traced by varying current with the core wrapped in wires in a solenoid configuration. Coercivity is the magnetic field strength (H field) required to demagnetize a PM; coercivity can be thought of as the PM's staying power (the reason for the adjective "permanent" modifying the noun "magnet"). Its SI unit is Amp/meter. The PM's remaining magnetic flux density (B field) at zero applied H field is known as remnance; its SI unit is the Telsa. Similarly, the magnetic energy is the energy stored in the PM's field; the SI unit is Joules per cubic meter. In undergraduate physics, you may have been introduced to these metrics in cgs units which, in the same order, are the Oersted (Oe), Gauss (G) and their energy product as MGsOe. Curie point is the temperature [K] at which magnetization is lost and, thus, the PM's maximum operating temperature is bounded from above by this limit.

Permanent magnets reside quietly in almost every electronics product. PMs are in electric generators and motors, in actuators and control devices, in instruments, in sound generating devices, in electron beam devices, and filters. Given the pervasiveness of PMs in products and their long technology history, the continuing innovation in PM materials is remarkable. These new materials enabled novel electronics packaging. Moreover, the advances and manufacturing of PMs has been driven by both governments and free market forces. As a result, the PM market has been estimated at over 20 B$ annually.

Over the 20th century, PM energy density increased by approximately a factor of 50. PM families introduced in the 20th century began with improvement in steel alloy magnets, and led to Alnico magnets, ferrite magnets (ceramic), and rare earth magnets. In the 21st century, work continues in the hope of eliminating or reducing the use of rare earth elements in PMs. All these PM's are based on alloying, and, therefore, alloying material price is important. The price of mined commodities is surprisingly volatile (order of magnitude swings) due to scarcity of economically available deposits (rare earths are found as ore), national political forces, safety and environmental regulatory requirements, and mine owner's business response to demand fluctuations. Furthermore, these remarkable material accomplishments are, in fact, part of "nanotechnology", a term made popular in the 1990s by Nobel Laureate Richard Smalley.

Ferrite magnets were invented in Japan in 1930 by Takeshi Takaei. Ferrites (MFeO) are non-conducting, minimizing eddy currents in RF applications. A Japanese patent was issued to Yogoro Kato and Takei in 1932. The corporation today known as TDK began to manufacture ferrite products in 1937. Of course, World War II (WWII) intervened, and ferrite components were used in Japanese military radios. Jacob Snoek at Philips filed a US patent (US 2,452,529) for ferrites in 1945 (and in other countries). After

WWII, Philips and TDK disputed patent rights. Unfortunately, Jacob Snoek died in an automobile crash in Indiana in 1950. Nevertheless, the work done by these innovators around the world and others has had profound impact on electronic products. The ferrite PM market is today on the order of 20% of all PMs. Ferrite PMs can be manufactured by bonding with a polymer (into required shape, inexpensively) or by sintering into denser parts.

Early mainframe computers used ferrite core memories. These were "soft" ferrites, meaning these were ferrites with low coercivity that could be demagnetized or magnetized easily. Soft ferrites are also used in high frequency switching power supplies and radio frequency devices where switching losses must be minimized, as described previously.

Ferrites are used in magnetic strip cards such as your credit card; if the magnetic strip is a black color, it is most likely a ferrite. Ferrites are used in many other applications, largely due to ease of manufacturing.

In 1931 Tokushichi Mishima, also in Japan, began (US 2,027,997) a long technical evolution leading to what became known as Alinco magnets (FeCoNi). By 1960, Alnico represented three quarters of all magnet production. Today, other technologies are displacing Alnico magnets.

What we call "rare earth" permanent magnets were invented in the United States and perfected, if that is the right word, in Japan. Karl Strnat invented the first of the rare earth magnets (SmCo) while working for the United States Air Force (US 3,540,945). Rare earth PMs were incorporated in microwave products soon thereafter (US 3,755,706). The Neodymium Iron Boron (NdFeB) magnet was invented by Sumitomo Special Metals in 1983 (US 4,792,368 and 4,770,723), and this type of magnet dominates the PM market today.

The Neodymium rare earth magnet has driven product designs using any type of motor or actuator. The first patent I found in which these RE magnets appear in a brushless DC motor was by Lordo and Rudlisch in 1989 (US 4,839,547). RE magnets provide smaller size, higher performance than previous motors. Rare earth PMs (PEPMs) are used in small form factor disk drives (US 5,025,336). In handheld tools, REPM motors have provided better balance and increased power (US 5,856,715). REPM motors are incorporated in hybrid electric vehicles. REPMs have also moved into acoustic speakers (US 5,802,191).

Thus permanent magnet technology advanced dramatically over the last century and that foundational technology diffused rapidly into all types of electrics products, enabling dramatic improvements in performance and substantial reductions in size, weight, power, and cost (SWaP-C). At least in the case of acoustic products, modern permanent magnets truly "rock our world".

Daniel Donahoe
IEEE Senior Member

Dan Donahoe Bio

I was born in Wisconsin as were my relatives on both sides of the family gong back approximately 175 years. My own technical heart is in the field we know as "electronics packaging". By that term, I refer to the technical and managerial tasks of brining electronic products into reality as products.

In my professional life, I have worked for Lockheed, Motorola, Ford Aerospace, Teledyne, Compaq Computer, Iomega, Exponent—Failure Analysis Associates, a consulting practice I named "1000 kilometers", and the United States Air Force. In academic roles, I have worked for the University of Illinois, the University of Maryland, and Maricopa County Junior Colleges.

I have served as IEEE CPMT chapter chair in Santa Clara Valley and as an Associate Editor (AE) of the related CPMT Transactions and as Member At Large (MAL) on the IEEE CPMT Board. In addition to CPMT, I have been very active in other roles in IEEE. In 2018 I chaired an ad hoc committee for TAB on economics. I served two years on the IEEE-USA Board as MAL. I have served as an AE for IEEE Access. I have served as a conference chair for SusTech. Beyond IEEE, I have participated in other professional societies and community endeavors. In 2019, I am beginning a term on the University of Illinois Industrial and Enterprise Systems Engineering Alumni Board.

I earned bachelors and masters degrees from the University of Illinois at Urbana-Champaign, an MBA from Santa Clara University, and a PhD from the University of Maryland in College Park. I am a licensed professional engineer in several states.

MISCELLANEOUS

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