IEEE Heterogeneous Integration Roadmap: Aerospace and Defense (HIR-A/D)

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Heterogeneous Integration Roadmap (HIR)
Driving Force and Enabling Technology for Systems of the Future

Introduction to Heterogeneous Integration Roadmap
Lesson from our Industry’s Foremost Prophet:

“Cramming more Components onto Integrated Circuits”

“Day of Reckoning........It may prove to be more economical to build large systems out of smaller functions, which are *separately packaged and interconnected*. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both *rapidly and economically*.”
40 Years Of Progress In Computing

Source: John Hennessy (Chairman Alphabet) Plenary presentation at DARPA ERI Conference July 23 2018
Progress in processor performance has slowed.
40 Year DRAM Memory Capacity Increase

Source: John Hennessy (Chairman Alphabet) Plenary presentation
“End of Moore’s Law, a New Golden Age” at DARPA ERI Conference July 23 2018
40 Year DRAM Memory Capacity Increase

Source: John Hennessy (Chairman Alphabet) Plenary presentation
“End of Moore’s Law, a New Golden Age” at DARPA ERI Conference July 23 2018

Progress in functional density has slowed
Moore’s Law Economics Meeting Headwinds


**WHILE COSTS CONTINUE TO INCREASE**

Cost Per Yielded mm² for a 250mm² Die

INCREASING DIE SIZES ARE ECONOMICALLY PROBLEMATIC
Semiconductor Technology Roadmap History


1998: NTRS expanded forming the first Global Technology Roadmap. Europe, Japan, Taiwan, and Korea joined. It was renamed International Roadmap for Semiconductors (ITRS).

2014: The benefits of Moore’s Law scaling diminish and decision was made to end ITRS.

2015: The ITRS Heterogeneous Integration Focus Team signed an MOU with the IEEE CPMT Society initiating the formation of the Heterogeneous Integration Roadmap. HIR was founded with initiative from three IEEE Societies (Electronics Packaging Society, Electron Devices Society, Photonics Society) together with SEMI and ASME EPPD.

2016: The last edition of the ITRS was published July 8, 2016.
Packaging Roadmap Metrics: Slow Progress in ITRS

Wire bond pitch *increased* on the roadmap with shift from Au to Cu to decrease cost

PCB solder ball pitch roadmap just *pushed out laterally* for years
The Definition of Heterogeneous Integration

Heterogeneous by material, component type, circuit type, node, bonding/interconnect method, and sources

Graphics Source: John Hunt (ASE)
Homogeneous Integration to Heterogeneous Integration

1st and 2nd Generations of the AMD EPYC Processors


Left is large die split into 4 “chiplets” die (14nm) tightly coupled on an organic substrate

Right are 4 groups of 2 “chiplets” (7nm) on each side of larger I/O die (14nm) tightly coupled on an organic substrate
HIR International Roadmap Committee

- William (Bill) Chen, ASE Fellow & Senior Technical Advisor, (Chair)
- W. R. (Bill) Bottoms, Chairman 3MTS (Co-Chair representing EPS)
- Subramanian Iyer, Distinguished Professor UCLA (representing EDS)
- Amr Helmy, Chair Professor, U. of Toronto (Representing Photonics)
- Tom Salmon, VP SEMI Collaboration Platform (Representing SEMI)
- Ravi Mahajan, Intel Fellow (Representing ASME EPPD)
- Gamal Refai-Ahmed, Distinguished Engineer Xilinx (ASME EPPD alternate)
HIR Global Advisory Council

• Ajit Manocha: President and CEO of SEMI. Former CEO of GlobalFoundries and served as chair of SIA. Also served in executive roles at Philips/NXP & Spansion.

• Nicky Lu: Founder and Chairman of Etron Technology in Taiwan. Served as chair of TSIA and WSC and is a member of the US National Academy of Engineering.

• Babak Sabi: Intel Corporation Corporate Vice President, General Manager, Assembly Test Technology Development.

• Hubert Lakner: Board of Directors Chairman, Fraunhofer Microelectronics Group and Founding Director of Fraunhofer Institute of Photonic Microsystems (IPMS) in Dresden.
Heterogeneous Integration Roadmap
Technical Working Groups

HI Market Applications
- High Performance Computing & Data Center
- Mobile
- Medical, Health & Wearables
- Automotive
- IoT
- Aerospace & Defense

Heterogeneous Integration Components
- Single Chip and Multi Chip Integration
- Integrated Photonics
- Integrated Power Electronics
- MEMS & Sensor Integration
- 5G RF and Analog Mixed Signal

Cross-Cutting Topics
- Materials & Emerging Research Materials
- Emerging Research Devices
- Test
- Supply Chain
- Security
- Thermal Management

Integration Processes
- SiP
- 3D + 2D & Interconnect
- WLP (fan in and fan out)

Design
- Co-Design & Simulation – Tools & Practice

Download HIR Chapters: http://eps.ieee.org/hir
Mission Statement for HIR – Aerospace / Defense (A/D)

• The mission of Heterogeneous Integration Roadmap for Aerospace and Defense is to provide guidance and recommend solutions to the profession, industry, academia and government to identify key technical challenges with sufficient lead time that they do not become roadblocks preventing the continued progress in Aerospace and Defense electronics.

• There is the need to address heterogeneous integration technologies for new capabilities for embedded high-speed computing, cyber, sensors, C4ISR and RF/analog for unique sets of requirements, production volumes and lifecycle timelines.

• That progress is essential to the future growth of the industry and the realization of the promise of continued impact on aerospace, defense and security applications.

• The approach is to identify the requirements for heterogeneous integration in the A-D electronics industry with 5-, 10- and 15-year horizons, determine the difficult challenges that must be overcome to meet these requirements and, where possible, identify potential solutions and synergies between the greater commercial sectors and the smaller A-D community.
PISCATAWAY, N.J.--(BUSINESS WIRE)--IEEE, the world's largest technical professional organization dedicated to advancing technology for humanity, today announced the 2019 release of the Heterogeneous Integration Roadmap (HIR), a roadmap to the future of electronics identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration among industry, academia and government to accelerate progress. The roadmap offers professionals, industry, academia and research institutes a comprehensive, strategic forecast of technology over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of emerging devices and materials with longer research-and-development timelines.
Backdrop to A & D Electronics
Future Warfighting Systems
Future Warfighting Systems

Complex and Evolving Battlespace

- System of Systems
- Autonomous and collaborative
- miniature and swarming
- Cyber and social
- Human and robot collaboration
- Diverse protected links
- Decentralized systems
- Human and autonomous systems
- Information microsystems
- Leverage global technology and infrastructure

• National Defense Strategy: “Platform electronics and software must be designed for routine replacement instead of static configurations that last more than a decade ... Deliver performance at the speed of relevance.”

• New commercial technology will change society and, ultimately, the character of war. The fact that many technological developments will come from the commercial sector means that state competitors and non-state actors will also have access to them, a fact that risks eroding the conventional overmatch to which our Nation has grown accustomed.


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DoD Funding Historical Perspective

https://www.semiwiki.com/forum/content/7368-meeting-challenges-national-defense-strategy.html
US Defense R&D Trend

Beyond Borders: Semiconductors are a Uniquely Global Industry
Typical semiconductor production process spans multiple countries: 4+ Countries, 4+ States, 3+ trips around the world, 25,000 miles travelled, 100 days TPT, 12 days in transit

Top Participants in Global Trade: Semiconductor Goods

- China
- Hong Kong
- Singapore
- Taiwan
- Korea
- USA
- Malaysia
- Japan
- Germany
- Philippines

Top Participants in Global Trade: Fabrication Material Goods

- China
- USA
- Taiwan
- Japan
- Germany
- Korea
- Norway
- Mexico
- Netherlands

Top Participants in Global Trade: Assembly, Test, Packaging Goods

- China
- Germany
- France
- Korea
- USA

Recent Government HI Programs
“Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act”*

• Creates a **40-percent refundable investment tax credit (ITC)** for qualified semiconductor **equipment** (placed in service) or any qualified semiconductor manufacturing facility investment expenditures through 2024. The ITC is reduced to 30 percent in 2025, 20 percent in 2026, and phases out in 2027.

• Directs the Secretary of Commerce to create a **$10 billion federal match program that matches state and local incentives** offered to a company for the purposes of building semiconductor fabs with advanced manufacturing capabilities.

• Creates a **new NIST Semiconductor Program** to support advanced manufacturing in America. The program’s funds will also support STEM workforce development, ecosystem clustering, U.S. 5G leadership, and advanced assembly and test.

• Authorizes funding for DOD to execute research, development, workforce training, test, and evaluation for programs, projects, and activities in connection with semiconductor technologies and direct the implementation of a plan to utilize **Defense Production Act Title III** funding to establish and enhance a domestic semiconductor production capability.

*S.3933 and H.R. 7178
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Clear focus on manufacturing not just R&D
“Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act”

- Creates new R&D streams to ensure U.S. leadership in semiconductor technology and innovation is critical to American economic growth and national security:
  - $2 billion to implement the Electronics Resurgence Initiative at DARPA.
  - $3 billion to implement semiconductor basic research programs at NSF.
  - $2 billion to implement semiconductor basic research programs at the DoE.
  - $5 billion to establish an **Advanced Packaging National Manufacturing Institute** under the Department of Commerce to establish U.S. leadership in advanced microelectronic packaging and, in coordination with the private sector, to promote standards development, foster private-public partnerships, create R&D programs to advance technology, create an investment fund ($500M) to support domestic advanced microelectronic packaging ecosystem.

- Broad reach: DARPA, NSF, DoE, DoC
"Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act"

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• Broad reach: DARPA, NSF, DoE, DoC

National security is not just defense.
DARPA’S HISTORY OF INTEGRATION INNOVATION

ASEM: Application Specific Electronic Modules
E-PHI: Electronic-Photonic Heterogeneous Integration
VISA: Vertically Integrated Sensor Arrays
COSMOS: Compound Semiconductor Materials on Silicon
DAHI: Diverse Accessible Heterogeneous Integration
MOABB: Modular Optical Aperture Building Blocks
CHIPS: Common Heterogeneous Integration and IP Reuse Strategies

1990s
Sources: DARPA, Smithsonian Chips

2000s
Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)

2010s

2020s

DARPA’s DAHI Program Illuminated Path Forward

<table>
<thead>
<tr>
<th>Technology</th>
<th>MPW0</th>
<th>MPW1</th>
<th>MPW2</th>
<th>MPW3</th>
<th>Future MPWs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>IBM 65nm</td>
<td>GF 45 nm</td>
<td>GF 45 nm</td>
<td>GF 45 nm</td>
<td>GF 45 nm</td>
</tr>
<tr>
<td>InP HBT</td>
<td>TF4 (2 metals)</td>
<td>TF4 (3 metals)</td>
<td>TF4 (4 metals)</td>
<td>TF4 (4 metals)</td>
<td>TF4 (4 metals)</td>
</tr>
<tr>
<td>InP Varactor Diode</td>
<td>TF5 (3 metals)</td>
<td>TF5 (4 metals)</td>
<td>TF5 (4 metals)</td>
<td>TF5 (4 metals)</td>
<td></td>
</tr>
<tr>
<td>GaN HEMT</td>
<td>GaN20</td>
<td>GaN20</td>
<td>GaN20</td>
<td>GaN20</td>
<td>GaN20</td>
</tr>
<tr>
<td></td>
<td>T3 (HRL)</td>
<td>T3 (HRL)</td>
<td>T3 (HRL)</td>
<td>T3 (HRL)</td>
<td></td>
</tr>
<tr>
<td>GaAs HEMT</td>
<td></td>
<td></td>
<td></td>
<td>P3K6</td>
<td>P3K6</td>
</tr>
<tr>
<td>Base Substrate</td>
<td>CMOS</td>
<td>CMOS</td>
<td>CMOS</td>
<td>CMOS</td>
<td>SiC Interposer (IWPS)</td>
</tr>
</tbody>
</table>

DAHI = Diverse
Emergence of Chiplets as the Evolution of Moore’s Law

• Chiplets (smaller pieces of silicon) will enable their silicon architects to design and fabricate silicon systems more quickly
  • Shorter time to market to mix and match modular pieces linked by shorter data interconnections instead of complex SOC design
  • Lower design costs and risks

• Industry leaders like Intel and AMD are implementing chiplet strategies
  • Ramune Nagisetty, a senior principal engineer at Intel calls it “an evolution of Moore’s law.”
  • AMD’s Papermaster: “I think the whole industry is going to be moving in this direction”

• DARPA jump-started the development of “chiplet” ecosystem via the CHIPS program
  • CHIPS = Common Heterogeneous Integration and IP Reuse Strategies
  • Numerous organizations are now pursuing a range of approaches: ODSA, OCP, CHIPS Alliance, etc.

https://www.wired.com/story/keep-pace-moores-law-chipmakers-turn-chiplets/
The CHIPS Program in a Nutshell

**Design**
- **Today:** Monolithic
- **Tomorrow:** Pseudolithic + Heterogeneous

Image source: Intel

**Technology**
- A universal CHIPS interface standard
- SOTA manufacturing for DoD
- A critical set of IP chiplets

**CHIPS END STATE**
- **IP Blocks**
  - ARM
  - Cadence
  - TSMC
- **CAD tools**
  - Mentor
  - Synopsys
- **Architecture**
  - Raytheon
  - Northrop
  - Lockheed
  - Boeing
  - BAE
- **Design**
- **Verification**
- **Fabrication**
- **Pkg / Test**
- **Systems**
  - Raytheon
  - Northrop
  - Lockheed
  - Boeing
  - BAE

Source: DARPA

Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)
CHIPS Program Step #1: Agree on a Standard Interface

Intel Advanced Interface Bus (AIB) Enables Modular Design

Intel's Advanced Interface Bus (AIB) is a die-to-die PHY level standard that enables a modular approach to system design with a library of chiplet intellectual property (IP) blocks.

AIB uses a clock forwarded parallel data transfer mechanism similar to DDR DRAM interfaces. AIB is process and packaging technology agnostic—Intel's Embedded Multi-Die Interconnect Bridge (EMIB) or TSMC's CoWoS* for example.

Intel now provides the AIB interface license royalty-free to enable a broad ecosystem of chiplets, design methodologies or service providers, foundries, packaging, and system vendors.

- AIB was supported by the DARPA CHIPS program.
- AIB specification is now available to the electronics community

Figure: example of a possible heterogeneous system in package (SiP) that combines sensors, proprietary ASIC, FPGA, CPU, Memory and I/O using AIB as the chiplet interface.
CHIPS Demonstration

- Heterogeneous Integration (EMIB)
- Standard Interface (AIB)
- IP Reuse
- Leading Edge Devices
  - Intel FPGA
  - Jariet converters
  - U of Michigan ASIC
  - Intel SERDES
  - Ayar Labs optical
DARPA CHIPS Clarified Requirements for HI Manufacturing

CHIPS Manufacturing Wishlist

<table>
<thead>
<tr>
<th>Dense Interconnect</th>
<th>Target Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metallization material</td>
<td>Copper</td>
</tr>
<tr>
<td>Front end metal layers</td>
<td>4 – 6</td>
</tr>
<tr>
<td>Front end metal wiring density</td>
<td>~0.5 μm line/space</td>
</tr>
<tr>
<td>Size (full reticle)</td>
<td>26 x 33 mm²</td>
</tr>
<tr>
<td>Stitching (strongly desired)</td>
<td>6” x 6’”</td>
</tr>
<tr>
<td>TSVs</td>
<td></td>
</tr>
<tr>
<td>Depth</td>
<td>100-200 μm</td>
</tr>
<tr>
<td>Diameter</td>
<td>25 μm</td>
</tr>
<tr>
<td>Pitch</td>
<td>150 μm</td>
</tr>
<tr>
<td>Assembly</td>
<td></td>
</tr>
<tr>
<td>Back side bump pitch</td>
<td>150 μm C4</td>
</tr>
<tr>
<td>Back side RDL</td>
<td>Needed, C4 on via?</td>
</tr>
<tr>
<td>Front end bump pitch</td>
<td>55 μm Cu (10 μm roadmap)</td>
</tr>
<tr>
<td>Chiplets supported</td>
<td>7nm to 180nm</td>
</tr>
<tr>
<td>Chiplets assembled</td>
<td>2 - 100</td>
</tr>
</tbody>
</table>

Potential Engagement Path

- Commercial **on-shore** manufacturing
  - (See previous slide)
  - Si interposer w/ TSVs
  - Organic package substrates
  - Copper bumping (<55 μm)
  - C4 bumping (150 μm)
  - 2.5D assembly
  - 3D assembly
  - Flip Chip Assembly
  - SOTA automation
- Assemble all silicon sources!
- Turnkey model

Source: DARPA
“SHIP”: SOTA Heterogeneous Integrated Packaging

• Brett Hamilton, Distinguished Scientist for Trusted Microelectronics at NSWC Crane, is the Principal Technical Lead for the SHIP project.
  • SHIP gives us the ability to leverage state-of-the-art commercial processing power needed for modern weapon systems such as autonomous systems where artificial intelligence and real-time sensor data processing is critical
  • For these types of applications, SHIP significantly reduces size, weight, and power, while increasing performance.

• By having a secure SHIP design, assemble and test facility, DoD will greatly lower supply chain risk while enabling the ability to better protect the DoD’s intellectual property (IP). In such an environment, DoD can integrate more robust security mechanisms, critical in lowering cyber security risks.

https://www.navsea.navy.mil/Media/News/Article/2005099/nswc-crane-leverages-ota-to-ensure-that-the-us-government-has-access-to-secure/
SHIP Requirements

SHIP Vision of Secure HI

SHIP General Specifications

Table 3 General Capacity and Capability for the SHIP-ATC

<table>
<thead>
<tr>
<th>Category</th>
<th>IOC</th>
<th>FOC</th>
<th>Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity: Volume (annual)</td>
<td>1k+</td>
<td>10k+</td>
<td>100k</td>
</tr>
<tr>
<td>Silicon interposer</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
</tr>
<tr>
<td>Organic interposer</td>
<td>Preferred</td>
<td>Required</td>
<td>Required</td>
</tr>
<tr>
<td>Utilize SOTA COTS FPGA(^1) and programmable devices</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
</tr>
<tr>
<td>Structured ASIC</td>
<td>Preferred</td>
<td>Preferred</td>
<td>Required</td>
</tr>
<tr>
<td>Security</td>
<td>ITAR</td>
<td>ITAR</td>
<td>Classified</td>
</tr>
<tr>
<td>Number of Chips/Packag(^2)</td>
<td>4</td>
<td>8</td>
<td>12+</td>
</tr>
<tr>
<td>Supply Chain target</td>
<td>&gt;50% US</td>
<td>&gt;75% US</td>
<td>&gt;90% US</td>
</tr>
<tr>
<td>Can process singulated die</td>
<td>Required</td>
<td>Required</td>
<td>Required</td>
</tr>
<tr>
<td>Can process up to 300mm wafers</td>
<td>Preferred</td>
<td>Required</td>
<td>Required</td>
</tr>
<tr>
<td>Can process 200mm wafers</td>
<td>Preferred</td>
<td>Preferred</td>
<td>Required</td>
</tr>
</tbody>
</table>

\(^1\) Must include ability to integrate and test SOTA FPGA (<14nm), not required for RF centric applications

\(^2\) Could include, but not limited to, memory, ADC/DAC, transceivers, optical couplers, ASIC, structured ASICs, etc.

Figure 1 Notional design and prototype manufacturing flow
### Table 6 Advanced Microelectronics Assembly Specifications

<table>
<thead>
<tr>
<th>Chip on Chip</th>
<th>IOC</th>
<th>Final State</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Interposer Sizes</td>
<td>(22 x 33) mm</td>
<td>(22 x 33) mm</td>
</tr>
<tr>
<td>Top Chip Process</td>
<td>All leading processes from 180nm to 7nm</td>
<td></td>
</tr>
<tr>
<td>Chip Size Range</td>
<td>(2 x 2) mm to (21 x 32) mm</td>
<td>(1 x 1) mm to (21 x 32) mm</td>
</tr>
<tr>
<td>Chips Placed Per Interposer</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>Chip Spacing</td>
<td>100 µm</td>
<td>100 µm</td>
</tr>
<tr>
<td>Chip Bump Pitch</td>
<td>50 µm</td>
<td>30 µm</td>
</tr>
<tr>
<td>Total Connections</td>
<td>21 (estimate only)</td>
<td>&gt; 21 (estimate only)</td>
</tr>
<tr>
<td>Number of chips in 3D stack</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td>Max Organic Substrate Sizes</td>
<td>(76 x 74) mm</td>
<td>(100 x 100) mm</td>
</tr>
<tr>
<td>Substrate C4 Bump Pitch</td>
<td>25 µm</td>
<td>45 µm</td>
</tr>
<tr>
<td>Chips Placed Per Substrate</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>Chip Spacing</td>
<td>100 µm</td>
<td>100 µm</td>
</tr>
</tbody>
</table>

**Packaging Features**
- High performance polymer and solder thermal interface materials integrated with Cu heat spreaders for improved thermal performance
- Package substrates that are optimized for low loss high speed signaling
- Integration of high performance passives (capacitors, inductors and resistors) to optimize power delivery networks and high speed signaling
- Flip-chip packages at a minimum pitch of 100 µm

### Table 7 RF Centric Specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>IOC</th>
<th>Final State</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV’s Depth</td>
<td>100 µm</td>
<td>100 ~ 200µm</td>
</tr>
<tr>
<td>Diameter</td>
<td>75 µm</td>
<td>10 µm</td>
</tr>
<tr>
<td>Pitch</td>
<td>150 µm</td>
<td>50 µm</td>
</tr>
<tr>
<td>Dense Interconnect Size (full pitch)</td>
<td>(76x33) mm</td>
<td>(76x33) mm</td>
</tr>
<tr>
<td>Sizing</td>
<td>5.5x5.5”</td>
<td>5.5x5.5”</td>
</tr>
<tr>
<td>Front-end metal wiring density</td>
<td>0.5 µm line-space, 0.3 µm line-space</td>
<td></td>
</tr>
<tr>
<td>Front-end metal layers</td>
<td>4 ~ 6 (copper)</td>
<td>4 ~ 6 (copper)</td>
</tr>
<tr>
<td>RF Performance RF Output Power</td>
<td>A</td>
<td>A ~ 5dBm</td>
</tr>
<tr>
<td>RF Sensitivity</td>
<td>B</td>
<td>B ~ 5dB</td>
</tr>
<tr>
<td>Increase Detection Range</td>
<td>C</td>
<td>C ~ 30%</td>
</tr>
<tr>
<td>Array Size and Weight</td>
<td>D</td>
<td>D ~ 40%</td>
</tr>
<tr>
<td>Power</td>
<td>E</td>
<td>E ~ 30%</td>
</tr>
<tr>
<td>Assembly Back side bump pitch</td>
<td>150 µm C4</td>
<td>50 µm C4</td>
</tr>
<tr>
<td>Front end pitch</td>
<td>25 µm</td>
<td>10 µm</td>
</tr>
<tr>
<td>Component thickness</td>
<td>800 ~ 300 µm</td>
<td>800 ~ 100 µm</td>
</tr>
<tr>
<td>Chiplets supported</td>
<td>Down to 7mm</td>
<td>Down to 7mm</td>
</tr>
<tr>
<td>Chiplets assemble</td>
<td>2 ~ 100</td>
<td></td>
</tr>
</tbody>
</table>

**Packaging Features**
- High performance polymer and solder thermal interface materials integrated with Cu heat spreaders and/or heat pipes for improved thermal performance
- Package substrates that are optimized for low RF loss, low latency data rates, high speed signaling
- Integration of high-performance passives (capacitors, inductors and resistors) and matching networks to minimize prime power consumption and maximize high speed signaling
- Flip-chip packages at a minimum pitch of 150 µm

1 Values A, B, C, D & E are classified. For the purpose of this proposal list best achievable.
SHIP Application Targets

<table>
<thead>
<tr>
<th>Type</th>
<th>Attributes</th>
<th>Schematic</th>
</tr>
</thead>
</table>
| Radiation Hard – Safety Critical | On-orbit Data Processing  
Autonomous Vehicles                                              |           |
| Extremely High Performance    | Cognitive EW  
AI - Radar Detection and Classification  
Sensor fusion for tracking and targeting  
Commercial applications - AML, test & measurement, remote sensing, signal processing |           |
| Ultra Low Power               | UAV, UUV  
Remote Sensors  
Robotics  
IoT – cloud edge computing, AI enabled “Smart Operation” |           |

**Table 1** Notional heterogeneous integration configurations that are of interest to the Government.

- RF performance frequency
- Efficiency – lower parasitic
- Increased power density
- Much smaller form factor
NAVY SHIP Phase 1 Awards:
~$25M Total for SHIP Foundry Planning

• SHIP-Digital Phase 1 Awarded to:
  • Intel Federal, LLC
  • Xilinx

• SHIP-RF Phase 1 Awarded to:
  • GE Research
  • Keysight Technologies
  • Northrop Grumman Aerospace Systems
  • Qorvo

https://nstxl.org/opportunity/state-of-the-art-heterogeneous-integrated-packaging-ship-prototype-project/
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Phase 2 Winners

https://nstxl.org/opportunity/state-of-the-art-heterogeneous-integrated-packaging-ship-prototype-project/
DARPA PIPES - Photonics in the Package for Extreme Scalability

- RF Phased Arrays – Radar & 5G
  - Improved Performance and System Scalability

- Digital Sensors – Imaging
  - Scaling Pixel Array Size, Frame Rate, and Power

- Machine Learning & Simulation
  - Large-scale Modeling and Artificial Intelligence

- Computing & Data Analysis
  - Advanced Parallel Systems

**PIVES Ecosystem**

**Facilitating DoD Access:** Create an ecosystem for package-level optical signaling, enabling disruptive advances for artificial intelligence, phased arrays, sensors and processing.

**Applications Limited by Connectivity at All Length Scales**
Unique Nature of A & D Roadmap
Challenges of Aerospace and Defense Electronics Systems

The Aerospace / Defense market segment has unique challenges:

- **High Performance** – Access to leading nodes and advanced packaging technologies
- **High Reliability** – harsh environments, human safety
- **Long Product Lifecycles** – parts obsolescence & upgradability
- **Low Volumes** – high product mix, affordability
- **Need domestic supply chain**
- **How can heterogeneous integration help to achieve system performance objectives?**
Commercial vs. DoD Business Models

**Commercial**
- Product last ~2 years (until new one is out) – Revenue Based
- Systems are complex, but differing scale and complexity from DoD Systems
- Requires assured access to components for 2-3 years.

**Military**
- Product Lifecycles are Decades
- Systems are much more complex, and therefore risk managed
- Consequences are Different
- Requires Assured Access to components for Decades
- Capabilities that are not needed Commercially (RadHard)

Timelines and Complexities Are very different for DoD Modern Semiconductor Processes

Aerospace and Defense Drivers

• What are system drivers?
  • NRE costs and schedules
  • Qualification / Reliability for harsh environments
  • RF Convergence & Autonomy

• What are technical drivers?
  • Digitization over wide bandwidths and at high dynamic range to enable new capabilities
  • Common DSP HW/SW to reduce required equipment, reduce power consumption and improve sustainability / upgradability
  • Integration of RF/analog and digital functions is required

• What are the supply chain issues?
  • Access to the most advanced technology but on-shore in low volumes
  • Parts obsolescence, security, industry support
  • Possible solutions: standardized interfaces, IP-Reuse ecosystem
What are Some Metrics to Consider?

- **Performance**: data rate, latency, throughput, TFLOPs, insertion loss, isolation, dynamic range, etc.
- **Energy/Power**: pJ/bit, throughput per Joule, TFLOPS/Joule, Leakage power, etc.
- **Interfaces**: signaling protocols, error correction, interconnect lengths, ESD, etc.
- **Thermal**: Maximum junction temperature, number and location of hot spots, power densities of hot spots
- **Electrical**: Power distribution losses to components inside package, losses in conversion, peak inductive noise, harmonic noise, etc.
- **Reliability/Availability**: MTBF, radiation hardness, metric related to graceful degradation on component failures, lifetime ranges, etc.
- **Others**: PLEASE SUGGEST!
<table>
<thead>
<tr>
<th>Area</th>
<th>Metric</th>
<th>SOTA 2020</th>
<th>2025</th>
<th>2030</th>
<th>2035</th>
<th>comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Performance</td>
<td>Frequency</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thermal</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Design</td>
<td>Tools</td>
<td>Point solutions</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interfaces</td>
<td>CHIPS AIB (early traction)</td>
<td>Broad adoption + roadmap</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IP reuse</td>
<td>Chiplets (broad interest)</td>
<td>Business model adoption</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Integration</td>
<td>RF + digital</td>
<td>Separate solutions (e.g., SHIP)</td>
<td>RF + FPGA/GPU/CPU in production</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3D</td>
<td>HBM, 3D layered NAND</td>
<td>True HI in 3D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Photonics</td>
<td>R&amp;D (e.g. DARPA PIPES)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reliability</td>
<td>HI standards</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Chain</td>
<td>Components</td>
<td>International ad hoc</td>
<td>“Zero trust” solutions</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Assembly</td>
<td>US-only, lagging and/or proprietary tech</td>
<td>On-shore HVM-like interposers, FOWLP</td>
<td>Flow accommodates any volume, price, TAT</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Security</td>
<td>Trusted facilities</td>
<td>“Zero trust” (data-based; need metrics)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Obsolescence</td>
<td>Lifetime buys</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Seeking more inputs to the proposed framework, metrics, and content in the table(s)
New Edition of HI Roadmap in 2021: A&D TWG Focus

• Track developments in industry and government
• Upgrade / populate roadmap table
• Increase linkages to other HIR chapters (photonics, design, thermal,...)
• Broaden scope internationally
• Address aerospace challenges that differ from defense

<table>
<thead>
<tr>
<th>Name</th>
<th>Affiliation</th>
<th>Role</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tim Lee</td>
<td>Boeing</td>
<td>Co-chair</td>
</tr>
<tr>
<td>Jeff Demmin</td>
<td>Keysight Technologies</td>
<td>Co-chair</td>
</tr>
<tr>
<td>Tom Kazior</td>
<td>DARPA</td>
<td>Member</td>
</tr>
<tr>
<td>Dan Blass</td>
<td>Lockheed Martin</td>
<td>Member</td>
</tr>
<tr>
<td>Susan Trulli</td>
<td>Raytheon</td>
<td>Member</td>
</tr>
<tr>
<td>Kenji Miyake</td>
<td>Minimal Fab</td>
<td>Member</td>
</tr>
</tbody>
</table>
Summary
The TWG for Developing the Heterogeneous Integration Roadmap for Aerospace and Defense

• Goal: develop a **roadmap for heterogeneously integrated components for applications in Aerospace and Defense**

• **Specific goals:**
  • Identify the A-D specific challenges in the next 5, 10 and 15 year horizons
  • Identify promising solutions and technologies
  • Identify any unaddressed challenges and the types of solution / technologies needed
  • Document all of these as a chapter in the overall HIR document
    • Reports will be freely available on the IEEE EPS and SEMI websites
    • 2020 update to inaugural 2019 version complete; devising 2021 update plan
We invite you all to consider joining in the Heterogeneous Integration Roadmap Development and participate in contributing to the Aerospace and Defense Technical Working Group.

Tim Lee, tt.lee@ieee.org
Jeffrey Demmin, jeffrey.demmin@keysight.com

Thank you
Additional Content
Silicon Manufacturing Largely Offshore

Foundries concentrated in Asia

Table: Ranking of the Global Top 10 Foundries by Revenue, 1Q20 (Unit: Million USD)

<table>
<thead>
<tr>
<th>Ranking</th>
<th>Company</th>
<th>1Q20E</th>
<th>1Q19</th>
<th>YoY</th>
<th>M/S</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TSMC</td>
<td>10,200</td>
<td>7,096</td>
<td>43.7%</td>
<td>54.1%</td>
</tr>
<tr>
<td>2</td>
<td>Samsung</td>
<td>2,996</td>
<td>2,586</td>
<td>15.9%</td>
<td>15.9%</td>
</tr>
<tr>
<td>3</td>
<td>GlobalFoundries</td>
<td>1,452</td>
<td>1,256</td>
<td>15.6%</td>
<td>7.7%</td>
</tr>
<tr>
<td>4</td>
<td>UMC</td>
<td>1,397</td>
<td>1,057</td>
<td>32.2%</td>
<td>7.4%</td>
</tr>
<tr>
<td>5</td>
<td>SMIC</td>
<td>848</td>
<td>669</td>
<td>26.8%</td>
<td>4.5%</td>
</tr>
<tr>
<td>6</td>
<td>TowerJazz</td>
<td>300</td>
<td>310</td>
<td>3.3%</td>
<td>1.6%</td>
</tr>
<tr>
<td>7</td>
<td>VIS</td>
<td>258</td>
<td>224</td>
<td>14.9%</td>
<td>1.4%</td>
</tr>
<tr>
<td>8</td>
<td>PSMC</td>
<td>251</td>
<td>178</td>
<td>41.2%</td>
<td>1.3%</td>
</tr>
<tr>
<td>9</td>
<td>Hua Hong</td>
<td>200</td>
<td>221</td>
<td>-9.4%</td>
<td>1.1%</td>
</tr>
<tr>
<td>10</td>
<td>DB HiTek</td>
<td>158</td>
<td>139</td>
<td>13.8%</td>
<td>0.8%</td>
</tr>
<tr>
<td><strong>Top 10 Total</strong></td>
<td><strong>18,060</strong></td>
<td><strong>13,737</strong></td>
<td><strong>31.5%</strong></td>
<td><strong>95.7%</strong></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Samsung’s revenue includes revenues from its System LSI unit and its foundry business
2. GlobalFoundries’ revenue includes revenue generated by the chip manufacturing unit that it acquired from IBM
3. PSMC’s revenue includes its foundry revenue only
4. Hua Hong’s revenue includes figures from its publicly disclosed revenue only

Source: TrendForce compiled this table with data from the respective foundries, Mar. 2020
Nearly all foundry growth in 2019 driven by customers in China

![Pure-Play Foundry Market by Region graph]

Total 2019 Pure-Play Foundry Market Growth = -2%.

Source: IC Insights