Could diamond be 2.5D/3D integrated systems' best friend?

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***Abstract*—Thermal management is currently one of the key challenges limiting electrical performance, efficiency and long-term reliability of electronic components. Diamond has an extremely high thermal conductivity and can enable substantial reductions in junction-to-ambient thermal resistance. This review discusses possible approaches for integrating diamond and chips, highlighting the main challenges faced by the engineer and emphasizing the importance of multi-physics modeling to overcome them.**

I. Introduction

Traditional materials and cooling strategies are reaching their limits, particularly as next-generation electronic systems push toward three-dimensional integration [1], [2]. In some cases, due to the continuous miniaturization and functional integration of electronic components, the power density at chip level exceeds several hundred watts per square centimeter [3], [4]. The intense local hot spots that are generated have a negative impact on both reliability and efficiency of the electronic components. Higher operating temperatures not only decrease the device's lifetime but also result in increased resistive losses and leakage currents. In some cases the cooling requirements will add to the total energy consumption. In the case of data centers, for instance, thermal management can account for more than 30% of total electricity usage [6].

To promote the fast extraction of heat generated during the devices' operation, a material with high thermal conductivity should be integrated as close as possible to the primary hot spots. This configuration would enable a rapid reduction of the junction temperature and facilitate the transport of heat toward a heat sink, to be dissipated through natural or forced convection. However, the best thermal conductors, such as copper, are also electrical conductors, which limits their application. On the other hand, electrical insulators such as ceramics and polymers are also poor conductors of heat.

The solution to this riddle may lie in the most unexpected material: diamond. Diamond has long been used for industrial applications (such as cutting and polishing) due to its unrivaled mechanical properties. But diamond is also the best bulk thermal conductor known to man while simultaneously being an electric insulator. However, its integration into complex semiconductor assemblies is far from trivial. Key challenges include its high cost and the mismatch of its coefficient of thermal expansion (CTE) and the one of materials such as Si, GaN, or Cu. If not properly addressed at the design stage, the CTE mismatch can lead to thermo-mechanical stresses during thermal cycling or device operation, causing delamination, cracking, or degradation of the thermal interface materials (TIMs).

Multiphysics simulations–combining thermal, electrical, and mechanical domains–can play a crucial role in this context. Realistic temperature gradients and stress distributions expected during devices' operation can be obtained via finite-element or compact modeling approaches and this *a priori* knowledge may help to optimize the type and thickness of the TIM layer.

This review evaluates the use of diamond heat spreaders for the thermal management of electronic components. The key properties of diamond are initially summarized and are followed by examples of its implementation as chip-level heat spreader and power board. The main technological challenges associated with diamond integration are then reviewed, and potential strategies to overcome them are presented. Finally, the importance of multi-physics simulations to optimize cost, performance, and reliability is discussed.

II. Why diamond?

Diamond is an allotrope of carbon in which the atoms are bonded through strong sp^3 covalent bonds in a tetrahedral lattice. This bonding configuration gives diamond exceptional properties such as high hardness, wide band gap ($5.47\,\mathrm{eV}$), high breakdown field ($2 \times 10^7\,\mathrm{V/cm}$), high thermal conductivity ($2200\,\mathrm{W/m \cdot K}$), small CTE ($1.0$–$2.0\,\mathrm{ppm/K}$) and low dielectric constant (5.5) [7]. Table I shows some properties of diamond and common packaging materials.

Diamond can be artificially synthesized by chemical vapor deposition (CVD), either as 2-inch single-crystal diamond (SCD) [8] or as $4-6$-inch polycrystalline diamond (PCD) wafers. Owing to its lower crystalline quality, PCD typically exhibits a thermal conductivity in the range of $1000-1800\,\mathrm{W/m \cdot K}$. Its surface can be polished to a peak-to-valley roughness of approximately $10\,\mathrm{nm}$ and subsequently metallized. PCD wafers can also be laser-cut to the desired size and shape, and may incorporate features such as vias, microchannels, or scribed patterns [9]. Alternatively, diamond heat spreaders with specific geometries and surface finishes are commercially available from various suppliers.

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TABLE I
PROPERTIES OF SELECTED MATERIALS USED IN MICROELECTRONICS AND OPTOELECTRONICS PACKAGING [3], [9]–[12]

Material	Function	CTE (ppm/K)	Thermal Conductivity (W/m·K)
CVD diamond	Heat spreader	1.0–2.0	500–2200
Silicon (Si)	Semiconductor/substrate	2.6	150
Gallium nitride (GaN)	Semiconductor	5.6	130–210
Silicon carbide (SiC)	Semiconductor/substrate	3.08	380–450
Gallium arsenide (GaAs)	Semiconductor	5.8	55
Indium phosphide (InP)	Semiconductor	4.6	68
Sapphire (Al_2O_3)	Substrate	7.0–7.7	42
Alumina (Al_2O_3), ceramic	Chip-carrier	6.0–7.1	20–35
Aluminum nitride (AlN), ceramic	Chip-carrier/heat spreader	3.5–5.7	60–250
Beryllium oxide (BeO)	Heat spreader	5.9–9.0	254–275
Silicon carbide (SiC), CVD	Heat spreader	2.4	200/250
Copper (Cu)	Heat sink	17	400
Aluminum (Al)	Heat sink	23	218
Copper/tungsten (Cu/W)	Heat spreader/heat sink	5.7–8.3	157–190
Copper/molybdenum (Cu/Mo)	Heat spreader/heat sink	7.0–7.5	184–197

III. SOME HISTORY...

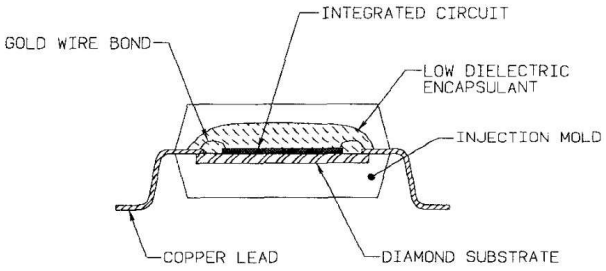
The use of diamond as an abrasive dates back to prehistoric times, with evidence suggesting applications as early as the third millennium BC [13]. Its use for thermal management of electronic devices emerged nearly five thousand years later, when Swan reported the use of diamond as a heat spreader in 1967 [14]. Swan metallized a Si wafer with avalanche diodes and type IIa natural SCD substrates with $20\,\mathrm{nm}/500\,\mathrm{nm}$ Ti/Au and $30\,\mathrm{nm}/75\,\mathrm{nm}/1000\,\mathrm{nm}$ Ti/Pt/Au, respectively, and bonded them together via gold-to-gold thermocompression at $350\,^{\circ}\mathrm{C}$. The addition of the SCD heat spreader between the diodes and a large copper stud reduced the total thermal resistance of a $0.014\,\mathrm{cm}$-diameter diode to less than half the value obtained with only the copper stud and more than doubled its input power capability.

The next notable reference appeared almost three decades later, when researchers in a study co-authored by Lockheed Martin replaced the copper lead frame of a plastic SOIC package with a PCD heat spreader [15]. The schematic view of the *NorCool*^{TM} package is represented in Fig. 1(a). GaAs MMIC dies were attached to the PCD heat spreader assembled using a metallic attach media. Since the PCD heat spreader was electrically insulating, all the copper leads could be physically connected to the PCD, providing additional paths to conduct the heat away from the package - Fig. 1(b). To compensate for the CTE mismatch between the GaAs die ($5.7\,\mathrm{ppm/K}$) and the PCD heat spreader the authors tried two different compliant metallizations (Ti/Pt/Au and Cr/Cu/Ni/Au) and evaluated several solders (AuSn, PbSnAg, and InPbAg) for optimal die attach to the PCD. Following thermal cycling tests, the authors observed that successful die attach was achieved using Pb/Sn/Ag and In-based solders and Cr/Cu/Ni/Au metallized PCD, having observed GaAs die-cracking failures for only AuSn soldered assemblies. The maximum junction temperature of a $2.5\,\mathrm{W}$ GaAs MMIC in the PCD-SOIC package was reduced by $163\,^{\circ}\mathrm{C}$ (43%) when compared to the same MMIC in a traditional plastic package, resulting in a $10^6\,\mathrm{h}$ increase in the mean-time-to-failure (MTTF). According to the authors, "*integrating a diamond substrate into a plastic package increases the thermal dissipation capability of the package to* $15\,\mathrm{W}$ *at half the cost of a typical ceramic package*". In 2002, one of the authors reported a comprehensive evaluation of the processing technology, including the filling of vias through $1\,\mathrm{mm}$-thick PCD using either screen-printed metal paste or a sputtering/electroplating approach, as well as the implementation of a $100\,\mu\mathrm{m}$-thick copper stress-relief layer to mitigate the CTE mismatch. This design successfully dissipated up to $20\,\mathrm{W}$ within a plastic package while maintaining acceptable reliability [16].

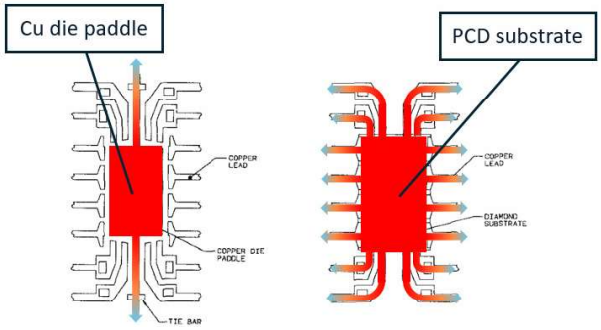
Despite the promising results reported at the beginning of the millennium, few significant studies appeared over the following decade. Since then, however, the growing importance of thermal management has led to a steady increase in related publications, as illustrated in the Fig. 2. In particular, several reference works describing the use of diamond heat spreaders for cooling silicon chips began to emerge in the 2020s.

IV. COOLING CHIPS WITH DIAMOND HEAT SPREADERS

In 2024 Zhong and his co-workers bonded PCD and silicon chips and integrated them into state-of-the-art glass interposer packages. The $12 \times 6 \times 0.2\,\mathrm{mm}^3$ silicon thermal test vehicles (TTV) with Sn3.5Ag solder bumps and $12 \times 6 \times 0.4\,\mathrm{mm}^3$ PCD substrates with $1500\,\mathrm{W/m \cdot K}$ thermal conductivity were metallized with $8\,\mathrm{nm}/200\,\mathrm{nm}/5\,\mathrm{nm}/20\,\mathrm{nm}$ Ti/Cu/Ti/Au and $8\,\mathrm{nm}/20\,\mathrm{nm}$ Ti/Au, respectively, and were pre-bonded at room temperature through gold-to-gold cold welding, followed by thermocompression bonding at $200\,^{\circ}\mathrm{C}$. The TTV/PCD pairs were chip-to-wafer flip-chip bonded to a glass interposer with underfill. The interposer wafer went through the standard process of compression molding, bumping and dicing and



(a)



(b)

Fig. 1. (a) Cross-view of the *NorCool*^{TM} package. Reprinted from [15], ©1996 IEEE. (b) Heat dissipation paths of (left) traditional and (right) *NorCool*^{TM} packages.

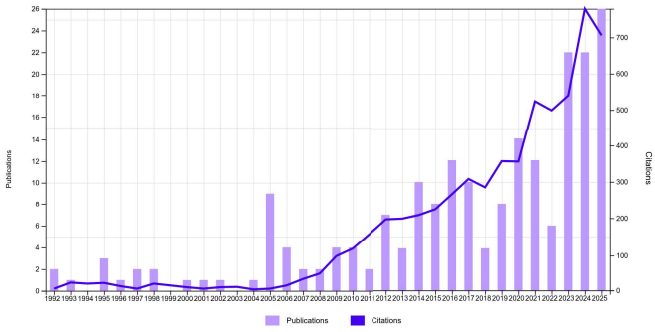
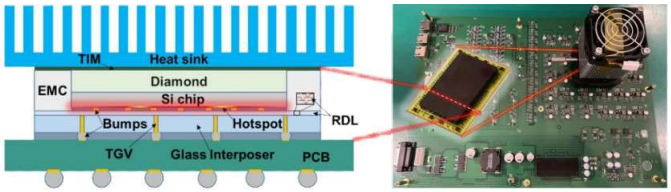


Fig. 2. Growth of publications and citations related to *"Diamond" AND "thermal management"*. Data collected from *Web of Science* on October 29, 2025, considering only articles indexed under *Applied Physics*, *Electrical & Electronic Engineering*, *Materials Science (Coatings & Films)*, *Condensed Matter Physics*, *Physical Chemistry*, *Manufacturing Engineering*, and *Nanoscience & Nanotechnology*.

an air-cooled heat-sink was mounted on the PCD using a TIM layer. The schematic structure and photograph of the resulting PCD-on-chip-on-glass interposer package are shown in Fig. 3(a) and (b), respectively. The thermal performance of the PCD-on-chip package was bench-marked against a similar package featuring a $600\,\mu$m-thick silicon TTV. For $33\,$W total power dissipation the integration of the PCD heat spreader decreased the maximum junction temperature by $24.1\,^{\circ}$C and reduced the junction-to-ambient thermal resistance by 28.5% (from 2.6 to $1.8\,^{\circ}$C/W).

The gold-to-gold thermocompression bonding process employed in the previous study produces an extremely thin metallic interface with minimal thermal interface resistance (TIR), thereby enabling the assembly to fully exploit the high



(a) (b)

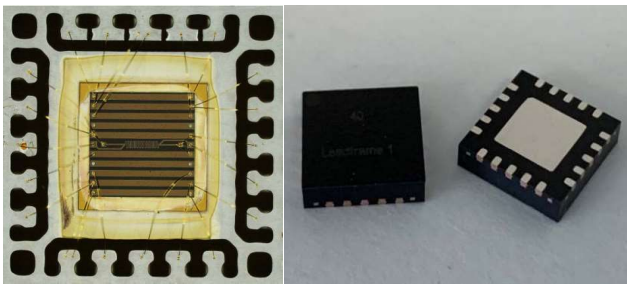
Fig. 3. (a) Schematic structure and (b) photograph of the PCD-on-chip-on-glass interposer package. Reprinted from [17], ©2024 IEEE.

thermal conductivity of the diamond heat spreader. However, this technique imposes very stringent requirements on the surface roughness of both chip and diamond, which must be below $5\,$nm. This requirement has a direct impact on the cost of the diamond heat spreader, as diamond polishing is a time-consuming–and therefore expensive–process. An alternative approach involves the use of a nano-silver paste followed by a sintering step. Although this process is significantly more tolerant to surface roughness, it introduces a considerably higher TIR when compared to gold-to-gold thermocompression bonding.

Zhao *et al.* attached $27 \times 28\,\mathrm{mm}^2$ silicon and PCD chips metallized with $20\,\mathrm{nm}/100\,\mathrm{nm}$ Cr/Au by sintering a $40\,\mu$m-thick nano-silver paste at $200\,^{\circ}$C and applying a pressure varying between 2 and $10\,$MPa. The thickness of the sintered silver layer varied between and $14-28\,\mu$m and the TIR between $428-769\,\mathrm{m}^2\cdot\mathrm{K/GW}$. The improved thermal management was evaluated by placing a $10\times10\,\mathrm{mm}^2$ film heater on the surface of a silicon or silicon/PCD pair and by placing the complete set on a cooling plate. For $2\,\mathrm{W/cm}^2$ heat flux the PCD heat spreader reduced the temperature of the hot spot by $\approx 8\,^{\circ}$C, whether the cold plate was turned on or off, and significantly improved the uniformity of the in-plane temperature. At $5\,\mathrm{W/cm}^2$ heat flux, the reduction in hot spot temperature increased up to $\approx 25\,^{\circ}$C.

In a different work, Martin *et al.* fabricated a thermally-enhanced PQFN package by including a $110\,\mu$m-thick PCD heat spreader between a $50\,\mu$m-thick TTV and the copper lead frame of the package [18]. The TTV and the PCD heat spreader were metallized with $100\,\mathrm{nm}/200\,\mathrm{nm}/600\,\mathrm{nm}$ Ti/Pt/Au, the nano-silver paste was dispensed on the PCD, the TTV was placed with a die-bonder and the nano-silver layer was pressureless sintered under nitrogen at $250\,^{\circ}$C. The TTV-on-PCD stack was further sintered to the die-pad of a lead frame following a similar procedure and the contacts of the TTV were wire bonded to the bond pads on the lead frame. The complete stack was then transfer molded with an epoxy molding compound and singulated into separate PQFN packages and the singulated packages were soldered to a test board using a SAC305 solder paste. An optical micrograph of the TTV/PCD pair sintered to the die-pad of the lead frame is shown in Fig. 4(a) and the final optimized thermally enhanced PQFN package is shown in Fig. 4(b). The thermal performance of this package was benchmarked against a similar package featuring a $400\,\mu$m-thick TTV sintered directly to the die-pad of the lead frame. To this end, an input power of $6.6\,$W,

corresponding to $\approx 10.5\,\mathrm{W/mm^2}$, was applied during $1\,\mathrm{s}$ to one resistor of the TTV. Under these conditions and for $25\,^{\circ}\mathrm{C}$ ambient temperature, the maximum junction temperature with the thermally enhanced PQFN showed a $\approx 9.6\%$ reduction and the thermal gradient was lowered as compared to the standard PQFN. The reliability of the thermally enhanced package was further assessed by thermal cycling from -55 to $150\,^{\circ}\mathrm{C}$ for two-hundred cycles. The junction temperature increased by $\approx 1.95\%$ as compared to its initial state, nevertheless it was still $\approx 5\%$ lower than the junction temperature of the standard package at 0-cycle.



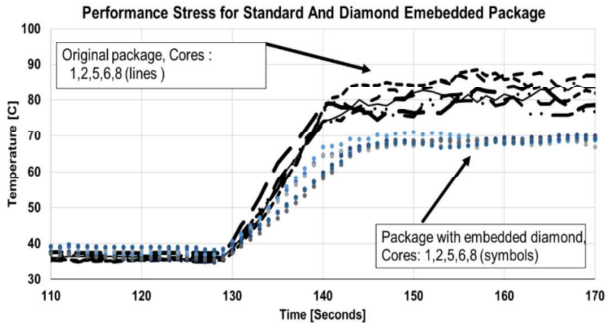
(a) (b)

Fig. 4. (a) Optical micrograph of the TTV/PCD pair sintered to the die-pad of the lead frame. Wire bonds connect the chip and package bond pads. (b) Over-molded and singulated final thermally-enhanced PQFN packages. Reprinted from [18], ©2023 IEEE.

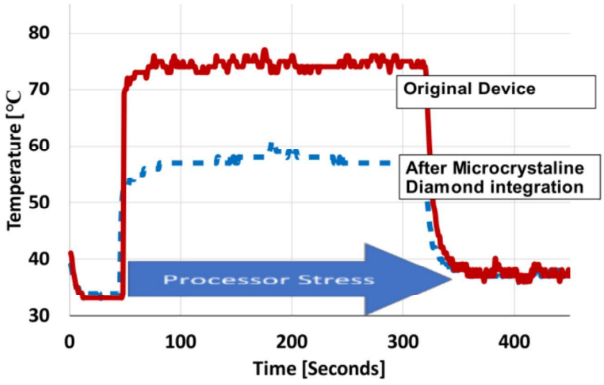
Using a gallium-based liquid-metal TIM, researchers from Phononics bonded PCD heat spreaders and advanced silicon-based CPUs. The evolution of the core temperature of original and PCD-enhanced packages of $14\,\mathrm{nm}$, 8 core and $7\,\mathrm{nm}$, 12 core CPUs can be seen in Fig. 5(a) and (b), respectively. The attachment of the PCD heat spreader allowed for a $15\,^{\circ}\mathrm{C}$ temperature reduction at full stress, a reduction of temperature spread from 4.8 to $1.2\,^{\circ}\mathrm{C}$ and a 5% increase in core operation power of the $14\,\mathrm{nm}$, 8 core CPU and a $15\,^{\circ}\mathrm{C}$ temperature reduction of the $7\,\mathrm{nm}$, 12 core CPU. According to the authors, the inclusion of the PCD heat spreader allows for significant savings in the cooling system: identical overclocking from 3 to $5.6\,\mathrm{GHz}$ of all cores could be achieved by attaching the PCD heat spreader to the CPU chip and using a standard cooling system or by using a custom 600$ $200\,\mathrm{W}$ water-based cooling system.

V. Diamond Boards

Beyond the bonding strategies described in the previous section, another possible approach is to mount the packaged power components directly onto PCD boards. Kyatam *et al.* attached Cree white XLamp XB-D LEDs to metal core printed circuit boards (MCPCBs) and to Ti/W/Au metallized PCD boards using SAC305 solder and silver paint, respectively [21]. The boards were then attached to a large copper CPU heat sink with thermal paste. The thermal resistance of the assembly decreased from $12\,\mathrm{K/W}$ with the MCPCB to $5\,\mathrm{K/W}$ with the PCD board, representing an approximate $58\,\%$ reduction. Using the values of activation energy of failure mechanisms reported in the literature, the authors estimated that replacing the MCPCB with the PCD board would increase the MTTF



(a)



(b)

Fig. 5. Core temperatures in stressed processors. (a) $14\,\mathrm{nm}$, 8 core. Reprinted from [19], ©2021 IEEE. (b) $7\,\mathrm{nm}$, 12 core. Reprinted from [20], ©2024 IEEE.

of the LEDs $2.5-8.8$ times for $350\,\mathrm{mA}$ and $4.6-33.3$ times for $700\,\mathrm{mA}$ current levels.

Ding *et al.* soldered deep-UV (DUV) LEDs on plated copper on thick film (PCTF)-metallized Al_2O_3 and PCD boards [22]. A layer of nano-silver paste was initially screen-printed and sintered on the Al_2O_3 and PCD boards. A copper layer was electroplated on the sintered silver and a final gold layer was electroless-plated on the copper. The DUV LED chips were soldered on the gold-finished pads at $280\,^{\circ}\mathrm{C}$. The emitting LED-on-PCD is shown in Fig. 6(a); Fig. 6(b) and (c) show the board connecting pads. The thermal images of the LEDs mounted on both boards obtained at different current levels are shown in Fig. 6(d). For $700\,\mathrm{mA}$ current the maximum surface temperature of the LED-on-PCD was $43\,^{\circ}\mathrm{C}$ lower than the one of the LED-on-Al_2O_3 board. The thermal resistance of the Al_2O_3 and PCD boards was measured as 2.293 and $1.064\,\mathrm{K/W}$, respectively, corresponding to an approximate $54\,\%$ reduction. The output characteristics (optical power, conversion efficiency, and wavelength) of the LED-on-PCD were also superior: at $700\,\mathrm{mA}$ current the light output power and conversion efficiency increased from 150.0 to $180.4\,\mathrm{mW}$ and from 3.39% to 3.87%, respectively, with respect to the LED-on-Al_2O_3. The red-shift of the LED-on-PCD also decreased from 1.2 to $0.4\,\mathrm{nm}$ as the current increased from 50 to $700\,\mathrm{mA}$.

VI. Challenges

Despite the clear thermal advantages of integrating diamond into power packages, several open issues still hinder its

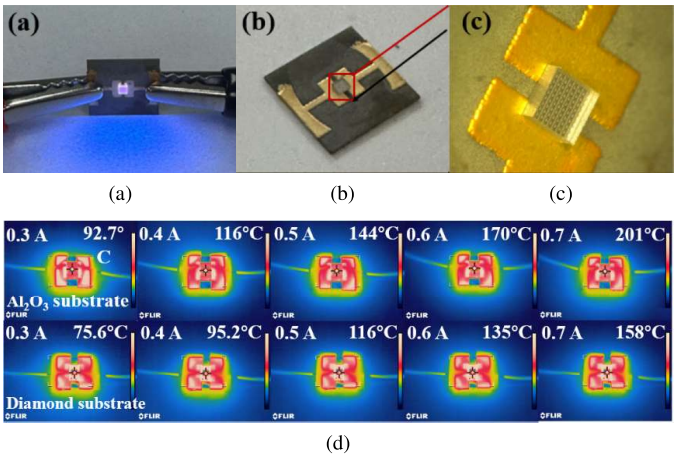


Fig. 6. (a) Emitting DUV LED mounted on the PCTF-PCD substrate. (b) Photo showing the DUV LED and the connecting pads. (c) Magnified view of the DUV LED. (d) Thermal images of DUV LEDs mounted on (top) Al_2O_3 and (bottom) PCD substrates at different current levels. Reprinted from [22], ©2024 IEEE.

widespread adoption as a heat-spreading material. The most significant challenge remains the high cost of diamond, particularly when large-area or high-thermal-conductivity grades are required. In 2016, PCD was priced at approximately $\approx\$1\,/\mathrm{mm}$ [23]. By 2025, the cost of synthetic SCD had decreased to roughly 20% of its cost in 2020 [24]; however, even with this reduction, the material remains prohibitively expensive for most commercial packaging applications.

To minimize integration costs, it is essential to avoid over-specifying the thermal conductivity, planar dimensions, or thickness of the diamond heat spreader for a given application, as each of these parameters directly increases the cost. For instance, as demonstrated in [25] and [26], the thermal improvement achieved by replacing PCD with more expensive SCD heat spreaders can be marginal, making such substitution economically unjustified in most cases.

Post-deposition processing steps, such as mechanical polishing of diamond, can also significantly raise fabrication costs. This issue can be mitigated by employing die-attachment techniques that tolerate higher surface roughness, such as soldering or sintering with nano-silver pastes, thereby reducing or eliminating the need for extensive surface finishing.

Another effective strategy to reduce material costs is the use of thin PCD films (typically thinner than $20\,\mu\mathrm{m}$) instead of conventional self-supporting diamond plates, which are usually around $300\,\mu\mathrm{m}$ thick. This approach, explored in the following section, offers a promising pathway to retain high thermal performance while significantly lowering material and integration costs.

A. Thin diamond film heat spreaders

Chen *et al.* [27] transferred a thin-GaN LED consisting of a GaN/n-GaN/multi-quantum well/p-GaN structure deposited on a sapphire substrate to a silicon substrate coated with $20\,\mu\mathrm{m}$ of diamond; the PCD film was polished and metallized with $50\,\mathrm{nm}/50\,\mathrm{nm}/2000\,\mathrm{nm}$ Cr/Pt/Au before the transfer process. 1×1 mm^2 vertical LED chips were patterned on the sapphire substrate by inductive coupling plasma (ICP) using a SiO_2 mask deposited by plasma-enhanced CVD and Ni/Au p-contacts were deposited on top of the p-GaN surface, followed by aluminum reflector and silver bonding layers. The metallized LED chips and PCD-coated silicon wafers were bonded together by gold-to-silver thermocompression, the original sapphire substrate was stripped off and a Cr/Au bilayer was deposited as n-contact on the n-GaN surface. The entire process is represented in Fig. 7.

The thermal images of the LEDs mounted on the silicon and PCD-coated silicon wafers obtained for $1\,\mathrm{A}$ current are shown in Fig. 8(a) and (b). The hot spot temperature (marked by an "H" in the figures) decreased from $118.7\,^\circ\mathrm{C}$ to $86.6\,^\circ\mathrm{C}$, respectively, which corresponds to approximate $20\,^\circ\mathrm{C}$ reduction in the LED junction temperature. The inclusion of the thin PCD layer on top of the silicon wafer also decreased the temperature gradient originating in the current crowding around the top n-contact pad from $44.9\,^\circ\mathrm{C}$ to $26.7\,^\circ\mathrm{C}$.

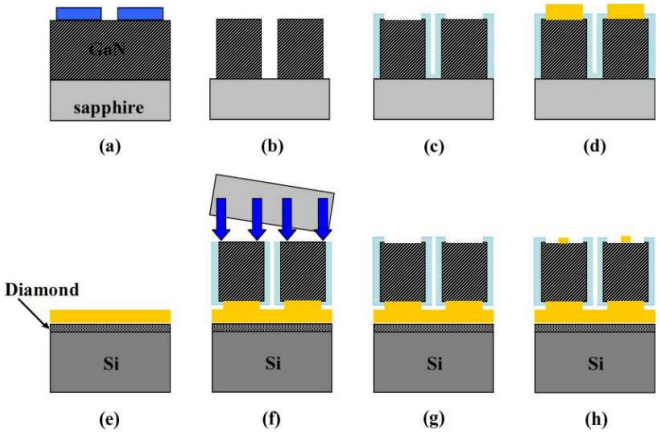


Fig. 7. Process for transferring thin-GaN LED chips to a PCD-coated Si wafer. (a) Plasma-enhanced CVD (PECVD) of SiO_2 hard mask. (b) Isolation of 1×1 mm^2 LED chips by inductive coupling plasma (ICP). (c) Sidewall passivation with SiO_2. (d) Evaporation of contact, reflector, and bonding metals. (e) Evaporation of adhesion and bonding metals on the PCD surface. (f) Gold-to-silver bonding of LED chips and PCD-coated silicon wafer and laser lift-off of sapphire substrate. (g) SiO_2 passivation. (h) Evaporation of n-contact metal. Reprinted from [27], ©2008 IEEE.

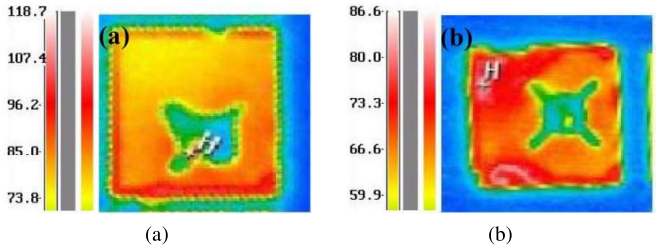
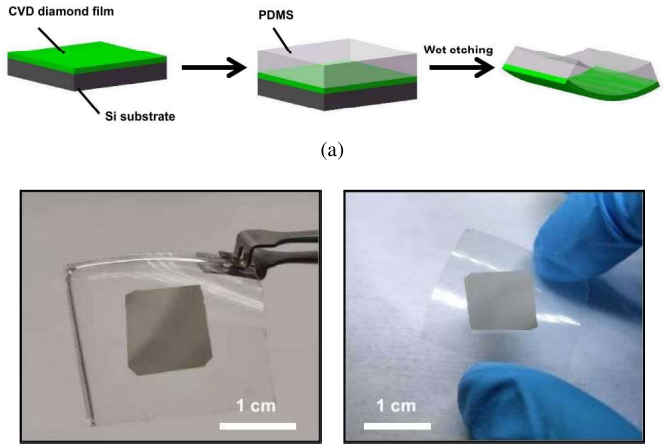


Fig. 8. Thermal images of the thin-GaN LED chips on (a) silicon and (b) PCD-coated silicon substrates. Reprinted from [27], ©2008 IEEE.

More recently, Xie *et al.* transfer-printed μ-LEDs to PCD films [28]. PDMS and PET adhesive stamps were attached to the top side of a $10\,\mu\mathrm{m}$-thick PCD film deposited on a silicon substrate and flexible PCD films were obtained following the complete chemical etching of the silicon. The schematic process flow for the fabrication of flexible PCD films is

represented in Fig. 9(a) and representative images of $\approx 10\,\mathrm{mm}^2$ $10\,\mu$m-thick PCD films on PDMS and PET substrates are shown in Fig. 9(b) and (c), respectively.



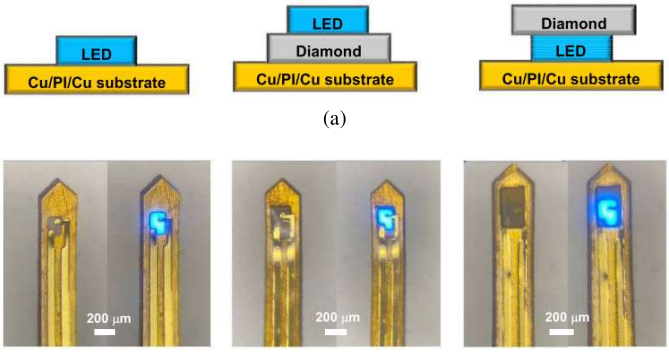
(a) (b) (c)

Fig. 9. (a) Schematic process flow for fabrication of flexible PCD films, including CVD, attachment of adhesive stamp to the top side of the PCD film and etching of Si substrate. Free-standing PCD films on (b) PDMS and (c) PET flexible substrates [28]. Reproduced from J. Phys. D: Appl. Phys., Vol. 54, Page 384004, 2021 © IOP Publishing. All rights reserved. Used with permission.

Blue μ-LEDs were transferred to copper and flexible PCD films using the procedure reported in [29]. Three different device configurations were tested (Fig. 10(a)): a μ-LED on a $18\,\mu\mathrm{m}/25\,\mu\mathrm{m}/18\,\mu\mathrm{m}$ Cu/polyimide (PI)/Cu substrate, a μ-LED-on-PCD on a similar Cu/PI/Cu substrate, and a μ-LED with PCD on top on another similar substrate. In all cases the side of the PCD exposed after etching the Si substrate was in contact with the μ-LED to minimize diffuse reflection. The corresponding images of the integrated needle-shape devices obtained after laser milling can be seen in Fig. 10(b). The external quantum efficiency (EQEs) of the bare μ-LED decreased from $\approx 12\%$ to $\approx 10\%$ for the μ-LED with PCD on top due to optical losses in the PCD film. On the other hand, the maximum EQE of the μ-LED-on-PCD on Cu/PI/Cu was $\approx 11\%$, slightly lower than the bare μ-LED due to the absorption of light transmitted from the backside of the LED by defects in the PCD.

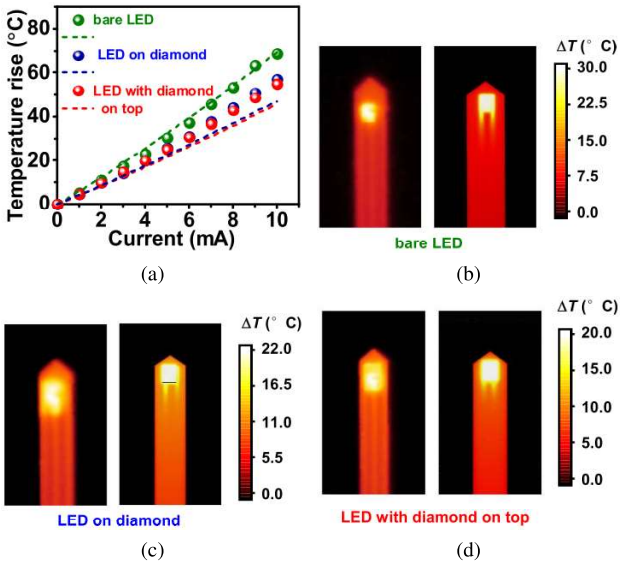
The temperature rise of the μ-LED probes was reduced by up to 20%, with the effect being most pronounced when the PCD layer was positioned between the μ-LED and the Cu/PI/Cu substrate - Fig. 11(a). The experimental and simulated surface temperature maps obtained under $5\,\mathrm{mA}$ injection current are shown in Fig. 11(d)-(b) for each of the different configurations.

As demonstrated by the studies discussed in this section, attaching a diamond film with a thickness between 10 and $20\,\mu\mathrm{m}$ to a LED die can reduce the junction temperature by approximately 10-20%. Furthermore, the ability to transfer such thin diamond films onto flexible substrates opens new opportunities for their integration into curved or convex package architectures.



(a) (b)

Fig. 10. (a) Schematic representation and (b) images of the PCD films integrated with blue μ-LEDs [28]. Reproduced from J. Phys. D: Appl. Phys., Vol. 54, Page 384004, 2021 © IOP Publishing. All rights reserved. Used with permission.



(a) (b) (c) (d)

Fig. 11. (a) Experimental (dots) and simulated (dashed lines) maximum temperature increase on the top surface of the μ-LED probes for the different configurations. (b)-(d) Experimental (left) and simulated (right) surface temperature maps of the probes under $5\,\mathrm{mA}$ injection current and different configurations: (b) Bare μ-LED, (c) μ-LED on PCD and (d) PCD on top of the μ-LED [28]. Reproduced from J. Phys. D: Appl. Phys., Vol. 54, Page 384004, 2021 © IOP Publishing. All rights reserved. Used with permission.

VII. Importance of Multi-Physics Simulations

Like was mentioned in a previous section, the successful integration of diamond heat spreaders into device packages requires balancing multiple, often competing, thermal and mechanical requirements. Multi-physics simulations have become indispensable tools that help the packaging engineer optimize these trade-offs and fully exploit the thermal benefit enabled by diamond while minimizing cost and reliability risks. The simulations enable the packaging engineer to take into account different parameters–including thickness, lateral dimensions, and thermal conductivity of the diamond plate, as well as the properties and thickness of the TIM that bonds it to the semiconductor chip or package. To reduce cost, it is essential to avoid over-specifying these parameters. For example, the cost of CVD diamond scales significantly with

its thermal conductivity, planar dimensions, and thickness. Through multi-physics-based thermal analysis, designers can determine the minimum thermal conductivity and plate dimensions required to meet system-level temperature constraints, avoiding unnecessary use of high-quality material. Since CVD diamond growth and post-processing conditions can be tailored to produce materials with different thermal properties (and cost levels), the simulations provide a valuable tool to establish the best cost-performance balance for each application [9].

Multi-physics simulations are equally valuable in evaluating thermo-mechanical reliability. The CTE mismatch between diamond and common semiconductor materials such as Si or GaN can generate substantial stresses during thermal cycling. These stresses depend not only on the CTE and Young's modulus of each material, but also on the chip size, thicknesses of the solder or TIM layers, and the operating temperature range. A multi-physics approach enable prediction of stress and strain distributions under realistic operating conditions, guiding the selection of optimal die-attach materials and layer thicknesses to prevent delamination or cracking.

A particular design trade-off exists between the TIR of the TIM layer and mechanical robustness. To withstand thermo-mechanical stresses, the TIM (e.g., solder or sintered metal) must be thick enough to absorb strain, yet increasing thickness also raises thermal resistance, which diminishes the heat-spreading efficiency of the diamond. Multi-physics simulations can quantify this trade-off and identify an optimal TIM thickness range that minimizes junction temperature while maintaining mechanical integrity. As reported in [11], thermo-mechanical modeling has shown that optimal CVD diamond heat spreader thicknesses are around $400\,\mu\mathrm{m}$, providing an effective balance between thermal performance and cost. General design guidelines suggest that the heat spreader's lateral size should be approximately $2.5\times$ the chip width for edge-mounted devices (e.g., laser diodes) and $5\times$ for centrally mounted RF transistor chips [11].

Moreover, a multi-physics analysis can guide package-level innovations to exploit the electrical insulation properties of diamond. Fabis, for instance, demonstrated that the thermal benefit of replacing the copper die paddle of a standard plastic SOIC package with a PCD plate was limited by the relatively low thermal conductivity of the die-attach material ($50\,\mathrm{W/m\cdot K}$) [16]. To fully explore the electrical insulating nature of PCD, Fabis proposed extending the copper leads over the PCD substrate to create additional heat-extraction paths, with an optimal overlap area between 0.5 and $1\,\mathrm{mm}$ to maintain manufacturability and thermal efficiency.

In summary, multi-physics simulations are crucial for determining the optimal geometry, material properties, and bonding strategy for diamond heat spreaders in high-power packages. These simulations not only ensure effective heat removal and mechanical reliability but also provide the necessary quantitative framework to justify cost-effective use of diamond in industrial packaging.

VIII. Conclusions

As shown in this review, diamond is far from being an exotic material; rather, it can offer a practical and highly effective solution for advanced thermal management. Diamond can be used both as a heat spreader and as a power board substrate to enhance heat extraction from advanced silicon chips and discrete power components. Alternatively, thin diamond films offer a lower-cost compromise that can still enable significant improvements in thermal performance.

To fully exploit the exceptional thermal conductivity of diamond while controlling cost and ensuring long-term reliability, several interdependent design parameters must be carefully taken into account–among them, the choice of bonding scheme, the type of thermal interface material, and the TIM layer thickness. These factors should be considered from the earliest stages of package and system design. Multi-physics simulations provide a powerful framework for this optimization, supporting the development of realistic, cost-effective, and thermally efficient solutions for next-generation electronic systems.

Looking ahead, and owing to its unrivaled thermal conductivity, mechanical stability, and compatibility with different semiconductor platforms, diamond is expected to play an increasingly important role in next-generation thermal management technologies. In addition, ongoing advances in CVD technology and cost reduction will accelerate diamond's transition from niche applications to mainstream adoption across power, RF, and AI computing platforms within the coming decade.

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