The 9th Annual Heterogeneous Integration Roadmap (HIR) Symposium was successfully concluded February 19-20, 2026 at the SEMI Global Headquarters, in Milpitas, California. The two day symposium was book ended by high profile keynote speakers on the morning of February 19th and the afternoon of February 20th. Two working sessions were held in between to facilitate interactions between TWG members.

Ait Manocha, President and CEO of Semiconductor Equipment and Materials International (SEMI) kicked off the morning session on Feb 19th by describing the evolution of computing and communication and the influence of AI on shaping human future. He presented a global vision of how HI influences this evolution and how SEMI shapes it positively through international collaborations. This talk was followed by a talk by Dr. Hai Ah Nam, the High Performance Computing (HPC) Technology Department Head at the National Energy Research Scientific Computing Center (NERSC) at Lawrence Berkeley National Laboratory. Dr. Ah Nam described National Energy Research Scientific Computing Center (NERSC)-10 (Doudna) which is a supercomputer designed for integrated workflows supporting the Genesis Mission. She went on to describe the upcoming NERSC-11 which is targeted to provide users with access to state-of-the-art quantum computing resources and workforce development to accelerate use of quantum computing in scientific discovery. A key aspect of her talk was a clear articulation of how HI helps system-technology co-optimization and how hardware combined with customizable software drives the future of science. Two excellent talks by Ritesh Jain (LightMatter) and Jean-Philippe Fricker (Cerebras) highlighted the value, growing importance, current progress and future in photonics interconnects and large scale system integration respectively. Both talks clearly highlighted the need for HI in enhancing and co-optimizing electrical and photonics interconnects. Prof. Dereje Agonafer (NAE Member, Professor UT Arlington) described how liquid cooling, once a boutique solution, is now a mainstream technology. He systematically walked the audience through the physical elements and modeling optimization of cooling systems and how they are projected to evolve to meet growing cooling demand. Dr. Devan Iyer (Global Electronics Association formerly IPC) closed the session by describing Advanced Packages to Board Assembly & Reliability Trends, Challenges mitigation paths. He highlighted the growing collaborations with HIR and how some of the demand trends for board technologies are included on the 2025 revision of the roadmap.

The morning session was followed by two interactive sessions where TWG members participated in small group interactions. For the first session a ‘speed dating’ format facilitated TWG member interactions. Half the TWGs (e.g. HPC, IoT) were stationed at their own table and the other half rotated. Discussions were 20 minutes in length before people rotated. The second session

centered around identifying roadmap attributes. Ravi Mahajan (Intel and HIR chair) gave an introduction to the topic and then attendees broke up into groups to discuss attribute identification. The day closed with a social hour of wine tasting and food.

On the second day the morning session consisted of several TWG member interactive sessions. First a report out the roadmap attribution discussions; each group shared their learnings. Then another round of speed dating between TWG members to facilitate cross-TWG interdependencies. In the final session small groups were formed to discuss volunteer management. Specifically, they discussed volunteer recruitment and maintaining volunteer engagement.

The final session of the Symposium had three talks. Prof. Sheng Xu (Stanford) provided a fascinating overview of wearable ultrasound sensor arrays for blood pressure monitoring, gesture recognition, temperature monitoring and showed a real application of fetal hemodynamics monitoring. This was followed by a talk by Doug Hackler (American Semiconductor) who shared technology features and application specifics for advanced flexible technologies such as Ultraflex Cu on PI and Semiconductor on Polymer (SoP). He emphasized the need to focus on manufacturability for US competitiveness. The last talk of the session was by Christine Kallmayer (Fraunhofer Group) who reported on progress of the Advanced Packaging for Electronic Components and Systems (APECS) pilot line. The APECS line is one of five pilot lines in Europe that focuses on HI using Advanced packaging for automotive, aerospace, energy and consumer applications. She showed examples of wafer and substrate level integration of 2.5D and 3D configurations developed in the APECS line and provided initial insights on planning for the 2029+ European Chips Act (EUCA II).

Thanks to the EPS Silicon Valley Chapter for supporting this event with by supporting the registration process and arranging for food and beverage service.

Presentations will only be accessible by registrants, who will be notified when they are available.



Technical Working Group Collaboration Sessions



The EPS Santa Clara Valley Chapter Members and William Chen