IEEE ELECTRONICS PACKAGING SOCIETY Newsletter

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Driving Innovation in Microsystem Packaging /// EPS.IEEE.ORG

PRESIDENT'S COLUMN

Jeff Suhling
Auburn University
Auburn, AL

Welcome to the mid-year newsletter of the IEEE Electronics Packaging Society. During 2026, the semiconductor industry has continued its remarkable trajectory of high-velocity growth, and advanced packaging and heterogeneous integration remain the critical enablers for disruptive breakthroughs in AI, autonomous systems, quantum computing, and Internet of Things (IoT). As the industry evolves, the IEEE Electronics Packaging Society (EPS) continues to expand its role as the premier global hub for packaging professionals.

Our community is thriving like never before. IEEE and IEEE EPS set new membership records at the end of 2025, surpassing 500,000 and 8,000 members, respectively. This explosive growth has been accompanied by a steady expansion of our global professional and student chapters. We now have 53 EPS Professional Chapters including recent additions in Nigeria, Chengdu China, and Nanjing China. We have also added eight new EPS Student Branch Chapters at Panimalar Engineering College-Chennai in India, University of Nottingham-Malaysia Campus, University of Malaya in Malaysia, University of Illinois, Texas Tech University, Padmasri Dr B V Raju Institute of Technology in India, University of Central Florida, and Noida Institute of Engineering and Technology in India.

We have had a great start to our financially and technically sponsored conferences in 2026 including record setting attendances at two events held in April: 1,100+ at ICEP 2026 in Hiroshima, Japan, and 350+ at EuroSimE 2026 in Warsaw, Poland. Our premier co-located conferences in the USA, the 2026 Electronic Components and Technology Conference (ECTC) and 2026 ITherm Conference, recently concluded at the end of May in Orlando, Florida. These events brought together over 3,300 global experts to share next-generation packaging research.

Our global flagship ECTC conference was dedicated to the memory of Dr. William (Bill) Chen, who passed away on March 27, 2026. Bill was a long-term and widely respected leader in the packaging community, who was a unique visionary with a strategic world view. He successfully fostered strong bridges between industry and academia, and served as an invaluable mentor to many of us throughout our careers.

Bill's legacy was honored at several events during the ECTC conference including in a heartfelt video tribute at the start of the Conference Keynote Address by Dr. Tien Wu, CEO of Advanced Semiconductor Engineering (ASE). After the video, Dr. Wu gave a wonderful keynote that recalled the history of electronics packaging technologies, and discussed how advanced packaging hardware has become the bottleneck to AI growth. He challenged us all to recognize that AI is changing everything, and that we need to prepare for the even bigger challenges and opportunities that lie ahead.

Our flagship ECTC conference shattered multiple historical benchmarks in 2026 including:

- Record Attendance: A historic 2,730 attendees and 714 Professional Development Course participants, both marking the highest turnouts in ECTC history.
- Unrivaled Technical Program: Outstanding technical exchange driven by a record 918 abstract submissions and 419 papers in the proceedings, spread across 41 technical sessions, 12 special sessions, and 16 professional development courses.
- Unprecedented Industry Support: Strong commercial backing featuring 136 exhibitors and record sponsorship support with 52 sponsorships from 50 companies.
- Community Engagement: Vibrant, multi-faceted participation that included interactive presentations, startup activities, numerous networking events, and deep student engagement through local college participation and dedicated student competitions.

(continued on page 34)

NEWSLETTER SUBMISSION DEADLINES

1 December 2026 for Winter issue 2027

15 June 2027 for Summer issue 2027

Submit all material to d.manning@ieee.org

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2027 Term End: Regions 1-6, 7, 9—Benson Chan, Region 10—Sarah Eunkyung Kim, Yoichi Taira, Shinya Takyu, Yik Yee Tan, Yu-Po Wang

2028 Term End: Regions 1-6,7, 9—Pradeep Lall, Ravi Mahajan, Region 8—Przemyslaw Gromala, Grace O'Malley, Jean-Charles Souriau, Region 10—Varun Kumar Kakar

Publications

Transactions on Components, Packaging and Manufacturing Technology

Managing Editor:
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VP Education: Eric Perfecto, eperfecto@gmail.com

Lecturers: Ramachandra Achar, Ph.D., Mudasir Ahmad, Kemal Aygün, Ph.D., Muhannad Bakir, Ph.D., Wendem Beyene, Ph.D., Chris Bower, Ph.D., Tanja Braun, Ph.D., Ken Butler, Ph.D., Francesco Carobolante, Kuan Yew Cheong, Ph.D., Xuejun Fan, Ph.D., Mukta Farooq, Ph.D., Przemyslaw Gromala, Ph.D., Deepak Gopal, Ph.D., Madhu Iyengar, Ph.D., Subu Iyer, Ph.D., Beth Keser, Ph.D., Pradeep Lall, Ph.D., John H. Lau, Ph.D., Ravi Mahajan, Ph.D., James E. Morris, Ph.D., Rajen Murugan, Ph.D., Katherine "Kitty" Pearsall Ph.D., Eric D. Perfecto, Mark Poliks, Ph.D., Markondeya (Raj) Pulugurtha, Ph.D., Gamal Refai-Ahmed, Ph.D., Katsuyuki Sakuma, Jose Schutt-Aine, Ph.D., John Shalf, Dongkai Shangguan, Ph.D., Rohit Sharma, Ph.D., Ephraim Suhir, Ph.D., Andrew Tay Ph.D., Manos Tentzeris, Ph.D., Rao Tummala, Ph.D., E. Jan Vardaman, Paul Wesling.

Chapters and Student Branch Chapters

Refer to https://eps.ieee.org/chapters/ for EP Society Chapters and Student Branch Chapters list.

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A Tribute to Dr. William (Bill) Chen — Architect of a Connected World

Bill Chen passed peacefully, surrounded by his family, on March 27, 2026.

There are engineers who solve problems. And then there are visionaries who reshape the entire industries before the rest of the world even knows the problems exist. Dr. William (Bill) Chen belongs to the rarest of that second category.

Bill Chen is a visionary strategist, lead mentor for innovation, and hands-on engineer — a combination that defines not just a career, but a calling. Over more than six decades in microelectronics, he has shown many of us what it looks like when brilliance is matched equally by generosity of spirit.

Bill received his PhD from the Theoretical and Applied Mechanics department at Cornell University. His journey began at IBM Corporation in Endicott, New York in 1963, at a time when the semiconductor industry was still finding its footing. Rather than merely follow the path, Bill helped *build* it. At IBM, he pioneered predictive verified modeling (Thermal Stresses in Bonded Joints" and "Advances in Electronic Packaging" — earning the IBM Division President Award for his leadership and innovation, and election to the IBM Academy of Technology. These were not incremental contributions. They were the foundational tools that future generations of engineers would inherit and build upon.

But Bill Chen was never a man content to rest on past achievements. His leadership led to the industrialization of game-changing packaging technologies — copper wire bonds replacing gold interconnects, saving the industry hundreds of millions of dollars a year; 2.5D packaging that set the standard for high-performance logic and memory; and a strategic vision for fan-out wafer-level packaging critical for meeting future demand for smaller, thinner, and faster electronic systems. Each of these breakthroughs represents not just technical triumph, but the courage to imagine what didn't yet exist.

His strategy portfolio — spanning SiP, copper wire-bond, 2.5D packaging, and fan-out wafer-level packaging, heterogeneous integration — brought game-changing technologies to high volume production, addressing new demands for IoT, cloud computing, autonomous automotive, AI, and smart mobility. In other words, the devices billions of people rely on everyday carry, invisibly within them, the fingerprints of Bill Chen.

What makes Bill Chen truly extraordinary, however, is that his vision was never limited to the lab. He has served as past President of the IEEE Electronics Packaging Society, stands as a Life Fellow of IEEE and a Fellow of ASME — honors that reflect not just technical mastery, but years of leadership given freely in service of the broader community. He chaired the Heterogeneous Integration Roadmap, helping the entire industry see around the next corner together.

The family of William Chen has worked with the IEEE Foundation to establish the IEEE William Chen Memorial Fund which supports the IEEE WIE Francis B. Hugle Scholarship (a program Bill helped to fund during life).

Donations can be made to the IEEE William Chen Memorial Fund via this page.

Ravi Mahajan, Intel Corp.
Past VP Publications IEEE EPS, Past Managing Editor-in-Chief of the IEEE Transactions of the CPMT

Special Tributes from Colleagues

"Bill was fantastic at recognizing talent and ability in younger engineers and with his low-keyed approach, he will ask/convince you to help with a project, and you will say YES. Over his many years working in the electronics packaging industry, he has helped cultivate many of the engineers with the most recent push to get volunteers working on all the chapters of the Heterogeneous Integration Roadmap."

Dr. Benson Chan, Binghamton University
Associate Director, IMAPS Fellow, IEEE Senior Member

"After a stellar career in Industry, Bill in his later years gave back immensely to our packaging community. I remember vividly the many conversations we had at IEDM in 2015 where he brought up the idea of the HIR to plug the hole left behind when the ITRS disbanded and how we could organize it. His enthusiasm and power of persuasion were infectious and inspiring. Bill has made a lasting impact. He reorganized our community with purpose!"

Subramanian S. Iyer,
Distinguished Professor and Charles P. Reams Endowed Chair,
ECE and MSE Departments
Director, UCLA CHIPS

"Talking to Bill Chen about his career in microelectronics is like jumping into the pages of a history book — and yet he has never looked backward. His eyes have always been fixed on what comes next, and more importantly, on who will carry it forward. He has dedicated himself to mentorship, knowing that the greatest technology he could ever architect is a new generation of engineers inspired to do what he did: show up, dig deep, and dare to innovate.

In 2022, IMAPS bestowed upon him the Daniel C. Hughes, Jr. Memorial Award — its highest, most prestigious annual technical honor — a recognition that echoed what his colleagues had known for decades: that Bill Chen's contributions to microelectronics are not measured in papers or patents alone, but in the culture of excellence and collaboration he leaves behind wherever he goes.

The world is smaller, faster, smarter, and more connected because of him. That is a legacy that will endure long after the last chip is packaged.

I'm deeply grateful for Bill's guidance at ASE and in the industry. His encouragement for my service in ECTC and EPS HIR greatly shaped my career in meaningful ways. I hope to pay it forward by supporting others to reach their full potential".

Ou Li, UTAC

"Bill was blessed with an incredibly disarming and generous demeanour that put every room at ease. Yet beneath that warmth was a remarkable depth and breadth of knowledge, which brought insight to every conversation he joined."

Amr S Helmy, Univ of Toronto

"I feel deeply fortunate to have known him and learned from him since my Ph.D. days at Cornell. Beyond his extraordinary professional achievements, I will always remember his kindness, generosity, and broad vision—he mentored me and many others, inspiring us to think bigger, push the boundaries, and contribute with purpose. His legacy will live on in the many lives he touched"

Jie Xue, Cisco (retired)

"His decision to entrust the IEMT Conference to EPS Malaysia once again reflected his remarkable foresight and deep commitment to nurturing a vibrant new chapter in IEEE Region 10".

Shaw Fong Wong, Intel Malaysia

"I first met Bill Chen in the late 1990s when, as IMRE director, he championed our electronic packaging program at HKUST and brought me into organizing the 1998 EMAP Symposium, launching a 30-year collaboration. From shifting IEMT to Malaysia and founding the HIR Symposium with the Silicon Valley EPS Chapter, to co-chairing the HI Roadmap's Advanced Manufacturing chapter, Bill's mentorship, friendship, and tireless dedication profoundly shaped both my career and our field".

Dr. Annette Teng, AIM Photonics

"In deep memory of Dr. Bill Chen who guided me into the Microelectronic Packaging field when I worked in Singapore' IMRE nearly 30 years ago. Bill is a visionary leader, a great mentor, and is forever remembered with my deep gratitude'.

Dr. Li Ming, ASMPT

"Bill was incredibly kind, thoughtful, and generous with his time and words. He was also a master listener. When a room is filled with different opinions, everyone would wait for Bill to speak. And when he spoke, everyone listened because he was the heart and soul of our technical community and our greatest compass".

Dr. Muhannad Bakir, Georgia Tech

"I was impressed with Bill's dedication and enthusiasm for the field the moment I met him. What impressed me more, though, was his kindness, humility, sense of humor and ability to bring people together. I will miss our daily talks and traveling together. His passing leaves a tremendous void, but his legacy will live on forever".

Denise A. Manning, IEEE EPS, Executive Director

"Bill was the humblest, kindest and brightest person I have met in my professional career. His leadership, wisdom and trust in people have helped advance packaging by leaps and bounds. I am truly lucky to have known him".

Swaminathan Madhavan,
Dept. Head Electrical Engg.
William E. Leonhard Endowed Chair
Director, CHIMES (an SRC JUMP 2.0 Center)
Penn State Univ.
Emeritus Professor, ECE Georgia Tech

"Bill interviewed me at Cornell prior to my being hired at IBM Endicott. As a former Cornell T&AM grad, Bill was naturally my technical mentor over the next three years at IBM, guiding me through the challenges of modeling packaging fabrication process - questioning my assumptions, but always positive and constructive. Bill remained a mentor after I left IBM to join academia, to

the end continuing to email information that he thought I should read. I admired Bill's technical thoroughness (his 1979 paper on modeling bonded joints is a true classic!), incredibly positive spirit, legendary energy and, most important of all, his ceaseless desire to learn (and guide). My last memory of him was sitting next to him in the first row of chairs listening to speakers at Binghamton University Electronics Packaging Symposium in 2024. I, like many of my colleagues at IBM, was fortunate to have been mentored by Bill; I will miss him dearly!"

Ganesh Subbarayan, Purdue University

"Bill Chen. His name, known far and wide across the world, will forever be synonymous with hard work, sharp intellect, fierce loyalty, legendary charm, and an innate thoughtfulness that always brought comfort and joy. What immense gratitude I feel to have worked alongside Bill for 22+ years, forever mentoring, guiding, and inspiring. The loss is immeasurable, for me, for us, for his community, but mostly for his beloved family that had his huge heart. Bill is already missed more than words can say. As Scottish Hebrideans often quote on such sad occasions, "Gus am bris an latha."

Patricia MacLeod, ASE
Sr. Director, Corporate Communications & Industry Partnerships

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"I met Dr. Bill Chen a few days after I started my career at IBM Endicott. He wasn't my manager nor a member of my department but he was involved in the core of what IBM was working on in packaging. He took the initiative to meet all the new hires, understand what we could do and involve us in the most pressing technical issues. I learned all about IBM and its technology from Bill. His patience and gentle persistence set an example of how best to work with other people. He encouraged me to become a technical manager, he invited me to give lectures on polymer materials at the electronics packaging course IBM co-taught at Cornell and to get involved in the ECTC and IEEE EPS. Since those early days he has had a constant presence in my career and his legacy lives on in what I do."

Mark Poliks
Binghamton University

"No one can do what you did, Bill." Listening to Tien Wu's keynote at ECTC on May 27, 2026, it felt as if I were having a live conversation with you through his reflections on your life and mentorship.

It has been my honor to step in and help complete the work you started on the 2026 IEEE ECTC HIR sessions. Since your passing on March 27, 2026, we faced significant challenges, but we refused to give up—driven by our desire to honor your legacy as the founder of the Heterogeneous Integration Roadmap. This was all for you, my dear friend.

Thank you for your invaluable guidance. Your vision shaped not only my journey in the packaging industry but also the professional I am today. I am deeply grateful for your support.

Rockwell Hsu, Cisco

2026 IEEE Rao R. Tummala Electronics Packaging Award

Shi-Wei Ricky Lee
HKUST, Hong Kong

Sponsored by IEEE Electronics Packaging Society

"For contributions through research on lead-free soldering reliability and promoting the globalization of electronics packaging."

During his distinguished career, Ricky Lee spent more than a decade advancing the understanding of lead-free solder joint failures in portable consumer devices. His interest in this area was motivated by the fact that more and more portable consumer electronics appeared susceptible to mechanical shocks. He and his team conducted comprehensive studies to investigate both macroscopic and microscopic failure mechanisms. Their groundbreaking research defined key solder joint failure modes and established critical correlations between high-speed shear/pull tests and real-world mechanical drops. Importantly, Lee's work shaped JEDEC test standards that are now widely adopted across the microelectronics industry, leaving a lasting impact on electronic packaging engineers worldwide.

An IEEE Fellow, Lee is Chair Professor of Smart Manufacturing Thrust and Vice-President (Research), The Hong Kong University of Science and Technology, Guangzhou campus.

2026 IEEE Electronics Packaging Society Award Recipients

Shaw Fong Wong
Intel, Malaysia

2026 IEEE EPS Electronics Manufacturing Technology Award
For over 25 years of full spectrum semiconductor leadership – from silicon sorting and 3D packaging to system solutions – driving yield, reliability, and high-volume production for generations of revolutionary products.

Bongtae Han
University of Maryland, USA

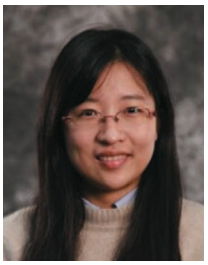
2026 IEEE EPS Outstanding Sustained Technical Contribution Award
For contributions to electronic packaging design for reliability and workforce development, especially measurement of advanced package behavior and material properties.

Tiwei Wei
UCLA, USA

2026 IEEE EPS Exceptional Technical Achievement Award
For outstanding contributions to thermal management in 2.5D and 3D system integration, including advancements in multi-physics and multi-scale modeling, electronic cooling, and thermal packaging materials.

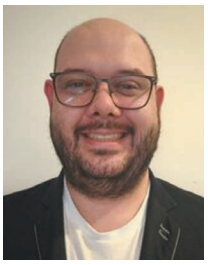
Ravi Mahajan
Intel, USA

2026 IEEE EPS William Chen Distinguished Service Award
For sustained excellence in leadership and service to the IEEE community helping promote global industry-academia collaboration in Heterogenous Integration.



Fan Wu
Hewlett Packard, USA

2026 IEEE EPS Outstanding Young Engineer Award
For groundbreaking innovations in the development of fine-pitch interconnect, molded integrated circuits, and adhesive dispense technologies that enable impactful contributions and industry advancements to MEMS packaging, microfluidic devices and beyond.



Waldir Ventura Filho
Federal Fluminense University, Brazil

2026 IEEE EPS Regional Contributions Award – Regions 1-7 & 9 (Americas)
For pioneering live organizational unit creation, achieving record-breaking EPS growth in Region 9, and demonstrating exceptional leadership in technical sustainability and global member engagement.

Karlheinz Bock
TU Dresden, Germany

2026 IEEE EPS Regional Contributions Award – Region 8 (Europe, Middle East and Africa)
For dedication to teaching and research, extraordinary contributions to international networking within the packaging industry, and encouraging and supporting the engagement of future generations of electronics engineers and others.

Rohit Sharma
Indian Institute of Technology Ropar, India

2026 IEEE EPS Regional Contributions Award – Region 10 (Asia & Pacific)
For leadership in advancing microelectronics education, pioneering high-speed interconnect research, and exceptional service in promoting the activities of the IEEE Electronics Packaging Society in India.

Ram Krishna
University of Illinois Urbana-Champaign, USA

2026 IEEE EPS PhD Fellowship
For a novel signal integrity modeling methodology that bridges fabrication variations and operating conditions to enable rapid yield prediction for die-to-die interconnects in advanced packaging systems.

EPS Santa Clara Valley Chapter

2026 IEEE EPS Chapter of the Year Award
For outstanding leadership in fostering a strong connection to and development of its members, volunteers and community.

EPS Major Awards Nomination Period Starts on September 15

The EPS Major Award nominations require online submission. The nomination period to input all the required documents runs from September 15 to January 21. The Electronics Packaging Society offers the following awards for the purpose of recognizing outstanding service and contributions to furthering the professional purposes of IEEE and EP Society.

Outstanding Sustained Technical Contributions Award: To recognize outstanding sustained and continuing contributions to the technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Technical contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. One major contribution will not qualify. Must be documented by open literature publications such as papers, patents, books and reports (available to the public).

Eligibility: Recipient must have been a member of IEEE and EPS for at least the past three years and renewed for the year of the Award.

A minimum of 3 endorsements is requested. (Endorsers do not need to be current EPS members).

Electronics Manufacturing Technology Award: To recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the EP Society.

Prize: $3,000 and Certificate

Basis for Judging: Contributions may include technical development of, or management (directing) of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes, etc. Contributions must be sustained and continuing over a period of at least 15 and preferably 20 years. Work in the management of EPS Conferences or its BoG may be contributory, but it is not a requirement for the award.

Eligibility: Membership in IEEE or the EPS is not required.

A minimum of 3 endorsements is requested. (Endorsers do not need to be current EPS members)

William Chen Distinguished Service Award: To recognize and honor outstanding service and leadership to the Electronics Packaging Society and its sponsored activities.

Prize: $5,000 and Certificate

Basis for Judging: Recipient is required to have made outstanding contributions to expanding the Society's impact in the electronic packaging field and profession through service and leadership within the EPS organization, including activities at the Chapter, Regional or BoG level or through the society's primary conferences and workshops. Examples would include serving as a conference chair, society officer, regional director, etc.

Eligibility: At the time of nomination, the nominee must have been continuously a member for the previous ten (10) years of IEEE and EPS with respect to the year of presentation of the award, and have already renewed the membership for the year of presentation of the award.

A minimum of 3 endorsements is requested. (Endorsers do not need to be current EPS members)

Exceptional Technical Achievement Award: To recognize an individual, or group of individuals (no more than three), for exceptional technical achievement in the fields encompassed by the EP Society.

Prize: $2,500 and a Certificate.

Basis for Judging: Technical contributions of the nominee(s) must be such that they are considered to be exceptional, not achieved

by most members. A single major contribution will qualify for this award. The contribution could be a significant invention, introduction of a significantly new and important technology or product (in which case, the nominee may be a team leader), or significant work that advances the state-of-the-art in EPS's field of interest. The technical contributions must be documented by open literature publications such as papers, patents, books, and reports (available to the public). Technical recognition and awards from the organization employing the individual as well as awards from other IEEE and non-IEEE technical societies may also be contributory.

Eligibility: Recipient(s) must have been a member of IEEE and EPS for at least the past three years and renewed for the year of the Award.

A minimum of 3 endorsements is requested. (Endorsers do not need to be current EPS members)

Outstanding Young Engineer Award: To recognize outstanding contributions to the fields encompassed by the EP Society through invention, technical development, publications, or new product implementation.

Prize: $1,500 and Certificate

Basis for Judging: Technical contributions through patent invention, contributions to technology or product development within the EPS Field of Interest. May encompass management (directing) of significant new product introduction or implementation of major new electronic manufacturing processes; significantly increasing yield and/or reliability of established manufacturing processes. Contributions to the Society, through the BoG, Conferences, Chapters, etc., will also be considered. Proof of contributions may consist of open literature publications (preferred) such as papers, patents, books, and reports (available to the public). At least three (3) letters from peers and management at the nominee's place of employment attesting to the accomplishment(s) can be accepted in lieu of publications.

Eligibility: Recipient must be a current member of IEEE and EPS, and have been a member of IEEE and EPS for at least the past three years and renewed for the year of the Award. Recipient must be less than 35 years of age on 31 December of the year before the award year.

A minimum of 2 endorsements is requested (Endorsers do not need to be current EPS members)

Regional Contributions Award: To recognize significant and outstanding leadership and contributions to the growth and impact of EPS programs and activities at the Region level. Maximum of one award annually from each Region/Groups of Regions (3 awards): Regions 1-7 & 9; Region 8; and Region 10.

Basis for Judging: Demonstrated service and leadership in areas that may include but are not limited to Chapter activities, Conference/Workshop activities, Membership Development, Student Programs and Technical Activities. The respective EPS Regional Advisory Committees will receive nominations, evaluate candidates, select a candidate(s), and present candidate(s) to EPS Awards Committee for review and approval.

Eligibility: Recipient has been a member of IEEE and EPS for at least the past three years and renewed for the year of the Award. Self-nominations will not be accepted.

Guidelines for Nominators:

- A recipient of any EPS Major Award will be eligible for nomination for another EPS Major Award *after two award cycles have passed*. (i.e., Recipient of XX Award in 2024 becomes eligible for nomination for YY Award in 2027). For lists of past awardees, see http://eps.ieee.org/awards.html
- Past recipients of an award are not eligible to receive that same award. For lists of past awardees, see http://eps.ieee.org/awards.html
- An individual may submit only one nomination per award but may submit nominations for more than one award.
- An individual may submit only one endorsement per award but may submit endorsement for more than one award.
- It is the responsibility of the nominator to ensure quality documentation to assist the Awards Committee in evaluating the candidate.
- Outstanding Sustained Technical Contribution Award is designed for the "practitioner", while the Electronics Manufacturing Technology Award intended for "Corporate Leadership".
- Complimentary material, such as candidate's picture, CV, list of publications and/or patents should be submitted separate from the award nomination.
- Self-nominations **will not** be considered.

EPS PhD Fellowship:

To promote, recognize, and support PhD level study and research within the Electronics Packaging Society's field of interest.

Prize: A certificate and a single annual award of US$5,000, applicable towards the student's research.

Basis for Judging: Demonstration of his/her significant ability to perform independent research in the fields of electronic packaging and a proven history of academic excellence, as documented in:

- Nomination by an IEEE EPS Member. Only one nomination per member per year.
- Two-page (maximum) statement by the student describing his or her education and
- Research interests, accomplishments, and impact on the electronics package industry.
- Proof of contributions to the community may consist of open literature publications (preferred) such as papers, patents, books, and conference presentations and reports (available to the public).
- At least one letter of recommendation from someone familiar with the student's work
- Student resume

Eligibility: Candidate must be an IEEE EPS member, at the time of nomination, and be pursuing a doctorate degree within the EPS field of interest on a full-time basis from an accredited graduate school or institution. The candidate must have studied with her/his advisor for at least 1 year, at the time of nomination, to be eligible. A Student who received a Fellowship award from another IEEE Society, within the same year, or is a previous EPS Fellowship winner is ineligible.

EPS Chapter of the Year Award

Objective

The objective of this award is to encourage Chapters to serve their local members by supporting:

- Development and execution of Chapter annual plan.
- Service its members in the technical area through organizing local Chapter activities, such as technical meetings, education, tutorials, industry visits, community service projects etc.

- Actions that keep Chapter volunteers active and maintain continuity of Chapter volunteers.
- Actions that help members with advancement to higher membership grades (senior and fellow).
- Actions that support EPS membership recruitment.
- Actions that support EPS awards solicitation.
- Establish means to recognize outstanding activities and to spread well-working practices.

Nominations
Nominations are solicited from the local EPS Chapter Chairs as self-nominations and according to the annual EPS Major Awards timeline. Winning chapter receives:
- Certificates for all registered Officers
- Monetary award of US$ 2,000 towards chapter leadership activities (this applies to all chapters, including joint chapters)

The award shall be presented annually in conjunction with local EPS Flagship conference, ECTC for Regions 1 – 7 and 9, ESTC for Region 8, and EPTC for Region 10 (or any other event considered most suitable for the winning chapter), to representative(s) of the winning Chapter.

More details can be found here

All Award nominations must be online. Nominations questions can be sent to the Society Awards Program director:

Patrick McCluskey
mcclupa@umd.edu

Winners will be notified by April 2027, and the awards will be presented at the 77th Electronic Components and Technology Conference (ECTC) in Denver, CO USA

ECTC 2026 Travel Award Winners

Congratulations to the winners of the 2026 ECTC travel award. The award is intended to assist students to attend ECTC.

Salma Abdelzaher, University of Illinois, USA
Waleed Alshaibani, Binghamton University, USA
Kevin Antony Jesu Durai, University of North Texas, USA
Shuchao Bao, Xiamen University, China
Fatin Battal, Radboud University, Netherlands
Xinyue Chang, KU Leuven, Belgium
Vineeth Harish, University of California, Los Angeles, USA
Chi Hsueh, National Yang Ming Chiao Tung, Taiwan
Hung-Chih Huang, University of Tokyo, Japan
Kyeong-Bin Kim, Sungkyunkwan University, South Korea
Sang-Hoon Kim, Sungkyunkwan University, South Korea
You-Gwon Kim, Hanyang University, South Korea
Hayato Kitagawa, Yokohama National University, Japan
Himanandhan Reddy Kottur, University of Florida, USA
Ram Krishna, University of Illinois, USA
Bonghak Lee, Seoul National University, South Korea
Jaewon Lee, Georgia Institute of Technology, USA
Jiyun Lee, Seoul National University of Science, and Technology, South Korea
Wei Choong Lee, National Taiwan University, Taiwan
Young-Joon Lee, Seoul National University, South Korea
Jie Li, Purdue University, USA
Jinzhu Li, Fudan University, China
Jialong Liang, Delft University of Technology, Netherlands
Weichang Lin, Rensselaer Polytechnic Institute, USA
Yujui Lin, Stanford University, USA
Chang Liu, Tohoku University, Japan
Jun-Nan Liu, National Tsing Hua University, Taiwan
Haran Manoharan, Missouri University of Science and Technology, USA
Mahbub Alam Maruf, Auburn University, USA
Golam Rakib Mazumder, Auburn University, USA
Md Rayid Hasan Mojumder, Pennsylvania State University, USA
Kirthika Nahalingam, Texas A&M University, USA
Nimish Nazirkar, Rensselaer Polytechnic Institute, USA
Abdelrahman Omar, University of North Carolina, USA
Yusuf Ozdemir, KU Leuven, Belgium
Junho Park, Korea Advanced Institute of Science and Technology, South Korea
Ramin Rahimzadeh Khorasani, Pennsylvania State University, USA
Sajith Rathnayaka, Florida International University, USA
Genaro Soto Valle Angulo, Georgia Institute of Technology, USA
Lin-Chun Su, National Yang Ming Chiao Tung, University, Taiwan
Mumtahina Islam Sukanya, University of Maryland, USA
Keyu Wang, Purdue University, USA
Shaojian Xie, Fudan University, China
Pradyot Yadav, Massachusetts Institute of Technology, USA
Yunchun Yang, University of California, Los Angeles, USA
Cheng-Yan Yang, National Taiwan University, Taiwan
Dalei Yang, Binghamton University, USA
Dong-Hoon Yoo, Hanyang University, South Korea
Jiwon Yoon, Korea Advanced Institute of Science and Technology, South Korea
Jingqi Zhang, Tohoku University, Japan

EPS/ECTC Volunteer Awards 2026

The EPS/ECTC Volunteer Award is given to those individuals who contribute to the success of the ECTC by volunteering in one of the conference committees, year after year. Here are the 2026 EPS/ECTC Volunteer Award winners:

10-Year Volunteers

Alvin Lee
Benson Chan
Bora Baloglu
David Danovitch
Erkan Oterkus
Hiren Thacker
Hongbin Yu
Jaemin Shin
Jiantao Zheng
Qianwen Chen
Steffen Kroehnert
Wei Wang

25-Year Volunteer

Dongji Xie

Congratulations to Recently Elevated IEEE EPS Senior Members

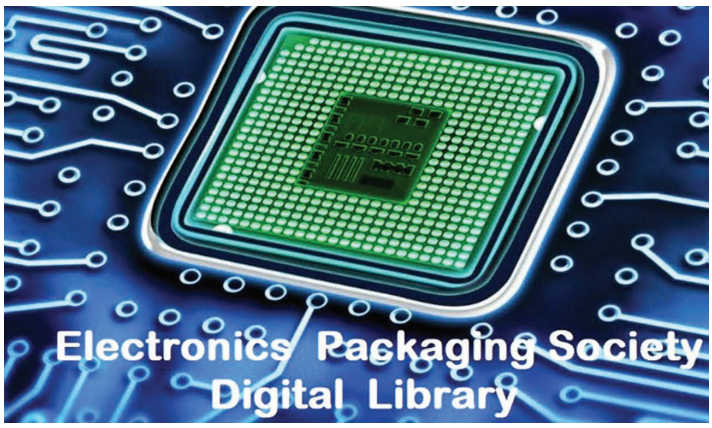
The members listed below were elevated to the grade of Senior Member in 2026.

The grade of Senior Member is the highest for which application may be made and shall require experience reflecting professional maturity. For admission or transfer to the grade of Senior Member, a candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE designated fields for a total of 10 years and have demonstrated 5 years of significant performance.

For additional information or to apply online: https://www.ieee.org/membership/senior/

Karsten Meier—Germany Section
Tengfei Jiang—Orlando Section
Pushkraj Tumne—San Fernando Valley Section
Hsiu-Che Wang—San Fernando Valley Section
Tushar Chauhan—Santa Clara Valley Section
Maria Gorchichko—Santa Clara Valley Section

MEMBERSHIP NEWS



Society Member Digital Library

The Digital Library allows members to view and download a wide selection of journals and conference proceedings.

Members have unlimited access to the full archive of EPS sponsored Transactions, journals, and conference proceedings via Xplore. This includes current and prior editions to the early nineties of more than 15 Transactions and journals and 35 conferences, including the ECTC, EPTC, ESTC, iTHERM and more.

IEEE EPS Student Chapter Programs

Student Chapter Promotion Program (SCPP)

To promote the formation of new EPS student chapters and the revival of current EPS student chapters which have become inactive, EPS has launched the Student Chapter Promotion Program (SCPP). Under the SCPP, six students from any university, which has an IEEE student branch, who are willing to serve as executive committee (exco) members in a new student chapter will be given free IEEE+EPS student memberships. The exco must ensure that their student chapter remains viable for the year. This includes the organization of at least two technical activities per calendar year, holding of annual elections and timely submission of required activity and financial reports every year. Additionally, faculty members who are willing to serve as Advisors to new student chapters will also be given free IEEE+EPS eMemberships where available, otherwise regular memberships will be provided. The Advisor's duties include advising on student chapter activities, endorsing financial statements where necessary, ensuring that annual election of new student exco members are held before end December, and required reports are submitted by the student exco in a timely manner every year. To request your

complimentary memberships, you must first have an IEEE account. If you do not have one you may create one here. Once all student members and the Advisor have an IEEE account, you may request your complimentary memberships here. Please note all student membership accounts must include an address, email, University name and expected graduation date before memberships can be applied.

Student Chapter Continuation Program (SCCP)

The Student Chapter Continuation Program (SCCP), will provide complimentary IEEE+EPS memberships for up to 6 student executive committee (exco) members per existing chapter provided they ensure that their student chapter remains viable for the following year. This includes the organization of at least two technical activities per calendar year, holding of annual elections and timely submission of required activity and financial reports every year. Annual election of the new exco should be held before the end December. The student chapter faculty Advisor will also be provided with a complimentary IEEE+EPS eMembership where available, otherwise a regular membership will be provided. To request your complimentary memberships, you must first have an IEEE account. If you do not have one you may create one here. Once all student members and the Advisor have an IEEE account, you may request your complimentary memberships here. Please note all student membership accounts must include an address, email, University name and expected graduation date before memberships can be applied.

An evaluation on the performance of subsidized student exco members and Advisors will be conducted in January each year based on reports submitted. Non-performing students and Advisors will not be subsidized for another year. All applications will be considered by a committee, and not all applications will be awarded. To support the organization of technical activities by student chapters, the student chapter exco may apply for subsidies of up to US$1500 per annum from EPS.

To apply for this program please submit your request here.

IEEE Senior Membership: Are You In?

If you have been involved in the electronics packaging field for 10 years or more, chances are that you probably already have the necessary qualifications to be an IEEE Senior Member.

Senior membership is the highest IEEE membership grade that can be applied for and is a recognition of sustained and significant performance in an IEEE-designated field. Individuals who are IEEE members can apply themselves for elevation to Senior Member or they can be nominated by others. Since a member can be nominated by someone else for Senior Membership, Society Chapters can play an important role in helping to identify and support applications for elevation. Nominating individuals in our Chapters is a great way to recognize their professional achievements and foster deeper personal and professional relationships with our peers. Individual members shouldn't hesitate to apply for Senior Member elevation on their own as well and call upon their IEEE colleagues for support for their application. The requirements for Senior Member eligibility are very straightforward:

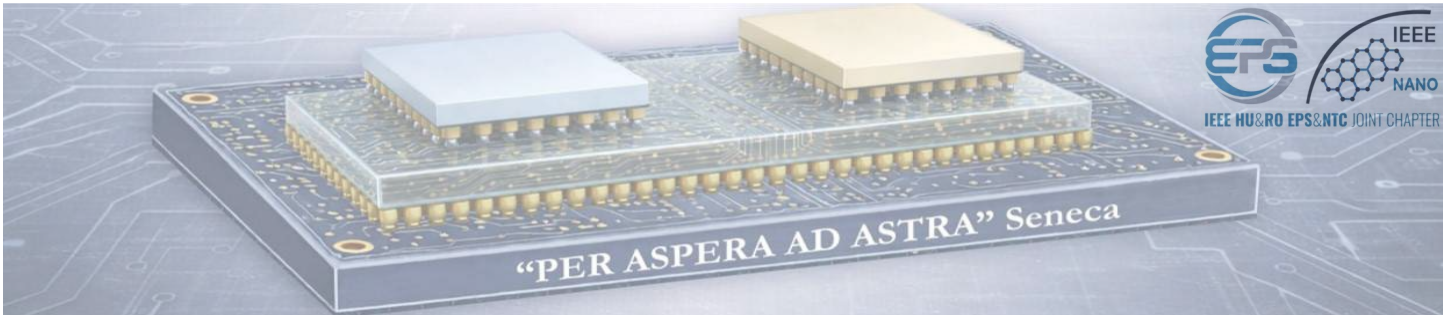
- The candidate shall be an engineer, scientist, educator, technical executive, or originator in IEEE-designated fields
- Candidates shall have been in professional practice for at least ten years
- Candidates shall have shown significant performance over a period of at least five of those years

As a member of EPS, the IEEE-designated field criteria will generally have been met. The criteria for ten years of professional practice can also take into account some portion of your educational experience as well as time spent in one's job or career, so a ten-year employment record isn't necessarily required. The final criteria of demonstrating significant performance over at least five of those ten years can be met in many different ways, including technical work, managerial responsibility, and publications to name a few. IEEE provides detailed information on the requirements for Senior Member grade at https://www.ieee.org/membership/senior/senior-requirements.html, along with sample cases that can be helpful for comparison to your own professional experiences.

Individuals applying for or nominating someone for Senior Member elevation can find additional information on the IEEE website at https://www.ieee.org/membership/grade-elevation.html and clicking on the Senior Member Grade link found there. Candidates applying for Senior Membership will need to supply three references from current IEEE members who are Fellows, Senior Members, or Honorary Members, and this is where EPS colleagues can support one another. Members of EPS chapters already have a group of local contacts that can help with nomination and reference support, simplifying and streamlining the process. Prospective applicants can find potential references through IEEE Collabratec via a link at the top of the EPS Membership page. There is also a link to the general Collabratec page on the MGA Senior Member Requirements page.

IEEE Senior Membership is a way for the Society to recognize the dedication and achievements of our members as well as a way to support our colleagues. If you have any questions about the Senior Membership application process or requirements, please don't hesitate to reach out to your local chapter or to us here at EPS for assistance.

Thanks
Alan Huffman, EPS VP Membership



IEEE EPS Newsletter Feature: Romanian Chapters Promoting Electronic Packaging Through the IEEE EPS & NTC Hungary-Romania Joint Chapter

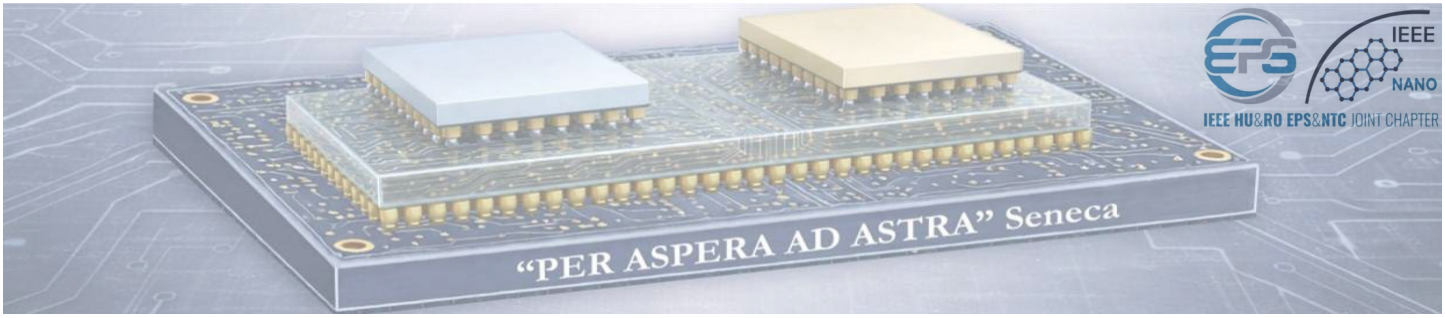
Romania's contribution to electronic packaging can be framed most clearly through the coordinated activity of the IEEE EPS & NTC Hungary–Romania Joint Chapter and its associated Student Branch Chapters, contests, and technical events. Rather than relying on isolated local initiatives, this ecosystem connects student competitions, chapter mentoring, summit activities, and conference participation into a visible structure for talent formation in electronic packaging.

The Real Story Is Continuity

From an IEEE EPS perspective, the strongest Romanian message is not simply that excellent contests exist, but that these contests are embedded in a recurring chapter environment. The Student Branch Chapters Summit make clear that the Hungary-Romania Joint Chapter is not a passive label attached to events; it appears also in the framework through which student chapters present their work and connect with one another. This creates something more valuable than visibility. It creates a rhythm. Students do not engage with electronic packaging only when a contest deadline appears; they encounter the field through chapter meetings, summit participation, mentoring, peer exchange, and the expectation that each year brings a new opportunity to learn, compete, and contribute. At the end of the newsletter, you can find the testimonial of **Ádám Csapody**, a part of this intricate rhythm as a student of the well-established IEEE NTC & EPS Student Branch Chapter Budapest University of Technology and Economics about his participation in further presented TIE competition.

TIE Shows What Packaging Education Can Look Like

One of the best examples for the contribution brought in electronic packaging is the **Technologies of Interconnections in Electronics (TIE) Industry-wide Student Challenges**, organized under the motto ***"A way to turn your HOBBY into PROFESSION"***. The event represents an initiative carried out through the collaboration between the **academic** and **industry** environments in Romania, having as its main objective the development of a community of students capable of capitalizing on the technical skills acquired during their studies and practical



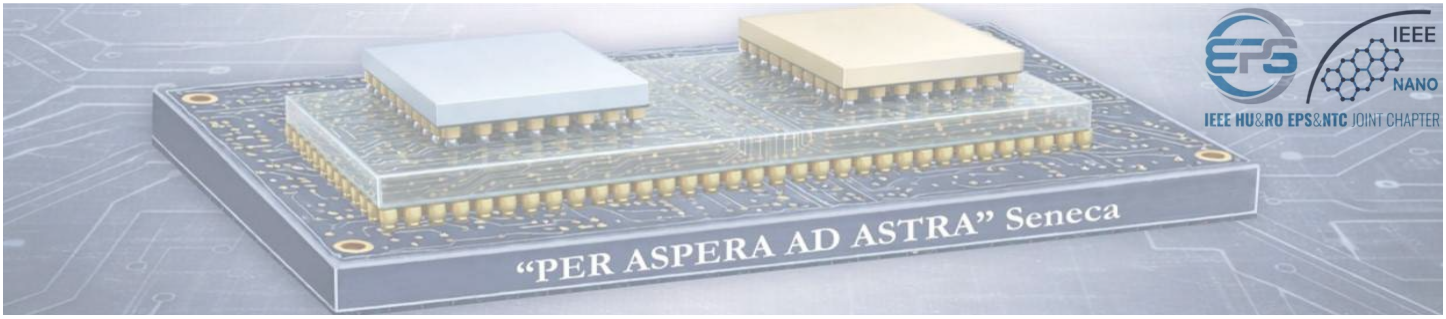
activities. The event focuses on real challenges from the electronics industry, especially in the field of electronic product design and development, offering participants the opportunity to use modern PCB design technologies. The certificate obtained following participation is recognized by employers and represents an advantage in professional development. At the same time, this event is designed by the industry to test students' skills in electronic packaging. It currently covers seven electronic packaging topics: electronic PCB design track (TIE-E), signal and power integrity (TIE-E+) mechanical CAD (TIE-M), structural analysis (TIE-M+), thermal analysis (TIE-T+), and advanced packaging topics such as 2.5D/3D integration (TIE-μ) and chip implementation (TIE-n). In other words, TIE teaches students that packaging is where these disciplines meet: electrical performance, heat, structure, manufacturability, and integration all have to coexist in the same design decision.

It is worth mentioning that **TIE may be a one-of-a-kind competition** in Europe where students tackle practical PCB design and packaging problems through a structured partnership between academia and industry, bridging theoretical knowledge with applied engineering. The name and format of the contest are registered as a **trademark**, underlining the maturity and distinct identity the competition has built over more than three decades. Through this structure, it has become an international platform focused on developing the skills necessary for electronic packaging activities. The **2026** edition marked the **35th** occurrence of the contest, organized in **Cluj-Napoca**, between **April 22nd–25th**, highlights its enduring role in connecting academic training with industrial practice. More information on this edition and all the previous ones can be found here.

The Summit Gives the Community a Voice

The October IEEE EPS & NTC Student Branch Chapters Summit is important for a different reason: it makes the community visible to itself. The event was created to bring students together, broaden horizons, and stimulate collaboration among chapters. That may sound simple, but in practice it addresses one of the biggest challenges in any technical field: students need to see that their local effort is part of something larger.

The summit does precisely that. It creates a stage on which chapters can present what they have done, compare approaches, and learn from one another. Just as importantly, the summit program ties student activity to current technical directions, including talks on maintaining active Student Branch Chapters and on topics such as chiplet technology, which place students in direct contact with contemporary packaging discourse. In 2026, the Summit will hold its 5th edition, confirming that it is no longer a one-off initiative but a recurring platform for student collaboration and visibility.



From an editorial point of view, this may be the clearest evidence of concerted action. A contest can reveal talent, but a summit reveals structure. It shows whether there is a living network capable of carrying enthusiasm from one campus to another and from one year to the next – you can visit the website here.

SIITME Completes the Picture

No account of Romanian activity in electronic packaging is complete without the **International Symposium for Design and Technology in Electronic Packaging (SIITME),** which remains the research and professional anchor of this landscape in Romania, this year reaching its 32nd edition. Its importance lies not only in longevity, but in the fact that it links student development with an international IEEE-facing environment in which packaging research, design technologies, and industry-oriented discussion can be encountered more formally.

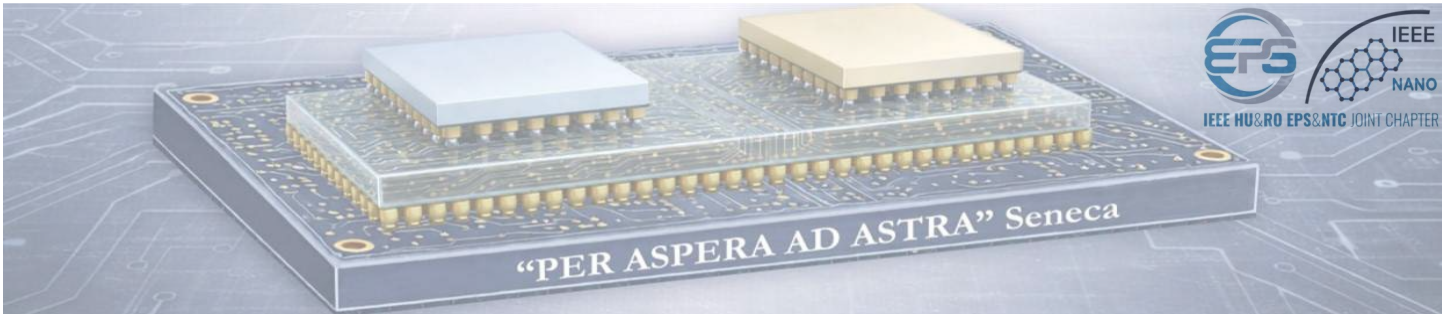
This is where the Romanian model becomes particularly strong. Students are not left at the level of contests alone. They can move from competition to chapter activity, from chapter activity to summit exchange, and from there toward a symposium environment that broadens their view of the field, all to the same goal – research in electronics packaging. For IEEE EPS, this progression is perhaps the most compelling part of the story because it shows how a community can cultivate both enthusiasm and depth. Anyone who would like to be part of the ecosystem can find more information here.

Beyond the HU & RO Joint Chapter Framework

Beyond the activities directly connected to the IEEE EPS & NTC Hungary-Romania Joint Chapter, Romania's contribution to the broader electronic packaging talent base is also visible in other established student competitions. The **Hard & Soft** International Computers Contest for Students in Suceava reached its 31st edition in 2026; it continues to strengthen practical skills in hardware, software, and system integration. Likewise, the **Tudor Tănăsescu** contest, which reached its 50th anniversary in 2026, remains a national benchmark for student excellence in electronics and related disciplines. Even when not directly framed as packaging events, such competitions help sustain the technical culture, student motivation, and engineering depth on which the packaging community ultimately relies.

A Stronger Framing for IEEE EPS & NTC

For IEEE, the Romanian story is strongest when presented as a chapter-coordinated ecosystem driven by the IEEE EPS & NTC HU & RO Joint Chapter and activated through local Student Branch Chapters. TIE offers direct exposure



to modern packaging problems, the October SBC Summit provides visibility and coordination, and SIITME connects student development with the research community. Seen together, these activities show a sustained and concerted effort to promote electronic packaging in Romania. The emphasis is not simply on organizing events, but on building a regional framework in which students can enter, grow, specialize, and remain connected to the IEEE EPS community through the HU & RO Joint Chapter structure.

Learning by Doing: A Conversation with Ádám Csapody on TIE 2026

Ádám Csapody, a student participant from Hungary and part of the IEEE NTC & EPS Student Branch Chapter Budapest University of Technology and Economics, came away from TIE 2026 with a view that many educators in electronic packaging would recognize immediately: competitions matter most when they do more than test knowledge—they reveal how engineering is actually practiced. In his reflections after the event, he described TIE not simply as a contest, but as an experience that forced him to adapt, rethink his assumptions, and better understand the gap between formal coursework and real design work.

What made you want to participate in TIE?

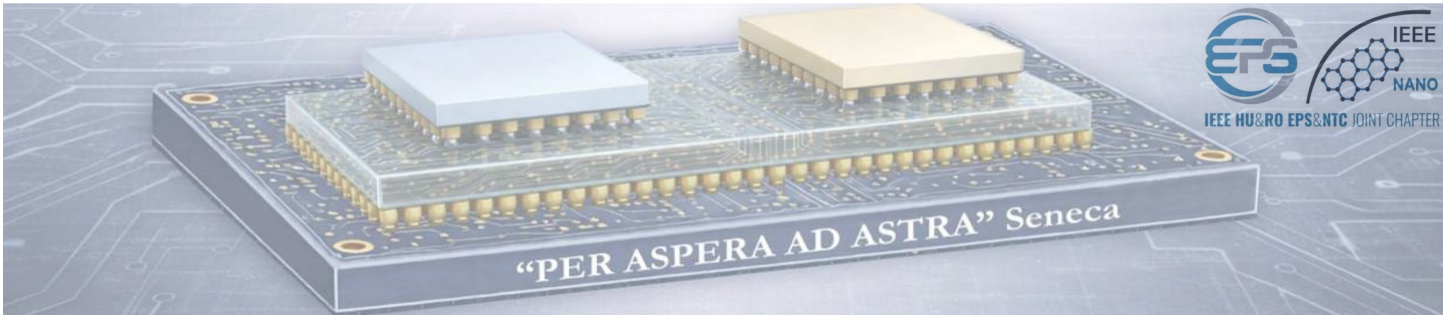
Ádám explained that his connection with TIE grew naturally from earlier contact with the community, noting that he had participated in SIITME the previous year and was personally invited to the event afterward. That pathway is revealing in itself: participation did not emerge from mass promotion, but from direct academic contact and from being brought into an existing professional and educational network.

Did the contest feel educational?

Very much so. One of the aspects he appreciated most was the evaluation process, which he described as a real discussion rather than a simple pass-or-fail judgment. He noted that when evaluators disagreed with a design choice, participants could explain the reasoning behind it, and a well-argued technical decision could be accepted. For students, that kind of dialog transforms evaluation into a learning moment, and his comments suggest that this was one of the strongest features of the TIE experience.

What are the barriers for students from Hungary?

Ádám was very clear that interest is not the problem. In his view, many students would like to participate, including in other categories such as TIE-E+ or TIE-μ, but preparation is difficult because the required knowledge is not



always taught in a coherent way within a classic university curriculum. He pointed out that at his institute, PCB design at this level is not taught directly, so preparing for TIE requires substantial self-learning.

He also emphasized a broader challenge: students may be attracted to advanced topics such as signal integrity or power integrity, but without accessible preparatory material they struggle to see how they could realistically get ready for such contests. His conclusion was straightforward and important: students are interested, but lack of knowledge pathways and lack of learning resources make participation harder than it should be.

How could more students be reached?

Here, his answer was especially practical. He argued that general university email announcements are often ineffective because students are overloaded and tend to ignore extracurricular messages unless they are directly connected to coursework or grades. Instead, he suggested that the most effective route is through teachers in relevant departments—lecturers who know the students, teach related material, and can promote opportunities in person during classes.

What was your overall impression of the contest?

His answer was unambiguous: he would gladly participate again. What made the experience valuable, in his view, was not only the competition itself, but the practical understanding it gave him of how to approach the task more effectively in the future. As he put it, reading about the contest or hearing others describe it offers only a general idea; actually going through the process gives a much clearer understanding of how everything works.

As Ádám's journey from SIITME to TIE illustrates, the real success of the IEEE EPS & NTC HU & RO chapter is not counted in events alone, but in the students who are more confident, more capable, and determined to come back even better prepared next year. In that sense, his testimonial is not simply a reflection on one competition, but a reminder of what this community is truly building: a lasting pathway into electronic packaging for the next generation.

Lect. Alexandra FODOR, Ph.D.
Student Branch Coordinator
IEEE EPS & NTC Hungary-Romania Joint Chapter

Become a Reviewer for the IEEE Transactions on Components, Packaging and Manufacturing Technology (T-CPMT)

Contribute to the research in your field by becoming an IEEE peer reviewer. Peer reviewers fulfill a vital role in the publishing process by giving detailed and professional commentary.

T-CPMT Associate Editors select potential peer reviewers who are experts in the topics that are covered in the article submission. After identifying reviewers, the system will send out invitations. Most invitations will include information about the article, such as the title and abstract, to help the reviewer decide if they should accept the invitation.

Selection Criteria:

- Minimum of bachelor's or master's degree in Material Science, Electrical Engineering, Mechanical Engineering or any related inter disciplinary field.
- Notable Publications in the field of expertise.
- Considerable Industry or academia experience.

Please submit your latest resume **here** or via the QR code below. Once you submit your resume the selection committee will review your application and get back to you.

Receiving a Peer Review Invitation

When you receive a review invitation, you should consider whether you have sufficient expertise in the article's subject area. You should also consider if you can complete the review by the deadline provided in the review invitation.

- If the answer to either of those questions is "no," you should promptly decline the invitation. Suggestions of other potential reviewers are always appreciated.
- If you decide to accept the invitation, follow the instructions in the email to signal your acceptance. You will then receive information on how to access the article and conduct your review.

Submitting Feedback and Timeline

T-CPMT uses an online submission system to facilitate peer review. Once you have accepted the review invitation, you will be given access to the article. You should evaluate the article with the following questions in mind:

- Is the study well designed and well executed?
- Is the existing body of relevant work acknowledged?
- Are the results interpreted and reported correctly? Have all other possible interpretations been duly considered?
- Are the results overly preliminary or speculative?
- Does the research contribute to the body of scientific knowledge in the field?
- Is the article appropriate for this publication?
- Is the article written in clear, concise language?

Follow the publication's instructions for submitting feedback, suggestions, and a recommended decision. Remember that your commentary should always be thorough and professional. Timeline for T-CPMT Journal:

a) AE/GE assigns reviewers: 5 Days
b) Reviews back: 14 Days
c) AE/GE + SAE make a decision – 7 Days

T-CPMT Reviewer Submission Form

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Publication Year: 2022, Page(s): 228–252

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John H. Lau
Publication Year: 2025, Page(s): 651–681

Mixed-Mode Fiber Array Alignment and Coupling to Photonic Integrated Circuits
Kamil Gradkowski
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Publication Year: 2025, Page(s): 2071–2082

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John H. Lau
Publication Year: 2023, Page(s): 399–425

Universal Chiplet Interconnect Express (UCIe): An Open Industry Standard for Innovations With Chiplets at Package Level
Debendra Das Sharma; Gerald Pasdast; Zhiguo Qian; Kemal Aygun
Publication Year: 2022, Page(s): 1423–1431

CPU Overclocking: A Performance Assessment of Air, Cold Plates, and Two-Phase Immersion Cooling
Bharath Ramakrishnan; Husam Alissa; Ioannis Manousakis; Robert Lankston; Ricardo Bianchini; Washington Kim; Rich Baca; Pulkit A. Misra; Inigo Goiri; Majid Jalili; Ashish Raniwala; Brijesh Warrier; Mark Monroe; Christian Belady; Mark Shaw; Marcus Fontoura
Publication Year: 2021, Page(s): 1703–1715

State of the Art and Outlooks of Cu–Cu Hybrid Bonding
John H. Lau
Publication Year: 2025, Page(s): 2575–2613

Thermally Conductive Electrically Insulating Electronics Packaging for Water Immersion Cooling
Tarek Gebrael; Arielle R. Gamboa; Muhammad Jahidul Hoque; Shayan Aflatounian; David Huitink; Robert Pilawa-Podgurski; Nenad Miljkovic
Publication Year: 2025, Page(s): 1222–1236

Best Associate Editor Award

To recognize the work and efforts of our Associate Editors, EPS instituted the Best Associate Editor Award. The 2026 recipients are:

Shubhra Bansal, Purdue University
Markondeya Raj Pulugurtha, Georgia Institute of Technology
Zhangming Zhou, Auburn University

2025 Transactions on CPMT Best Paper Awards

Each year, the Editors of the IEEE Transactions on Components, Packaging and Manufacturing Technology select the best papers published in the prior year. The papers are selected from among over 300 published papers and represent the best, based on criteria including originality, significance, completeness and organization.

Subscribers to this publication can access the papers on-line in IEEE Xplore at: http://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=5503870

"Broadband Characterization of Interconnects in Die Embedded Glass Interposer "Erdogan, Serhat; Jia, Xiaofan; Li, Xingchen; Kathaperumal, Mohanalingam; Agarwal, Ravi; Swaminathan, Madhavan; Volume 15, Issue 4, April 2025

"Co-Designed Silicon Photonics Chip I/O for Energy-Efficient Petascale Connectivity" Wang, Yuyang; Wang, Songli; Parsons, Robert; Sanyal, Swarnava; Gopal, Vignesh; Novick, Asher; Rizzo, Anthony; Lipson, Michal; Alexander L. Gaeta; Volume: 15, Issue: 8, August 2025

EPS Distinguished Lecturers

Ramachandra Achar, Ph.D. (7/1/2024–6/30/2028)
Department of Electronics, Carleton University
Ottawa, Ontario, CANADA
Topics: CAD tools and methodologies for interconnects, packages, and systems with an emphasis on signal, power and EMI integrity

Mudasir Ahmad (1/1/2026–12/31/2029)
Google
CA, USA
Topics: Internet of Things (IoT), Advanced Packaging, 2.5D, Heterogeneous Silicon Photonics, Advanced Reliability (Thermo-mechanical, Mechanical Shock), Numerical Modeling, Advanced Thermal Solutions, Stochastic Analysis, Bayesian Inference, Machine Learning, Artificial Intelligence

Kemal Aygün, Ph.D. (7/1/2024–6/30/2028)
Intel Corporation
Chandler, AZ USA
Topics: Package/socket/board/interconnect technologies, electrical simulation methodology and lab metrologies

Muhannad Bakir, Ph.D. (1/1/2024–12/31/2027)
School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA USA
Topics: Emerging interconnection architectures and technologies; heterogeneous system design and integration

Wendem Beyene, Ph.D. (7/1/2024–6/30/2028)
Meta
San Jose, CA
Topics: Electrical modeling and simulation techniques for analysis of interconnects, packages, and systems. Machine learning techniques

Chris Bower, Ph.D. (7/1/2025–6/30/2029)
Daktronics, Inc.
North Carolina, USA
Topics: Novel assembly methods, elastomer stamp micro-transfer-printing, heterogeneous integration, three-dimensional integration, manufacturing of micro-assembled displays and other large-format electronics.

Tanja Braun, Ph.D. (7/1/2023–6/30/2027)
Fraunhofer IZM
Berlin, Germany
Topics: Advanced Packaging, Heterogeneous Integration, Flip Chip, Chiplet, Fan-out Wafer and Panel Level Packaging.

Ken Butler, Ph.D. (7/1/2025–6/31/2029)
WattsButler LLC
Texas, USA
Topics: Semiconductor test and reliability, AI/ML applications and edge computing for test and reliability, test challenges in advanced packaging and heterogeneous integration, product and test engineering, design for testability and automatic test pattern generation

Francesco Carobolante (1/1/2026–12/31/2029)
Intel Corp.
Reno, Nevada, USA
Topics: Power management and integrations, Technology Roadmapping

Kuan Yew Cheong, Ph.D. (1/1/2024–12/31/2027)
School of Materials and Mineral Resources Engineering
Universiti Sains Malaysia
Topics: Materials, Physical Failure Analysis

Xuejun Fan, Ph.D. (1/1/2024–12/31/2027)
Department of Mechanical Engineering
Lamar University
Beaumont, TX USA
Topics: Design, modeling and reliability in micro-/nano- electronic packaging and microsystems

Mukta Farooq, PhD. (1/1/2026–12/31/2029)
IBM Research
Yorktown Heights, New York, USA
Topics: 2.5D/3D packaging technologies, Cu TSV integration and reliability, HI architectures for AI systems

Deepak Goyal, Ph.D. (7/1/2024–6/30/2028)
Intel Corp.
Phoenix, AZ USA
Topics: 2.5D/3D packaging technologies, Failure mechanisms, Failure analysis methods and challenges.

Przemyslaw Gromala, Ph.D. (1/1/2026–12/31/2029)
Robert Bosch GmbH
Reutlingen Germany
Topics: Power module design, advanced packaging, and reliability under harsh environments.

Madhu Iyengar, Ph.D. (7/1/2024–6/30/2028)
Google
Mountain View, CA, USA
Topics: Thermal component and system design for packages, servers, and data centers.

Subu Iyer, Ph.D. (7/1/2025–6/3/2029)
University of California, Los Angeles
Los Angeles, CA USA
Topics: Heterogeneous Integration; Flexible hybrid electronics; 3D interposer, and wafer scale integration and stacking.

Beth Keser, Ph.D. (1/1/2024–12/31/2027)
Zero ASIC

San Diego, CA USA
Topics: Fan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; Advanced Packaging; Introduction to Packaging; and photoimageable liquid polymer filmsFan-Out Wafer Level Packaging and Wafer Level Packaging structures; processes, materials, tools, design rules and roadmaps; photoimageable liquid polymer films.

Pradeep Lall, Ph.D. (1/1/2024–12/31/2027)
Auburn University
Auburn, AL USA
Topics: Semiconductor Packaging, Modeling and Simulation, Reliability in Harsh Environments, Shock/Drop/Vibration, Cu Wirebonding, Flexible Hybrid Electronics, Additive Manufacturing, Prognostics and Health Management, LEDs, Micro CT Measurements

John H. Lau, Ph.D. (1/1/2024–12/31/2027)
Unimicron Technology Corporation
Palo Alto, CA USA
Topics: Electronics and Photonics 2D and 3D packaging and manufacturing

Ravi Mahajan, Ph.D. (7/1/2024–6/30/2028)
Intel Corporation
Arizona, USA
Topics: Advanced Packaging Architectures, Assembly Processes and Thermal Management

James E. Morris, Ph.D. (1/1/2024–12/31/2027)
Department of Electrical and Computer Engineering
Portland State University
Portland, Oregon USA
Topics: Electrically conductive adhesives, Nanopackaging, Discontinuous Metal Film Applications in Electronics Packaging

Rajen Muguran, Ph.D. (7/1/2026–6/30/2030)
Texas Instruments
Dallas, TX, USA
Topics: Multiphysics and System Co-Design modeling for complex analog and mixed-signal packaging, mmWave/THz signal integrity, power electronics packaging, and System-Level EMI/EMC modeling, analysis, and characterization.

Katherine "Kitty" Pearsall, Ph.D. (7/1/2024–6/30/2027)
President of Boss Precision Inc.
Independent Consultant
Austin, TX USA
Topics: Supply chain, component qualification and end quality; Leadership

Eric D. Perfecto (1/1/2024–12/31/2027)
IBM Research
Poughkeepsie, NY USA
Topics: Fine pitch interconnect, chip to chip and chip to laminate connection, UBM and solder selection, chip package interaction and 2.5D fabrication

Mark Poliks, Ph.D. (1/1/2024–12/31/2027)
Binghamton University (SUNY)
Binghamton, NY USA
Topics: Materials and Processes, Advanced Manufacturing, Flexible Hybrid Electronics, High Speed and Additive

Markondeya (Raj) Pulugurtha, Ph.D. (1/1/2026–12/31/2029)
Florida International University,
Miami, FL USA
Topics: Health monitor systems, Embedded-components/wearables, photonics biosensors, RF electronics, antennas

Gamal Refai-Ahmed, Ph.D. (7/1/2026–6/30/2030)
Xilinx
San Jose, CA USA
Topics: Thermo-mechanical Semiconductor and Electronics Industry Roadmap and directions, Advanced holistic Thermo-mechanicalsolution, assembly and reliability ofHeterogeneous Packagingand Silicon Photonics, Future thermo-mechanical technology, architecture for component and system

Katsuyuki Sakuma, Ph.D. (7/1/2024–6/30/2027)
IBM T.J. Watson Research Center; Visiting Professor at Tohoku University, Japan
New York, NY USA
Topics: 3D integration technologies, bonding technologies, advanced packaging, and biomedical sensors

Jose Schutt-Aine, Ph.D. (7/1/2024–2/2027)
University of Illinois
Champaign, IL USA
Topics: High-Frequency Measurements, Mixed-Signal Design, High-Performance Computing, electromagnetic Modeling, Signal Integrity, CAD Tools for Interconnects and Packages, Machine Learning for High-Speed System Modeling

John Shalf (1/1/2024–12/31/2027)
Lawrence Berkeley National Laboratory
Berkeley, CA USA
Topics: HPC System Integration, System Integration, Photonics and Packaging

Dongkai Shangguan, Ph.D. (7/1/2023–6/30/2027)
Thermal Engineering Associates, Inc.
San Jose, CA USA
Topics: Heterogeneous Integration and SiP; Electronics Packaging and Miniaturization; Materials; Thermal management; Reliability; Electronics manufacturing technology; Flexible hybrid electronics

Rohit Sharma, Ph.D. (1/1/2023–12/31/2026)
Indian Institute of Technology Ropar
Punjab, India
Topics: Design of High-speed Graphene-based and 2D materials-based nanoelectronics; Electrical-Thermal co-design of electronic packages and microsystems; Application of Machine Learning in design and analysis of interconnects; Heterogeneous integration.

Ephraim Suhir, Ph.D. (1/2024–12/2027)
Los Altos, CA 94024 USA
Topics: Accelerated life testing; Probabilistic physical design for reliability; Bonded assemblies; Thermal stress; Predictive modeling; Fiber optics structures: design for reliability; Dynamic response to shocks and vibrations

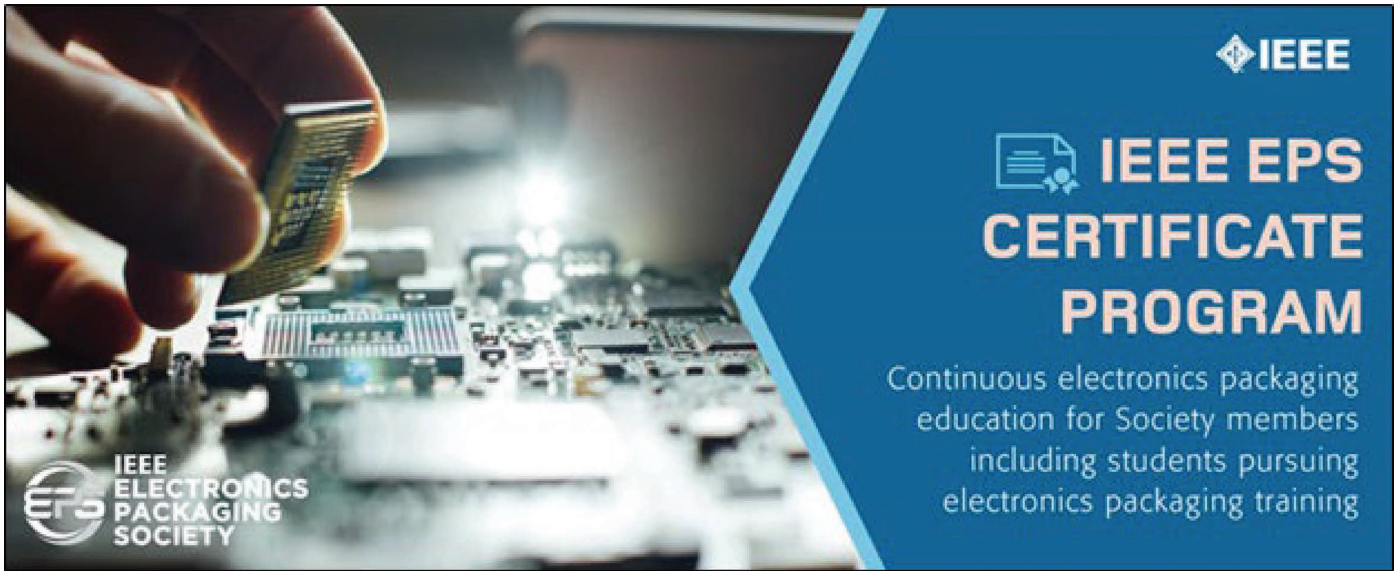
Andrew Tay, Ph.D. (1/1/2023–12/31/2026)
SHINE Center, National University of Singapore
Singapore
Topics: Thermomechanical reliability of microelectronics packages; Thermal and failure analysis of microelectronic devices; Thermal management of electronic and EV battery systems; Solder joint reliability; Delamination and fracture; Moisture effects; Modelling and simulation.

Manos Tentzeris, Ph.D. (7/1/2023–6/30/2027)
Georgia Institute of Technology
Atlanta, GA USA
Topics: RF/mmW/3D/electronics industry/nanotechnology/materials/packaging/3D printing/energy harvesting-zero power

Rao Tummala, Ph.D. (1/1/2024–12/31/2027)
Microsystems Packaging Research Center (PRC)
Georgia Institute of Technology
Atlanta, GA USA
Topics: Electronics Packaging

E. Jan Vardaman (1/1/2024–12/31/2027)
TechSearch International, Inc.
Austin, TX USA
Topics: International developments in semiconductor packaging, manufacturing and assembly; SiP: Business and technology Trends; drivers in advanced packaging; Flip chip and wafer level packaging

Paul Wesling (1/1/2024–12/31/2027)
Saratoga, CA USA
Topics: Origins of Silicon Valley and the Electronics Packaging Society; the IEEE/SEMI/ASME Heterogeneous Integration Roadmap and how to use it (as editor for the 2019 Roadmap).



EPS Certificate Program

The IEEE Electronics Packaging Society Certificate Program provides a pathway for early and mid to late-career professionals to highlight their accomplishments.

Criteria for all Certificates: Must be an IEEE Electronics Packaging Society Member.

There are three Certificates you may apply for, which are noted below.

EPS Achievement Certificate

The first level ***EPS Achievement Certificate*** is aimed at early-career professionals working in the field of electronics packaging. It is especially intended to encourage the career development of young professionals including advanced graduate students.

Criteria: Current EPS Member

To receive your certificate, 15 professional development hours (PDHs) must be completed. This can be obtained from a combination of the following:

1) IEEE EPS Webinar (1 PDH) – must complete **PDH evaluation**.
2) IEEE EPS Distinguished Lecture (1 PDH) - must complete the **PDC online survey.**
3) Professional Development Courses – **must complete survey and CEU credit form**. Previous ECTC PDCs from the last 10 years can be used towards this if the CEU application was completed at the time of the course. PDCs from ESTC and EPTC 2018 and forward can be used.

- Electronic Components and Technology Conference (USA) = 4 PDHs
- Electronic Systems-Integration Technology Conference (Europe) = 3 PDHs
- Electronic Packaging Technology Conference (Asia) = 4 PDHs

4) Author of IEEE T-CPMT and/or EPS conference paper(s) (5 PDHs) – paper must be published in IEEE Xplore within the last 5 years.
5) Reviewer for IEEE T-CPMT (3 Reviews = 5 PDH) within the last 5 years.

Once you have completed any combination of the above and received 15 PDHs, please complete the certificate form to request your Electronics Packaging Society Certificate of Achievement.

EPS Distinguished Achievement Certificate for Technical Leadership and Expertise

Criteria: Must be a current EPS member

There are five high-level focus areas for this new certificate. These areas include:

1) Being a recognized authority of technical expertise in electronics packaging.

Examples include being an advanced member of the technical staff at a company (e.g. Fellow, Senior Technical Staff, Distinguished Engineer, etc.), making technical contributions as a Member or Fellow of professional associations/societies related to electronics packaging (e.g., IEEE, IMAPs, SMTA, ASME, etc.), and being an invited speaker at companies, technical conferences, and EPS Chapter meetings.

2) Being a subject matter expert (SME) in electronics packaging at conferences, keynotes, webinars, blogs, etc.

Methods to demonstrate participation as a SME include abstracts accepted and papers presented at conferences, giving keynote lectures at conferences or professional society meetings, presenting webinars for EPS and other IEEE Societies, and serving on technical panels at conferences and other venues.

3) Demonstrating sustained technical contributions to the electronics packaging industry.

Examples of sustained technical contributions include publishing well-cited technical papers at conferences and in journals, book chapters, and patents; serving as an editor of a journal or reference book; and being a leader or participant in industry blogs, focus groups, technical roadmaps, newsletters, and forums.

4) Documenting advanced technical recognitions in electronics packaging.

Methods to document technical recognitions include receiving technical awards from a company, institute, professional society, or academic institution; being the acknowledged inventor of a seminal technology or process important to industry; serving as the point person for global high-level task force activity; and being elected to be a Member of an organization such as the US National Academy of Engineering, Royal Academy of Engineering, Chinese Academy of Engineering, IBM Academy of Technology, etc.

5) Provide at least one endorsement letter.

Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1 - June 30 and Aug 30–Oct 31.

EPS Distinguished Achievement Certificate for Professional Engagement and Service

Criteria: Must be a current EPS member

There are four high-level areas of focus for this new certificate. These areas include:

1) Demonstrating leadership in the electronics packaging field.

Leadership and broad impact activities in electronics packaging can be documented from outstanding accomplishments during industry employment or for notable volunteer contributions to the profession and society.

2) Illustrating broad impact/influence in the electronics packaging field.

Examples of significant professional service include serving as an officer in a technical society at the international, national, or local chapter level; participating in packaging related technical committees, councils, or affinity groups; contributing to technology roadmaps such as the Heterogeneous Integration Roadmap

(HIR); and receiving a professional society or industry award based on service contributions.

3) Providing extensive service and "give back" to the profession and/or industry; and

Documentation of "give-back" to one's technical community can be accomplished via demonstrations of coaching and mentoring of co-workers, young professionals, and students.

4) Provide at least one endorsement letter.

Nominations for the Distinguished Achievement Certificates will be accepted two times per year: Jan 1 - June 30 and Aug 30–Oct 31.

More details on the Certificate Program are available on the EPS website at https://eps.ieee.org/education/eps-certificate-program/. The EPS Certificate Program is sponsored by the IEEE EPS VP Education and is offered only to EPS members. For questions, please contact Eric Perfecto (eperfecto@gmail.com).

EPS Achievement Certificate

Congratulations to the EPS Member on receiving the IEEE Achievement Certificate from the IEEE Electronics Packaging Society and completing the required number of professional development hours.

Vinod Arjun Huddar, Rambus, Inc.

EPS Resource Center

The IEEE EPS Resource Centers contains valuable, technical content from reputable experts to enhance research or industry work, implement trainings, or earn CEU/PDH credits—all of which are universally available on demand.

IEEE EPS Resource Centers benefits include:

- Access to valuable technical community content
- Access to content 24 hours a day, 7 days a week through an easy-to-use global portal
- Available at no cost for EPS members
- Opportunities to earn CEUs and PDHs

Popular webinars:

- Heterogeneous Integration Roadmap (HIR) Chapter 1 Overview
- AI for Thermal Management of Electronic Systems: A Pathway to Digital Twins
- From Automation to Autonomy: Agentic AI in Chip Assembly and Manufacturing Test
- Heterogeneous Integration Roadmap (HIR) Chapter 22 Interconnects for 2D and 3D Architectures
- Laser-based Micro/Nano-scale Manufacturing for Semiconductors and Electronics

Just a reminder to EPS members that you have free access to all of our content on the EPS Resource Center, including webinars and conference best papers.

https://resourcecenter.eps.ieee.org/

76th ECTC Conference – *An Event to Crush Records*

Submitted by
Karsten Meier, Assistant Program Chair,
IEEE EPS ECTC 2027

I. Introduction

This year's IEEE EPS Electronic Components and Technology Conference (ECTC) took place in Orlando, Florida, at the JW Marriott & The Ritz-Carlton Grande Lakes Resort, from May 26–29, 2026. The conference brought together a stunning total of 2,730 junior and senior experts from industry and academia but also numerous students – another record for ECTC. Attendees came from 29 countries.

As our community recently lost a truly respected leader with the passing of Dr. William (Bill) Chen (ASE) on March 27, 2026, 76th ECTC was honorably dedicated to his memory. Over his distinguished, decades-long career, Bill was instrumental in shaping ECTC into the conference it is today. We are sure, by setting new records, providing a crowded platform for the global electronics packaging community and engaging students, 76th ECTC proudly carried on the incredible legacy and mentorship mindset of Bill.

The 76th ECTC included 423 technical papers, which were organized into 36 oral sessions and five interactive presentation (IP) sessions. There were eight special sessions, five plenary sessions and a keynote opening the conference. The 16 professional development courses (PDCs) were attended by 714 attendees, also a new record. The conference had 136 exhibitors at the ECTC Technology Exhibition. Additionally, the conference benefited from a strong number of sponsors (50) and sponsorships (52), further testament to the value delivered by this flagship IEEE EPS conference.

Preparations for the 76th ECTC conference began on November 6–7, 2024 in Dallas, where the ECTC Executive Committee and representatives of 10 technical sub-committees met and decided about the conference sessions based on 918 abstracts received – one more all-time record. In the end, 47% of the submissions were accepted. In a testimony to the diversity of the industry and the conference, abstracts were received from 21 countries with the United States, South Korea, Japan, and Taiwan leading the way in number of abstract submissions.

The new IT system that was installed for ECTC 2025 proved its efficiency also during preparation and operation of ECTC 2026 and will help for the years after. The system includes session organization, manuscript submission and review, exhibitor management, registration, the conference app and many more features, representing a big help in the management and operation of this year's event and future ones to come. The conference program successfully followed the renewed program that was implemented in ECTC 2025:

- Student engagement program: invited students from local schools and colleges were invited to get in touch with the electronic packaging community first time – in fact, 21 students enjoyed this great opportunity; student volunteers helped to run the conference; BSc&MSc and PhD student teams competed in the "*Innovative Solutions for Advanced Packaging in Microelectronics*" students' competition.
- Special sessions on Tuesday, two parallel blocks with special sessions - the rooms were fully occupied.
- A 76th ECTC Gala Reception with great food and drinks going along with live music.

The 76th ECTC conference kicked off on Tuesday, May 26, 2026. Each day at ECTC begins with the Speakers Breakfast in which the presenters and session chairs meet and take care of the preparatory work for their respective sessions. The PDC Chair, Kitty Pearsall, provided instructions to the PDC instructors and proctors on Tuesday morning, and Bora Baloglu, the Program Chair, hosted the breakfast meetings on Wednesday through Friday.

As usual, the first day of the conference, the Tuesday following Memorial Day, featured PDCs, a workshop related to Heterogeneous Integration Roadmap (HIR), and a variety of special sessions. This year, the conference had eight morning PDCs, running from 8 a.m. to noon, and another eight afternoon PDCs, running from 1:30 to 5:30 p.m. The courses continued to serve as a convenient way for students and engineers to quickly get "up to speed" on the current topics of importance in electronics packaging.

On Tuesday, parallel to the PDCs, there was an opportunity to contribute to the IEEE EPS Heterogeneous Integration Roadmap (HIR) special workshop chaired by Ravi Mahajan, Intel

Corporation; Subu Iyer, UCLA; Anne Meixner, HIR Fellow; Benson Chan, Binghamton University; Rockwell Hsu, Cisco Systems; and Jose Schutt-Aine, UIUC. The workshop started at 8:00 a.m. and lasted until 5:00 p.m. The workshop was divided into four topics:

- Additive Electronics Manufacturing (AME) for Advanced Packaging,
- Metrology for Advanced Packaging: Challenges, Innovations, and Industry Impact,
- Emerging Technologies and
- Neuromorphic Computing.

This year eight special technical sessions were organized. The following topics were covered in the morning sessions:

- "*Quantum Infrastructure for AI Applications: Packaging Challenges and Roadmap*" organized by Rabindra N. Das, MIT Lincoln Laboratory, and Pavel Roy Paladhi, NVIDIA.
- "*New Packaging Technologies Enabled by Panel Level Integration*" organized by Venkata Mokkapati, AT&S, and Markus Leitgeb, AT&S, and Rozalia Beica, Rapidus.
- "*System Integration Challenges of Large-Size and High-Power Components for High-Performance Computing and AI Applications*" organized by Tae-Kyu Lee, Cisco Systems, Inc., and Mike Gallagher, Qnity Electronics.
- "*Electrical-Thermal-Mechanical Co-Design in High-Performance Packaging*" organized by Ning Ye, Sandisk, and Tiwei Wei, University of California, Los Angeles.

After lunch, another four sessions provided a platform to learn and discuss about the topics:

- "*AI-Enabled Electronic Design Automation for Multi-Physics Advanced Packaging*" organized by Ian O'Connor, Ecole Centrale de Lyon, France, and Jose Schutt-Aine, University of Illinois at Urbana-Champaign.
- "*Photonic-Based Systems for AI and Exascale Computing*" organized by Stéphane Bernabé, CEA-LETI, and Lars Brusberg, Corning Inc.
- "*Enabling Next-Generation Advanced Packaging Technology From Wafer to Panel*" organized by Kuldip Johal, MKS Instruments, and Beth Keser, Volantis Semiconductor, and Lihong Cao, ASE.
- "*Innovative Materials for Advanced Packaging – Materials for Packaging, Integration, and Performance*" organized by Zia Karim, Yield Engineering Systems, and Ksenija Varga, EV Group.

The ECTC Student Reception, sponsored by Texas Instruments, was held on Tuesday from 5:00 to 6:00 p.m. Numerous student attendees took advantage of the opportunity to mingle and network with professionals in the field. Right after this, the General Chair's Speakers Reception was given from 6:00 to 7:00 p.m. for Speakers and Session Chairs. These receptions provided a great start to the conference and helped prepare everyone for the following three days filled with technical presentations and networking opportunities.

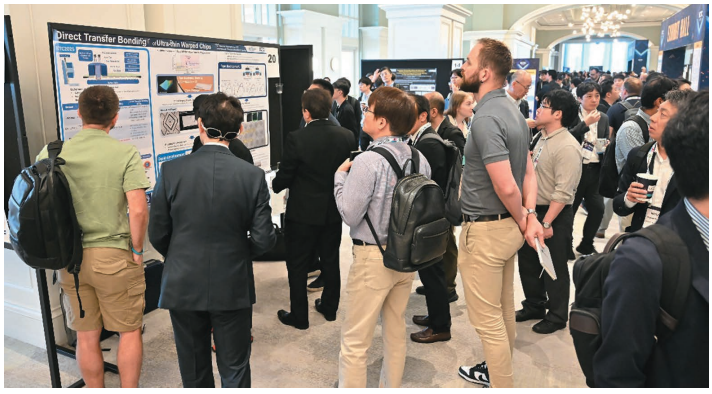
The Young Professionals Networking Event took place from 6:45 to 7:45 p.m. and was chaired by Aakrati Jain, IBM. As last year the discussion was organized and very successfully conducted in a fishbowl setup, and everybody was invited to join. The format proved its importance and networking effect. We are sure to see this event next year again.

The Tuesday program ended with a well-attended IEEE EPS Seminar on "*Redefining System Integration: The Rise of Organic Substrates in the Chiplet Era*" from 7:45 to 9:15 p.m., chaired by Takashi Hisada and Yasumitsu Orii, both from Rapidus. Panelists were invited from Shinko, Unimicron, ASE, Intel, and Synopsys.

On Wednesday, the conference day started with the Keynote presentation. Michael Mayer – University of Waterloo and ECTC 2026 General Chair introduced this year's keynote speaker Tien Wu, CEO of Advanced Semiconductor Engineering, Inc. The title of the keynote was: "*Advanced Packaging and the Future of System Optimization*" (76th ECTC keynote). In his keynote, Tien Wu focused on high performance computing and the challenge of power delivery from the device to the datacenter level, which are core topics of the ECTC conference, and important future areas of interest.

Tien Wu was unparalleled catching the audience's full attendance when communicating his key message that we are reaching the physical and thermal limits in electronic packaging and semiconductor technologies. Everyone - *the room was packed with hundreds of folks standing* – understood that our efforts have to focus on the future needs to address power delivery and latency. Voltage regulators and co-packaged optics were exemplarily named approaches to solve these challenges. He pointed out, that the semiconductor landscape is expected to see tremendous growth for hardware companies with advanced technologies and integrated systems. Our ecosystem is to expect a paradigm shift in the industry requiring partnerships across research fields, technology domains, business models, geographics, and supply chain.

After the keynote, six technical sessions ran in parallel throughout each of the three days. Each oral session featured seven paper presentations, and the interactive presentation sessions featured between 28 and 39 papers. Wednesday morning started six well attended sessions with titles: "*Enabling Fan-In and Fan-Out Wafer/Panel Level Packaging Technology*", "Co-Packaged Optics", "*Advances in Low Temperature Hybrid Bonding*", "*Breakthrough in Pitch Scaling With Advanced Bonding Technology*", "*RF and High-Speed Design for mmWave and Sub-THz*", and "*Thermo-Mechanical Interactions With Reliability*". In parallel, the first of five interactive sessions took place from 10:00 a.m. – 12:00 p.m., with 28 paper presentations discussing research on "*Thermo-Mechanical Stress and Reliability Analysis for Materials in Future Packaging*".



The Student Engagement Program, chaired by Ibrahim Guven (Virginia Commonwealth University) and co-chaired by Przemyslaw Gromala (Robert Bosch Kft), took place throughout the day, welcoming 21 undergraduate students from local universities and colleges, *i.e.*, Valencia College and University of Central Florida. Highlight of the day for the students was a private meeting with ASE's CEO Tien Wu just after he gave his inspiring keynote speech.

During lunch, ECTC 2026 General Chair, Michael Mayer, welcomed all attendees and introduced the Executive Committee. Afterwards, Awards for Best and Outstanding Papers from the 75th ECTC 2025 and the Intel Best Student Paper Award, as well as the TI Best IP Student Award were presented by Vice General Chair Przemyslaw Gromala.

In the afternoon, high attendance in the sessions was noticeable, with the topics "*Heterogeneous Integration: The New Horizons*", "*Die-to-Wafer Hybrid Bonding: Current Advancements and Future Directions*", "*Advances in Thermal Materials and Encapsulation*", "*Reliability of Large Body High Performance Computing and AI Packaging Solutions*", "*Signal Integrity Design for High-Speed Interfaces*", and "*Characterization and Modeling for Process and Multi-Domain Analyses*". In parallel to the technical session, the second interactive session about "*Photonics, mmWave Applications, and Emerging Technologies*" took place from 2:30–4:30 p.m., with 34 paper presentations. Thursday's interactive presentations sessions were filled in the morning with 38 presentations in the field of "*Bonding Processes and Analysis in Next Generation Interconnects*" and in the afternoon with 32 presentations covering "*Materials, Manufacturing, and Assembly Techniques in Advanced Packaging Solutions*". On the last conference day, Friday, the student interactive session with 39 presentations took place and covered a broad field of research. Attendees of the ECTC rated all oral and interactive session paper ratings only through the ECTC mobile app.

The ECTC Technology Exhibition area hosted 136 exhibitors. Exhibitors had multiple resources available within their booth, offering introductions, brochure materials, staff contact information, and an opportunity to submit inquiries and directly discuss with exhibit members their latest developments, tools, and services. In the late Wednesday afternoon, there was a chance to meet all the exhibitors during the exhibition reception and enjoy excellent food and drinks.

Wednesday and Thursday evening the ECTC Student Competition and Start-Up Innovation Challenge took place, respectively. The sessions offered competing pitches of both student teams and start-ups followed by deliberation of a jury panel, awards announcements, and networking. The ECTC Student Competition asking for "*Innovative Solutions for Advanced Packaging in Microelectronics*" that attracted contributions from 40 students was organized by Przemyslaw Gromala, Robert Bosch Kft, and Ibrahim Guven, Virginia Commonwealth University. Rozalia Beica (Rapidus), and Farhang Yazdani (BroadPak), chaired the Start-Up Challenge on "*The Light Age: Strategic Investment in Photonics to Power the Next Computing Era*". Congratulations go to the winners:

- Student Competition, BSc & MSc Level Category: "*Low-Cost Robust Thermal Solution for High Power AI/Datacenter Processors*"
  Hiroyuki Sakuma, Dennis Y. Gao, Lok Teng Cheung Georgia Institute of Technology, USA
- Student Competition, PhD Level Category: "*Tetrahedral Amorphous Carbon as a Cu Diffusion Barrier in Through Silicon Vias Deposited by Filtered Cathodic Vacuum Arc*"
  Sihang Shao, Li Ying, Nanyang Technological University, Singapore
- Start-Up Challenge: "*Lightwire Interconnects*" – *optical interposers with monolithic integration of GaN, microLEDs to enable 500 links/mm at Gbps with <0.5pJ/bit and BER <15*
  Andrew Kim, CEO of New Silicon Corp.

On Thursday from 8:00 to 9:15 a.m., the ECTC Plenary session on Data Center Needs "*Efficiency Is Not Enough: Are We Solving the Wrong Problem in Data Center Energy Use?*" was organized by Masha Gorchichko, Marvell Technology, Inc., and Jan Vardaman, TechSearch International, Inc. Panelists were from Celestial AI, Accelsius, IBM, Google, AMD, and Microsoft. Top experts discussed key challenges and opportunities in improving energy use in data center applications, spanning hardware, system architecture, software, and infrastructure.

Thursday's technical morning sessions were well attended and covered the topics "*Advances in Thermal Design and Characterization*", "*RDL and Fan-Out Interconnections", "Optical Interconnects*", "*Assembly and Manufacturing: 3D Stacking and Thermal Solutions*", "*Digital Twin and AI in Advanced Packaging and Interconnect Security*", and "*Hybrid Bonding: Advanced Processing and Modeling*".

The IEEE Electronics Packaging Society President, Jeffrey Suhling, presided over the luncheon on Thursday and presented the EPS Society Awards. The recipients were presented with a certificate and very warm applause from the audience.

After the luncheon technical sessions continued, including: "*Substrate Core Innovations: Glass, Ceramic, and Silicon*", "*Performance Analysis and Metrology of High-Bandwidth Electrical and Optical Interconnects*", "*Novel Laser-Based Technologies and Fine-Pitch Interconnects*", "*Reliability of High Current and High Power Packaging Solutions*", "*Power Integrity Analysis for High-Performance Computing*", and "*AI and Machine Learning for Electronics Packaging*".

The 76th ECTC 2026 Technical Program Committee meeting was held on Thursday at 5:15 p.m. Tanja Braun, who will serve as the Program Chair for 77th ECTC 2027, chaired this meeting and presented the statistics of the 76th ECTC and the timeline for the run-up to the next year's 77th ECTC that is planned to be held in Denver, Colorado. Tanja Braun also introduced Karsten Meier of Technische Universität Dresden as the Assistant Program Chair of the 77th ECTC. This meeting also enabled the ECTC technical program subcommittees to get in touch with potential new members of their committees. All interested attendees of the conference are welcome to join this meeting.

The traditional ECTC Gala Reception took place on Thursday evening. It was the social highlight of the week for the conference attendees, exhibitors, sponsors, and their guests. It was a memorable reception though following the expectation setting last years's birthday party. It was an excellent place for networking, meeting friends or partners, and starting new professional relationships. The evening filled with live music truly became the social highlight of 76th ECTC. It was a rewarding time celebrating the success of the ECTC by socializing and enjoying the excellent food and beverages that were supported by the Gala Reception Gold and Silver sponsors.

On the last day of the conference, Benson Chan, Binghamton University, David McCann, Amkor Technology, and Jeff Suhling, Auburn University, chaired the IEEE EPS President's Panel discussion entitled "*Data Centers in the Age of AI: Challenges and Solutions*". Panelists well known in the community including Arvind Kumar, IBM, Nandish Mehta, NVIDIA, Farnood Rezaie, Cisco, and Bahgat Sammakia, Binghamton University discussed projected energy demands of AI data centers that are about to exceed the available energy sources as well as the upcoming cooling needs. Throughout the panel, technology, economic and environmental challenges posed by AI data centers were taken into account.

The Friday morning technical sessions were also well attended, covering the topics "*Optical and Electrical Design for High-Performance Computing*", "*Advanced Wafer-to-Wafer Hybrid Bonding*", "*Innovation in Glass and Dielectric Materials for Heterogeneous Integration*", "*Beyond Silicon: Innovation in Glass Substrates and Panel Level Packaging*", "*Innovation in Metallization, Alignment,*

Additive Manufacturing, and Low Temperature Interconnection", and "*Thermal Management and Cooling Simulation*".

During Friday's luncheon, there was a traditional raffle chaired by Alan Huffman - ECTC Exhibit Chair, with several prizes from our sponsors including a hotel stay, free conference registration, IEEE EPS membership, books, and many other cool gadgets.

Friday afternoon included the sessions: "*3D Integration, TSV, and Hybrid Bonding Innovations*", "*Solder and Through Via Interconnections: Material & Process Innovations*", "*Emerging Materials and Interconnect Technologies for Advanced Packaging*", "*Optimizing Power Delivery, Thermal Management, and Metrology Solutions for Next-Generation Devices*", "*Reliability of Advanced Automotive, AI, and Interconnect Packaging Solutions*", and "*Flexible Electronics and Thin-Assembly Warpage*".

Overall, the 76th ECTC was an amazing experience, giving the opportunity to meet in an excellent location, and have a lot of discussions regarding future development of electronic components. It was again a record setting ECTC conference with respect to attendance. One of the many highlights was Wednesday's keynote about "*Advanced Packaging and the Future of System Optimization*". The Gala All attendees recognized the reception on Thursday evening as a very enjoyable social highlight with food and drinks. ECTC continued to have a very strong exhibitor presence, excellent sponsorship, and many high-quality technical presentations with excellent presentation attendance. The ECTC Executive Committee sincerely thanks all the attendees, exhibitors, and conference sponsors (ECTC 2026 platinum sponsors: Amkor, ASE, IBM) for their support as well as all the committee members and chairs who are volunteering their time to help organize the technical sessions and make ECTC such a success year after year. Very special thanks also to our excellent event management team for tackling all foreseen and unforeseen challenges. THANKS!!! See all the conference pictures at Flickr, the videos on Youtube and keep in touch with the ECTC through LinkedIn.

The 77th ECTC will be held at the Gaylord Rockies Resort & Convention Center, Denver, Colorado, June 1–4, 2027. Przemyslaw Gromala from Robert BoschKft will be the General Chair of this conference. The Call for Papers and PDC proposals will be available at www.ectc.net, and the abstract submission will close on October 05, 2026. So, get your abstracts ready for submission as soon as abstract submission opens.

I look forward to meeting you at 77th ECTC 2027 to be held at the Gaylord Rockies Resort & Convention Center, Denver, Colorado, June 1–4, 2027.

75th 2025 ECTC Best Paper Awards

1) Best Session Paper
Direct-to-Silicon Liquid Cooling Integrated on CoWoS® Platform
Co-authored by Yu-Jen Lien, Sing-Da Jiang, Cheng-Chieh Hsieh, Han-Jong Chia, Tsunyen Wu, Chien-Chih Lin,Ke-Han Shen, Szu-Wei Lu, Kathy Yan, Kuo-Chung Yee, Douglas C.H. Yu, Taiwan Semiconductor, Manufacturing Company, Ltd., Hsinchu, Taiwan, R.O.C.

2) Best Interactive Presentation Paper
An Effective 3D Thermal Network Integrated With Deep Learning for Improved Prediction of the 3D Thermal Properties of Complex Packaging Patterns
Co-authored by Jeong-Hyeon Park, Jaechoon Kim, Sukwon Jang, Sungho Mun, Eun-Ho Lee, Samsung Electronics Co. Ltd, Yongin-Si, Republic of Korea.

3) Outstanding Session Paper
Development of Glass Core Build-up Substrate With TGV
Co-authored by Masahiro Sunohara, Jun Yoshiike, Hiroshi Taneda, Yoko Nakabayashi, Noriyoshi Shimizu, Shinko Electric Industries Co., Ltd, Nagano, Japan.

4) Outstanding Interactive Presentation Paper
Novel Packaging Platform Based on Bridge Dies With Top and Bottom I/O Connections on Standard Substrates
Co-authored by Jae-Sung Lim, Sangkyu Jang, Yong Gyu Jang, Yongnam Koh, Jin-Wook Jang, R&D Center, HANA Micron Inc., Republic of Korea, Jayden Donghyun Kim, HANA Micron Inc., Asan, Korea.

5) Intel Best Student Paper
Physics-Informed Neural Networks for SAM Image Enhancement with a Novel Physics-Constrained Metric for Advanced Semiconductor Packaging Inspection
Co-authored by Shajib Ghosh, Nitin Varshney, Antika Roy, Patrick Craig, Md Mahfuz Al Hasan, Sanjeev J. Koppal, Navid Asadizanjani; ECE Department, University of Florida, Rayhane Ghane-Motlagh, ficonTEC Service USA Inc.; Nelly Elsayed, University of Cincinnati.

6) Intel Outstanding Student Paper Award
Packaging and Integration of Multifunctional Brain Computer Interface
Co-authored by Ziqi Jia, Ariel David Cerpa, Gloria J. Kim, Yong-Kyu Yoon, University of Florida, Gainesville, United States.

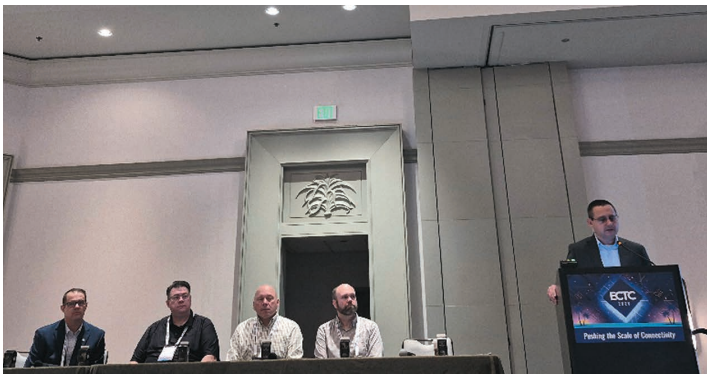
7) TI Best IP Student Award
Parasitic Extraction and Signal Integrity Analysis of Memristor-Based Crossbar Arrays for Neuromorphic Computing
Co-authored by Tahsin Binte Shameem, Hanzhi Ma, Yi Zhou, Zohreh Salehi, José E. Schutt-Ainé, Urbana-Champaign, University of Illinois, Urbana, IL, USA.

IEEE EPS Society Award Winners

Recipient	Award	Contribution
Shi-Wei Ricky Lee	IEEE Rao R. Tummala Electronics Packaging Award	For contributions through research on lead-free soldering reliability and promoting the globalization of electronics packaging.
Bongtae Han	Outstanding Sustained Technical Contribution Award	For contributions to electronic packaging design for reliability and workforce development, especially measurement of advanced package behavior and material properties.
Shaw Fong Wong	Electronics Manufacturing Technology Award	For over 25 years of full spectrum semiconductor leadership – from silicon sorting and 3D packaging to system solutions – driving yield, reliability, and high-volume production for generations of revolutionary products.
Ravi Mahajan	William Chen Distinguished Service Award	For sustained excellence in leadership and service to the IEEE community helping promote global industry-academia collaboration in Heterogenous Integration.
Tiwei Wei	Exceptional Technical Achievement Award	For outstanding contributions to thermal management in 2.5D and 3D system integration, including advancements in multi-physics and multi-scale modeling, electronic cooling, and thermal packaging materials.
Fan Wu	Outstanding Young Engineer Award	For her groundbreaking innovations in the development of find pitch interconnect, molded integrated circuits, and adhesive dispense technologies that enable impactful contributions and industry advancements to MEMS packaging, microfluidic devices and beyond.
Waldir Ventura Filho	Regional 1-7 & 9 Contributions Award	For pioneering live organizational unit creation, achieving record-breaking EPS growth in Region 9, and demonstrating exceptional leadership in technical sustainability and global member engagement.
Rohit Sharma	Regional 10 Contributions Award	For leadership in advancing microelectronics education, pioneering high-speed interconnect research, and exceptional service in promoting the activities of the IEEE Electronics Packaging Society in India.
Ram Krishna	PhD Fellowship	For a novel signal integrity modeling methodology that bridges fabrication variations and operating conditions to enable rapid yield prediction for die-to-die interconnects in advanced packaging systems.

Heterogeneous Integration Roadmap Workshop 2026 Report

At ECTC 2026, a special workshop on heterogenous integration was organized by Heterogenous Integration Roadmap technical working group members. The workshop opened with a tribute to William Chen and a review of the HIR. The team announced the availability of the 2025 edition of the roadmap (0.9 version) and informed the attendees that later this summer all 25 chapters will be updated to their final version.



ECTC 2026 HIR Session 1 Speakers

The first session covered cutting-edge additive technologies as well as more mature printing methods used in advanced electronics packaging. Speakers from academia and industry presented their latest technologies in the field and then answered questions in a roundtable format. All the topics presented in the session are covered in the latest update of Chapter 25 of the IEEE HI Roadmap on Additively Manufactured Electronics (AME). The detailed overview of those topics provided during the session, and the discussion that followed, will certainly inform future updates and impact packaging professionals that attended the event.

The second session featured five speakers from NIST who discussed their work on metrology methods of interest for advanced packaging technology. The presented research covered defect detection and classification, reliability modeling of polymers (e.g. TIM and underfills), characterization of process induced thermo-mechanical changes in materials and remote thermal sensing. The session concluded with a Q&A with the attendees.

In the afternoon, the HIR Emerging Technologies session highlighted the rapid evolution of AI-driven next-generation hardware. Key discussions spanned from in-space electronics manufacturing (Purdue) to the future of high-speed networking, where experts from Marvell and Meta explored how Co-packaged Copper (CPC) and Optics (CPO) will support 224G and 448G channels for AI/ML and LLM workloads. The test manufacturability challenges

ECTC 2026 HIR Session 2 Speakers


ECTC 2026 HIR Session 3 Speakers

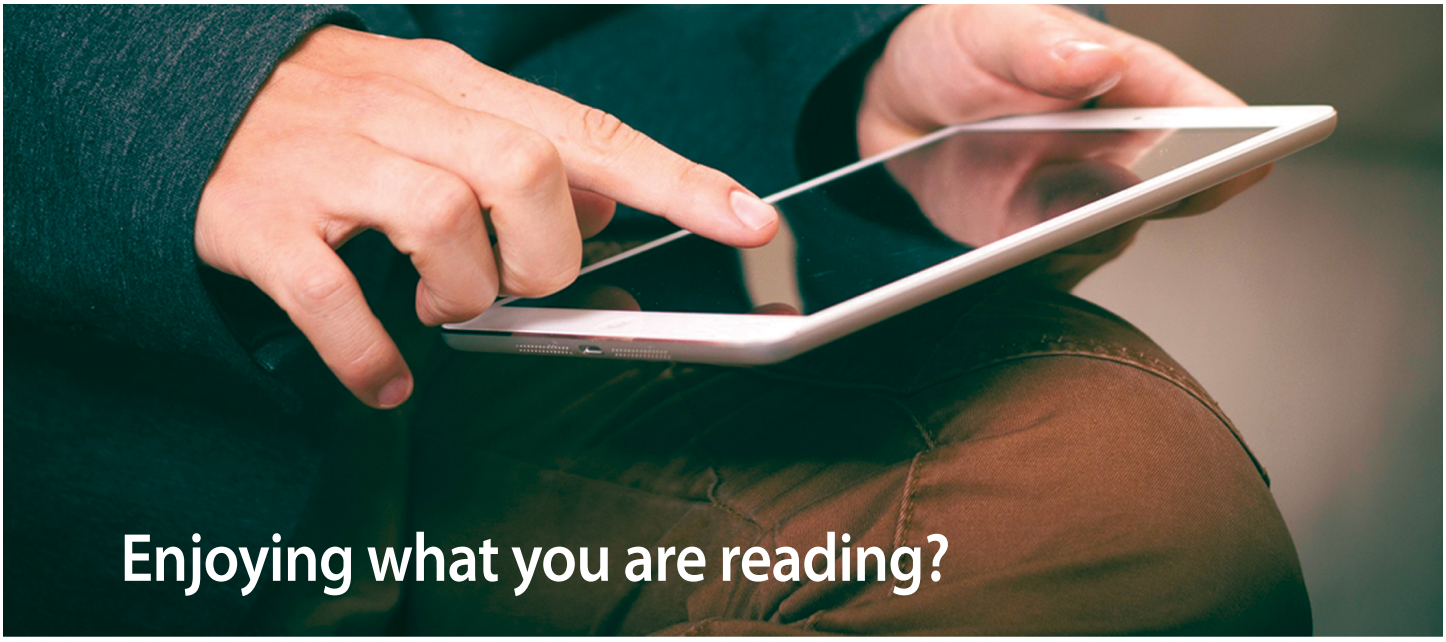
ECTC 2026 HIR Session 4

HIR Session Audience

for CPO (Intel) highlighted the need for standardization to scale this technology. This third session also covered breakthroughs in 3D heterogeneous integration—specifically 3D X-DRAM (Neo Semiconductor) and advanced packaging materials (FIU)—concluding with Lam Research's insights on the manufacturing equipment necessary to scale these innovations.

The fourth and final session provided attendees with insights into the latest research on neuromorphic computing. With the prospective applications for edge computing components the speakers covered a broad spectrum of technology research that included memory architecture hierarchies, usage of emerging devices such as ferro electronics, benchmarking TCAM technologies and signal integrity modeling for hardware-software co-design.

The presentations for which speakers granted permission to distribute can be found at this location.



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We'd love to hear your thoughts!

Drop us a note and let us know how we're doing.

Send the editor-in-chief an e-mail!

EPTC 2026

IEEE EPS Flagship Conference in Asia Pacific Region

28th Electronics Packaging Technology Conference

EPTC2026

1st - 4th December 2026
Marina Bay Sands Expo & Convention, Singapore

ABOUT EPTC

The 28th IEEE Electronics Packaging Technology Conference (EPTC2026), organised by the IEEE RS/EPS/EDS Singapore Joint Chapter and co-sponsored by IEEE EPS, is the flagship IEEE EPS conference in the Asia-Pacific region. Since 1997, EPTC has brought together the global electronics packaging community across materials, assembly, reliability, interconnects, heterogeneous integration, wafer-level packaging, 2.5D/3D technologies, IoT, 5G, smart manufacturing, automation and AI. Held from 1-4 December 2026, the conference will feature keynotes, technical sessions, panels, workshops, exhibitions and networking. Supported by over 100 technical experts, EPTC2026 expects to exceed last year's 800+ attendees and showcase leading technologies and products.

ABOUT EPTEX

The Electronics Packaging Technology EXPO (EPTEX) is a technology-driven platform that unites the advanced packaging ecosystem to accelerate innovation and collaboration. Bringing together semiconductor companies, equipment and materials suppliers, engineers, R&D leaders, research organisations, universities and regional partners, EPTEX enables meaningful technical exchange and strategic partnerships. Beyond product displays, the EXPO features live demonstrations, start-up showcases, student innovation contests and MoU signings—turning industry dialogue into actionable roadmaps for next-generation electronics packaging and heterogeneous integration.

CONFERENCE TOPICS

1. Advanced Packaging
2. Assembly and Manufacturing
3. Electrical Simulation & Characterization
4. Emerging Technologies
5. Interconnection Technologies
6. Materials and Processing
7. Mechanical Simulation & Characterization
8. Optoelectronics & Display Packaging
9. Quality, Reliability & Failure Analysis
10. Smart Manufacturing & Equipment Technology
11. Thermal Management & Characterization
12. Wafer-Level & Panel-Level Packaging

EPTC WEBSITE

CALL FOR EXHIBITORS / SPONSORS

Details of the exhibition and sponsorship opportunities are available here: Exhibitors/Sponsors. For enquiries, please email exhibition@eptc-ieee.net or sponsorship@eptc-ieee.net.

CALL FOR INVITED TALKS

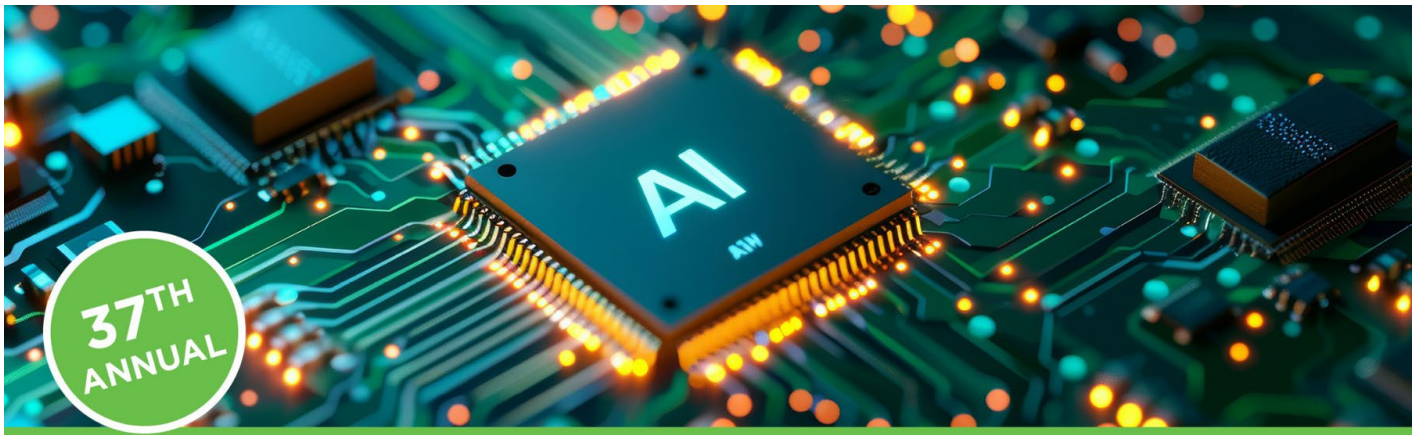
You are invited to submit an abstract between 500-750 words long and clearly state the purpose, methodology, results (which must include data, drawings, graphs, or photographs), and conclusions of the work. Abstracts for invited talks must be received by July 31, 2026. Your submission must have been cleared up by your management and co-authors as applicable and include the authors' affiliations and email addresses. All submissions should be in English, either in pdf or MS Word. Abstract should be in 1 of the 12 Electronic Packaging Conference topics. 1 pager bio with a photo embedded needs to be provided along with the abstract for consideration of invited talks. ⩾ 10 years of electronic packaging experience in academia/ research institutes/ industry is typically preferred. Abstract for invited talk needs to be directly emailed to techchair@eptc-ieee.net. Acknowledgement will be sent within a day of submission. Abstract for invited talks will be reviewed by the organizing committee and the decision will be notified separately by 31 August 2026. Invited talks are exempted from the full paper submission for publication in the conference proceedings. Invited talks will be scheduled for the first presentation on each track and 30 min will be assigned for each invited talk. Invited talk needs to be technical in nature and strictly no commercial content.

ORGANIZED BY

IEEE Singapore RS/EPS/EDS Chapters

SPONSORED BY

IEEE ELECTRONICS PACKAGING SOCIETY



ELECTRONICS PACKAGING SYMPOSIUM

SEPTEMBER 9-10, 2026

Binghamton University • Binghamton, NY

Presented by: IEEC, Binghamton University • CAMM, Binghamton University • GE Aerospace • IBM Research

S3IP IEEC Integrated Electronics Engineering Center — Binghamton University

GE Aerospace

IBM

IEEE Electronics Packaging Society

ASE Group

S3IP CAMM Center for Advanced Microelectronics Manufacturing — Binghamton University

Binghamton University, GE Aerospace and IBM Research are proud to host the **37th Annual Electronics Packaging Symposium**. The program will include two days of exciting invited presentations with a focus on supply chain interconnectivity.

We invite you to join us for this event on Sept. 9-10, 2026, at Binghamton University, N.Y. We look forward to seeing you there.

The symposium brings together leaders in academia, industry and government to network and discuss the latest advances in the field of electronics packaging, and to bring value from the varying viewpoints of each sector.

The program will also include keynote presentations and student poster sessions. The goal of the symposium is to have those who attend walk away with insights, career-building opportunities and the knowledge of having been an integral part of the advancement of the electronics packaging field.

Session topics will include: future of computing for HPC/AI, flexible, additive and wearable electronics, heterogeneous integration, photonics packaging, thermal challenges, advanced substrates and power electronics.

The full agenda is still taking shape.

Visit https://www.binghamton.edu/ieec/eps for the most up-to-date details about panel discussions, a special workshop and registration.

TOPICS WILL INCLUDE:

- **Future of Computing for HPC/AI**
- **Flexible, Additive and Wearable Electronics**
- **Heterogeneous Integration**
- **Photonics Packaging**
- **Thermal Challenges**
- **Advanced Substrates**
- **Power Electronics**

For sponsor, exhibit and participant info, contact:

Benson Chan
Associate Director, S3IP
Binghamton University
(607) 777–4349

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www.binghamton.edu/ieec

BUSS 2026

Build-Up Substrate Symposium — Highlights & Report

170+	8	30+
ATTENDEES	TECHNICAL SESSIONS	SPEAKERS & PANELISTS

Theme: *Next-Gen Substrates: Accelerating Innovation in the AI Era*

OVERVIEW

THIRD ANNUAL EDITION

The third annual IEEE Build-Up Substrate Symposium convened on May 19–20, 2026, in Milpitas, California, drawing more than 170 attendees from across the global substrate ecosystem. Substrate manufacturers, material suppliers, equipment companies, semiconductor firms, research organizations, and end users gathered under the theme *Next-Gen Substrates: Accelerating Innovation in the AI Era*.

As artificial intelligence, high-performance computing, and heterogeneous integration continue to drive unprecedented demands on semiconductor packaging, advanced substrates have emerged as a critical enabler of system performance. What was once considered a supporting technology is now a key factor in determining package density, power delivery, signal integrity, manufacturability, and overall system scalability.

Read the full edition here

IEEE Tech Summit: Ethical AI

Shape the Future of Ethical AI at the 2026 IEEE Tech Summit

Be part of the conversation shaping the future of artificial intelligence at the **2026 IEEE Tech Summit: Ethical AI**, taking place **1–2 October** in **Budapest, Hungary**. This unique two-day summit serves as a platform for exploring how AI can be designed, governed, and implemented in ways that prioritize transparency, fairness, accountability, and societal benefit.

Through inspiring keynote presentations, engaging panel discussions, breakout sessions, and networking opportunities, the 2026 IEEE Tech Summit will foster meaningful dialogue on creating AI that is trustworthy, responsible, accountable, and advancing society for the benefit of humanity.

Join us in one of Europe's most vibrant cities and help shape the future of ethical AI. **Register today and reserve your place at the forefront of AI innovation.** https://tech-summit.ieee.org/ethical-ai-2026

Check out the THERMINIC 2026 Workshop programme!

The technical programme for THERMINIC 2026 – the 32nd International Workshop on Thermal Investigations of ICs and Systems is now available online. Join us September 16–18, 2026, in Berlin, Germany, for Europe's leading workshop dedicated to thermal management and reliability challenges in electronic components and systems.

This year's diverse programme features technical presentations, poster sessions, industrial keynotes, Professional Development Courses, an exhibition, and numerous networking opportunities. Topics include thermal simulations, materials innovations, reliability, high-performance computing, electronics cooling, thermal management of data centers, and emerging thermal technologies.

Explore the full technical programme here: https://therminic.eu/programme.

We are pleased to welcome keynote speakers from IBM Research, ams-OSRAM, and Infineon Technologies, who will share insights into current challenges and future developments in their respective fields.

Additionally, participants can benefit from two Professional Development Courses (PDCs) held prior to the workshop, covering experimental statistics and advanced thermal management for next-generation package designs.

Register by July 29, 2026 to take advantage of the extended Early Bird registration deadline: https://therminic.eu/registration.

We look forward to welcoming you to THERMINIC 2026 in Berlin!

Announcing 3D-PEIM 2026 Tutorial and Panel Session

3D-PEIM 2026, the premier international symposium dedicated to 3D power electronics packaging and heterogeneous integration, will take place November 16–19, 2026, at Arizona State University in Tempe, Arizona. The symposium will bring together researchers, manufacturers, and industry leaders to discuss emerging technologies and manufacturing approaches shaping the future of advanced power packaging.

As part of the 2026 technical program, the Organizing Committee is pleased to announce the addition of four expert-led tutorials and a special panel session to be held on Monday, November 16. The tutorial program will provide attendees with in-depth perspectives on key technical challenges and industry developments across advanced packaging, reliability, materials, and system integration.

Tutorial presentations will include **Advanced Packaging**, presented by George Dogiamis (Deca Technologies), Chanyeop Park (ASU), Hongbin Yu (ASU), and Chris Bailey (ASU); **Die-Attach by Metal Powder Sintering: The Science and Practice** by G.-Q. Lu (Virginia Tech); **Digital Twin-Driven Reliability and Prognostics in Power Electronics Systems** by Jong Eun Ryu (North Carolina State University); and **Trends in Magnetic Material Properties to Meet the Challenges of Supporting High-Performance Computing** by Matt Wilkowski (Würth Electronics). Tutorials will be held from 1:00 PM to 5:15 PM, with registration available during the conference registration process opening in June. Attending the tutorials and panel session is free. Conference registration is not required.

Following the tutorials, 3D-PEIM 2026 will host a panel session titled "**Key Challenges for 3D Power Electronics Packaging/Manufacturing**," featuring academic and industry experts discussing current manufacturing, reliability, and integration challenges facing next-generation power electronics systems. Tentatively confirmed panel participants include Ravi Mahajan (Intel/HIR Chair), Doug Hopkins (North Carolina State University/HIR Power Chapter), Chris Bailey (Arizona State University/HIR Modeling and Simulation Chapter), Pat McCluskey (University of Maryland/HIR Thermal Chapter), George Dogiamis (Deca Technologies), and Francesco Carobolante (IoTissimo).

The 2026 symposium will also feature six plenary speakers, seven technical sessions, poster presentations, industry exhibits, and guided tours of ASU's MacroTechnology Works facility. Technical focus areas include advanced packaging and 3D integrated modules, thermal management, design and simulation, reliability and failure analysis, passive components, power delivery and energy storage, and materials for advanced packaging.

Conference registration will open June 8, 2026. Additional information regarding sponsorship opportunities, exhibitor participation, and registration can be found at https://www.3d-peim.org/.

We look forward to welcoming attendees to Arizona State University for 3D-PEIM 2026.

President's Column (*Continued from page 1*)

Following ECTC this year, IEEE EPS will sponsor flagship events in Europe and Asia, including the ESTC Conference to be held in Helsinki, Finland in September, and the EPTC Conference to be held in Singapore in December. Additional major technically sponsored international events coming later in 2026 include ICEPT (Xi'an, China, August), IEMT (Kuala Lumpur, Malaysia, October), IMPACT (Taipei, Taiwan, October), ICSJ (Kyoto, Japan, November), and IDSPS (Visakhapatnam, India, December).

The EPS Board of Governors (BoG) has planned and budgeted an extensive set of new initiatives and projects to support students, who are the future of our packaging industry. We will award over 160 travel grants this year to support university student attendance at our ECTC, ITherm, ESTC, and EPTC conferences. In addition, a new program was established to support US$1,000 education grants to graduate students who are involved in research and development in the electronics packaging field. The first 25 grants will be awarded this August. To support undergraduate students, a series of packaging summer schools was established this year, and the first four funded programs will run later this summer in India, Kenya, and the United States. Finally, over 50 undergraduate students have been supported over the past year with US$1,000 grants to participate in one semester long hands-on experiences in packaging under the mentorship of a faculty member.

EPS remains the preeminent source for technical information on packaging and Heterogeneous Integration (HI). In addition to our conferences and associated proceedings, we sponsor an archival journal, the IEEE Transactions on Components, Packaging, and Manufacturing Technologies (T-CPMT), which achieved a new high in Impact Factor in 2025. Our 12 Technical Committees (TCs) sponsor a variety of activities including webinars, newsletter technical articles, benchmarking studies, and specialized workshops. Finally, EPS continues to be a strong sponsor of the Heterogeneous Integration Roadmap (HIR). All Chapters of the HIR were updated and published earlier in 2026, and planning for the next revisions is underway. EPS members have access to all of this information through our EPS Digital Library within IEEExplore and our online EPS Resource Center.

None of these achievements would be possible without the tireless dedication of our EPS Board of Governors, committee volunteers, and outstanding staff. Your enthusiasm and commitment keep us uniquely positioned to serve the global engineering community and advance technology for the benefit of humanity. Whether you are a long-standing member or are joining us for the first time, we invite you to join us in the technical activities of the Society. Together, let us continue leading the future of electronic packaging.

Jeff Suhling
IEEE EPS President 2026–2027

Upcoming Conferences

In pursuit of its mission to promote close cooperation and exchange of technical information among its members and others, the EPS sponsors and supports a number of global and regional conferences, workshops and other technical meetings within its field of interest.

All of these events provide valuable opportunities for presenting, learning about, and discussing the latest technical advances as well as networking with colleagues. Many produce publications that are available through *IEEE Xplore*.

2026 27th International Conference on Electronic Packaging Technology (ICEPT)
Xi'an, China
Aug 05–07, 2026

2026 IEEE 11th Electronics System-Integration Technology Conference (ESTC)
Helsinki, Finland
Sep 09–Sep 11 2026

2026 IEEE International Conference on Quantum Computing and Engineering (QCE)
Toronto, Canada
Sep 13–18, 2026

2026 32nd International Workshop on Thermal Investigations of ICs and Systems (THERMINIC)
Berlin, Germany
Sep 16–18, 2026

2026 48th Annual EOS/ESD Symposium (EOS/ESD)
Frisco, TX
Sep 26–Oct 5, 2026

2026 IEEE 71st Holm Conference on Electrical Contacts (HOLM)
Kansas City, Missouri USA
Oct 03 2026–Oct 08 2026

2026 IEEE 35th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS)
Fort Worth, TX
Oct 18–21, 2026

2026 21st International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)
Taipei, Taiwan
Oct 19–22, 2026

2026 IEEE CPMT Symposium Japan (ICSJ)
Kyoto, Japan
Nov 10–12, 2026

2026 IEEE Symposium on Reliability for Electronics and Photonics Packaging (REPP)
Los Angeles, CA
Nov 12–13, 2026

2026 Sixth International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)
Tempe, AZ
Nov 16–19, 2026

2026 8th International Conference on the Challenges, Opportunities, Innovations and Applications in Electronic Textiles (E-Textiles)
Pilsen, Czech Republic
Nov 2–26, 2026

2026 IEEE 28th Electronics Packaging Technology Conference (EPTC)
Singapore
Dec 01–04, 2026

2026 IEEE Electrical Design of Advanced Packaging and Systems (EDAPS)
Chandigarh, India
Dec 14–16, 2026

Top Conference Papers based on Usage

2026 IEEE 76th Electronic Components and Technology Conference (ECTC)

(May 26–29, 2026)

100-nm-level Post-Bond Accuracy and High-Yield Die-to-Wafer Hybrid Bonding System Using Non-Contact Die Transfer
Kentaro Mihara; Takashi Hare; Hirofumi Sakai; Shimpei Aoki; Fumihiro Inoue; Akira Uedono; Murugesan Mariappan; Hiroyuki Hashimoto; Takafumi Fukushima

2.5D and Vertical Integration for Real-time Co-Optimization of Voltage Regulation and Power Gating in HPC Systems
Salma Abdelzaher; Inna Partin-Vaisband

3D Analysis of Hybrid Copper Bonding through X-ray Photon-Counting Nano-CT Imaging
Till Dreier; Darius Rückert; Spyridon Gkoumas; Julius Hållstedt

3D Heterogenous Integration Packaging of 5G RF Systems using Additive Electronics
WT Alshaibani; Abdullah S. Obeidat; Riadh Al-Haidari; Zhi Dou; SG Lieberman; Shiwantha Gunathilake; Yoga Viswanathan;

Stephen Gonya; Jason Case; Joseph Iannotti; Felippe Pavinatto; Mark D. Poliks

3D Integration of an SRAM chiplet in Fan-Out Embedded Bridge Platform Achieving Low Energy Read/Write
Dany-Sebastien Ly-Gagnon; Li Chen; Dwight Lee; Max Wu; Jiajing Wang; Ping-Chen Liu; Ch Yang; Chung-Ching Peng; Steven Lin; Bruce Xu; Chung Kang Cai

2025 IEEE 24th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)

(May 27–30, 2025)

Compact thermal modeling methodology for HBM
Younghoon Hyun; Seongwoo Yang; Daewoong Lee; Heejin Lee; Kang-Wook Lee

Performance Analysis of Single-Phase Immersion Cooling in high powered electronic components
Ali Heydari; Anto Barigala; Pardeep Shahi; Himanshu Modi; Lochan Sai Reddy Chinthaparthy; Mohammad Raisul Islam; Dereje Agonafer; Mohammad Tradat; Saket Karajgikar; Jeremy Rodriguez

Scaling liquid cooling for Google Data Center AI applications to a 1 GW fleet
Madhusudan Iyengar; Jorge Padilla

G-flow Immersion Cooling Solution for High-power Data Center Servers
Yuehong Fan; Chuanlou Wang; Yang Yao; Yingqiong Bu; Guangying Zhang; Liguang Du; Xiang Que; Luping Zhao; Minghui Xu; Shuisheng Fan; Hongming Xie; Libo Chen; Xinxin Wang; Zhitao Xin; Jiaying Huang; Shanshan Zhang; Feiyang Wu; Xiaohan Sun

Performance Comparison of R1233zd(E) and R515B for Two-Phase Direct-to-Chip Cooling
Qingyang Wang; Akshith Narayanan; Serdar Ozguc; Jacob D. Moore; Richard W. Bonner

2024 IEEE 10th Electronics System-Integration Technology Conference (ESTC)

(September 11–13, 2024)

Bond Strength Measurement for Wafer-Level and Chip-Level Hybrid Bonding
Junya Fuse; Yuki Yoshihara; Marie Sano; Fumihiro Inoue

Overlay Scaling Error Reduction for Hybrid Die-to-Wafer Bonding
Pieter Bex; Mario Gonzalez; Steven Brems; Alain Phommahaxay; Koen D'Havé; Prathamesh Dhakras; Dieter H. Cuypers; Ye Lin; Eric Beyne; Jonathan Abdilla; Kawsar Ahmed Prince; Benedikt Auer; Djuro Bikaljevic; Manuel Deubler; Thiago Moura; Stefan Schmid; Pavel Seroglazov

Simulations of Wafer-to-Wafer Bonding Dynamics and Deformation Mechanisms
Oguzhan Orkut Okudur; Serena Iacovo; Shuo Kang; Mario Gonzalez; Eric Beyne

Fan-Out Packaging Reaching New Heights: Market and Technology Overview
Gabriela Pereira

Signal Integrity Optimization for CoWoS Chiplet Interconnection Design Assisted by Reinforcement Learning
Weiyang Miao; Chuan Seng Tan; Mihai D. Rotaru

2025 IEEE 27th Electronics Packaging Technology Conference (EPTC)

(December 3–6, 2024)

Overview for Overlay Metrology Challenges and Solutions in Advanced Packaging
Roie Volkovich; Nimrod Bar-Yaakov; Yoav Grauer

Advanced Liquid Cooling for 2.5D ICs: Integrated Top Diamond Heat Spreader with Embedded Liquid Channels
Chia-Wei Tseng; Hsin-Cheng Lin; Ho-Ming Tong; C. W. Liu

Surface Activation and Bonding Mechanisms of SiCN and TEOS Dielectrics for Low-Temperature Hybrid Bonding
Liu Chang; Gangli Yang; Yuan Xu; Zhiyu Ma; Keke Tong; Long Cheng; Liyi Li

Cu/SiCN Wafer-to-Wafer Hybrid Bonding Interface Reliability Down to 400 nm Pitch
Emmanuel Chery; Soon-Aik Chew; Théo Bermond; Boyao Zhang; Eric Beyne

2.5D PIC Photonic Interposer Engine for Next Generation Photonic Link CPO of High-Performance Computing and Data Communications
Ting-Ta Chi; Feng Xu; Xiangyu Wang; Zhenyu Li; Wen Lee; Xiao Jun Yuan

Next Generation Advanced Substrate Technologies for Heterogeneous Integration

Jobert van Eisden, *Member, IEEE,* Mohit Khurana, *Member, IEEE,* Venky Sundaram, *Member, IEEE,* Vijay Sukumaran, *Member, IEEE,*

***Abstract*— The burgeoning of high-performance computing (HPC), artificial intelligence (AI), and server applications has resulted in the need for heterogeneous integration (HI) of semiconductor components to meet the desired performance. Disaggregation of chiplets, scaling of interconnects and innovative materials enable HI through advanced packaging solutions. Substrate technology has and continues to evolve, to enable HI and these advanced packaging solutions. This article will focus on the next generation substrate technologies required to be keep up with the industry needs. Initially, the motivation for advancements in substrate packaging enabling HI is discussed. Additionally, different substrate technologies are elaborated, highlighting their key technology attributes and applications. Moreover, the advantages and challenges of each substrate technology are described. Lastly, future scope and emerging areas of innovation are highlighted.**

***Index Terms*— AI, substrate, advanced packaging, heterogeneous integration, glass substrate, ceramics, silicon interposer.**

I. INTRODUCTION

THE advent of HPC, AI, and server compute demand over last decade has driven the need for HI of semiconductor components. Transistor density has not kept up with the compute demand due to the physical limitations. Thus, larger die area is needed to enable a high transistor count [1]. Additionally, disaggregation of these chiplets provides yield resiliency and a multi-modular approach, leading to emergence of 2.5D, 3D and 3.5D advanced packaging architectures [2]. Disaggregation also enables use of discrete functionality chiplets such as memory, I/O and power delivery components which improves the customizability of components [2]. Scaling interconnects is additionally needed to enable high density of high speed I/O (HSIO) channels to keep up with the bandwidth requirements. Lastly, better performing dielectrics, photoresist, cleaning and plating materials are required to scale interconnects and meet the performance required.

Substrates are an essential part of a semiconductor package that bridges the compute chiplets with the system. Substrates play a role in multiple aspects, such as electrically providing routing with required interconnect scaling, mechanically providing reliability to the package, providing a medium for thermal management and lastly enabling heterogenous integration by leveraging disaggregated packaging architectures. Semiconductor packages during 1980s used ceramic substrates due to high thermal stability and mechanical strength, especially for aerospace applications. Multi-layer ceramic substrates with metal lead frame were used for enabling desired electrical routing. However, with scaling of transistors and the need for higher density I/O and bigger substrates, ceramics were not cost effective. Early organic substrates based on bismaleimide triazine (BT) resin enabled lower cost organic substrates and led to the rise of chip scale packaging during 1900s and early 2000s. Surface mount technology enabled the move from wire bonded lead frames to grid arrays: pin grid array (PGA) and ball grid array (BGA) [3]. Additionally, flip chip packaging was developed for direct chip attach on substrate using solder technology. To further scale I/O density, organic substrates with Ajinomoto build-up film (ABF) emerged as the build-up dielectric technology, allowing finer line/space dimensions with lower loss leading to I/O pitches on order of 100s of microns. Disaggregation to multichip packages, 2.5D packaging emerged during 2010s with development of silicon interposer technology, through-silicon via (TSV) and embedded silicon bridge [4]. This era led to development of silicon-based substrates as interposers or bridges, advancing heterogeneous integration and reducing I/O pitch to 10s of microns. With applications in server and high-performance compute needing high bandwidth memory (HBM), 2.5D technology development was critical and led to development of fanout wafer level packaging. Besides I/O density, the packages have enlarged to form factors up to 100 mm x 100 mm and beyond due to need for integration of large chiplets, components and thermal/warpage solutions. To further scale I/O density below 10 microns, 3D packaging has emerged commercially in late 2010s and early 2020s by leveraging hybrid bonding technology [4], [5]. The latest boom in AI has resulted in a need for hardware development to accelerate much faster than the past. Figure 1 shows the compute usage for training AI models which drive the need for fast innovation and commercialization of emerging technologies [6]. Some of the emerging technologies in the current decade involve use of glass-based substrates for enabling very large form factors, thus mitigating warpage driven scaling issues, enabling co-package optics and moving from wafer level packaging to panel level

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packaging.

The objective of this article is to summarize the current substrate technologies to enable HI, along with challenges that may create roadblocks for meeting future requirements to meet the HI roadmap. This article will describe various substrate technologies, based on the material type, processes and applications. The current technologies for each substrate type enabling HI will be elucidated. Subsequently, these substrates are compared for various application vectors, and their current challenges identified. The work needed to ensure substrate technologies can keep up with upcoming packaging needs and drive necessary development is highlighted.

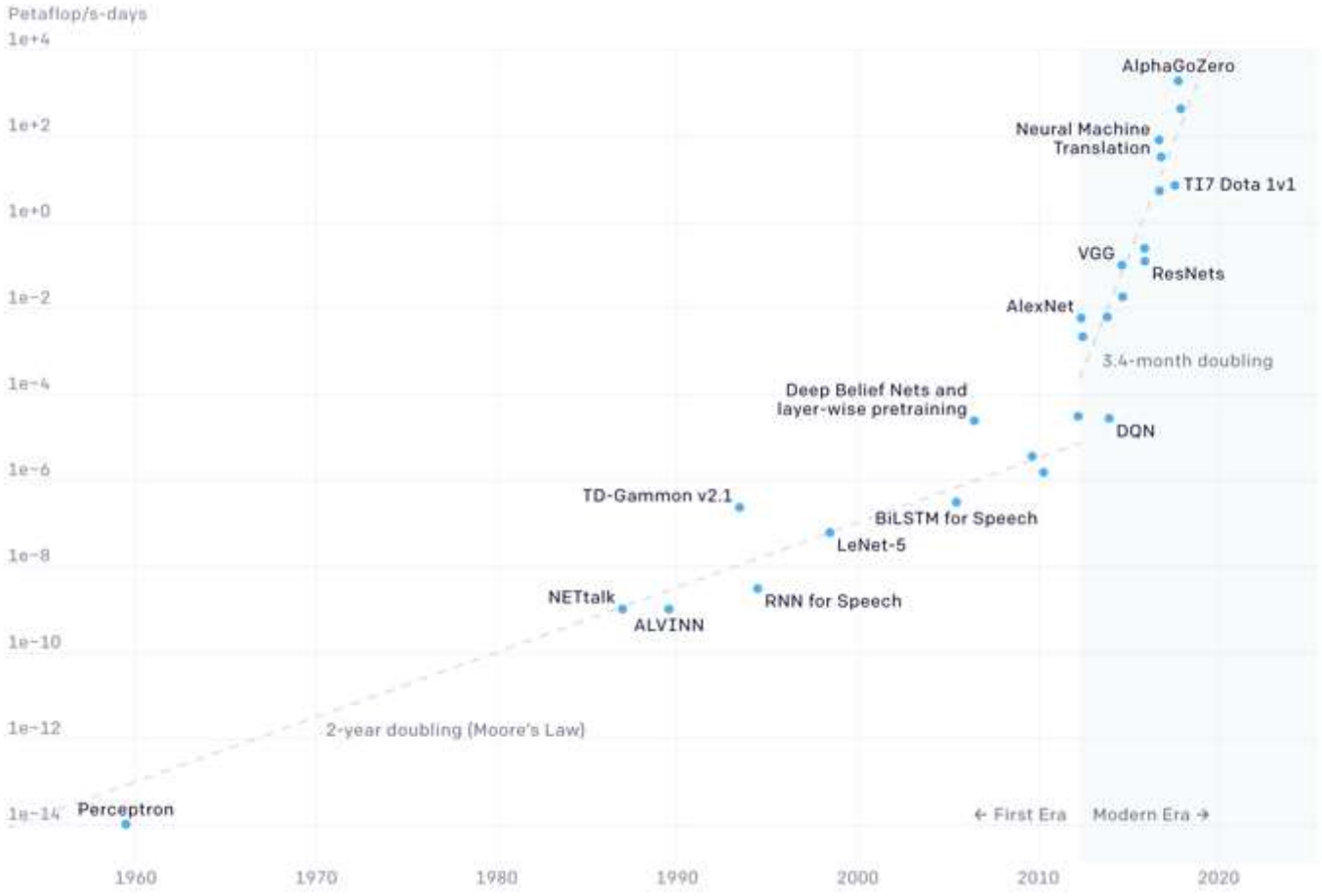

Fig. 1. Rise of compute usage accelerated by AI and HPC applications [6].

II. Type of Substrates Enabling Heterogeneous Integration

A. Ceramic Substrates

The first ceramic substrates used for semiconductor packages were High-Temperature Co-fired Ceramics (HTCC), which offered exceptional hermeticity and mechanical robustness. However, HTCC substrates were limited by the need for refractory metals (like tungsten or molybdenum) compatible with the high co-firing temperatures, and these conductors had poor electrical conductivity.

The critical inflection point for ceramics in high volume packaging occurred with the advent and maturation of Low-Temperature Co-fired Ceramics (LTCC). By lowering the sintering temperature below the melting point of highly conductive metals (such as silver, copper, and gold), LTCC enabled the co-firing of low electrical loss transmission lines. LTCC substrates also integrated high-Q passive components (inductors, capacitors) directly within the substrate. This transition firmly established ceramics as the premier platform for high-frequency RF modules, radar systems, and early-generation mobile communications, leveraging their low dielectric loss and excellent dimensional stability. Concurrently, Direct Bonded Copper (DBC) on alumina (Al_2O_3) and aluminum nitride (AlN) emerged as the standard for power electronics, driven by the need to provide improved heat spreading while providing high-voltage isolation.

LTCC substrates utilize a highly parallel "green tape" fabrication process that allows for the individual inspection and validation of each dielectric layer prior to final lamination and firing, significantly enhancing the yield of high-layer-count (often exceeding 20 layers) packages [7]. The process begins with "green" (unfired) ceramic tape, which is cast from a slurry of ceramic fillers (typically alumina or glass-ceramic composites), organic binders, and plasticizers. The tape is blanked into standard panel sizes and thermally pre-conditioned to stabilize shrinkage. Vertical interconnects or vias are formed by mechanical punching or UV laser drilling through the

individual green sheets [8]. The vias are then filled with a high-conductivity thick-film paste (typically silver, gold, or a silver-palladium alloy). Subsequently, high-precision screen printing or photo-patterning is used to define the horizontal conductive traces, ground planes, and embedded passive components (resistors, inductors, and capacitors) directly onto each individual layer. The individually metallized layers are precisely aligned using optical registration and stacked. The entire assembly is then subjected to isostatic pressing under elevated heat and pressure (e.g., 3000 psi at 70°C) to fuse the individual green sheets into a monolithic block. The laminated stack undergoes a carefully controlled, two-stage thermal profile. First, organic binder burnout occurs at approximately 300°C to 400°C. Second, the temperature is ramped up to the sintering phase at 850°C to 900°C. Because this temperature remains below the melting point of the highly conductive metals, the ceramic and the conductors "co-fire" simultaneously, forming a dense, hermetic, and rigid substrate. After cooling, the monolithic substrate can undergo post-fire metallization (for surface mount pads), singulation, and electrical testing before final die assembly.

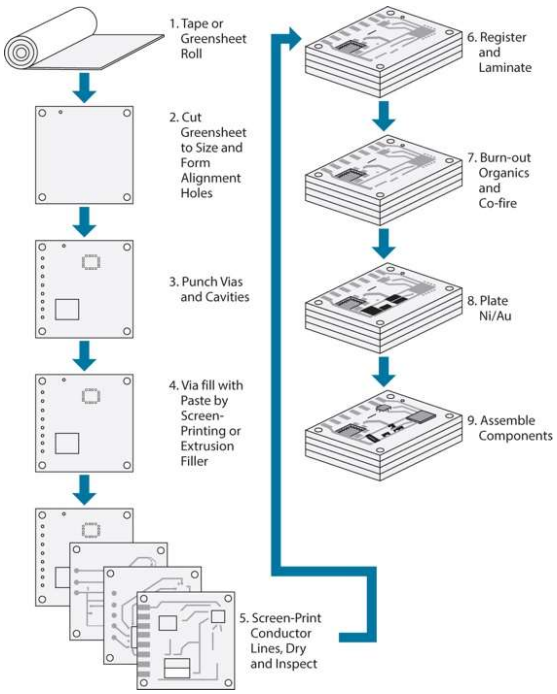

Fig. 2. Typical Process Flow for Low Temperature Co-Fired Ceramic (LTCC) Substrate Fabrication [7]

LTCC substrates are widely used in RF and mm-wave packages, such as 5G front end modules at 28 and 39 GHz bands, automotive radar modules at 77 and 79 GHz bands, and emerging applications in the sub-THz D-band (110 to 170 GHz). At these millimeter-wave frequencies, transmission line losses and parasitic inductances from standard board-level interconnects become prohibitive. This has led to a resurgence of advanced Low-Temperature Co-fired Ceramic (LTCC) and hybrid packaging technologies specifically engineered to enable highly integrated Antenna-in-Package (AiP) architectures [9]. A recent development in LTCC substrates is the fabrication of polyimide copper thin film redistribution layers (RDL) directly on the LTCC substrates to allow for fine pitch chip assembly in heterogenous integration applications. A systematic study presented in 2025 evaluated the direct fabrication of novel non-photosensitive polyimide (non-PSPI) dielectrics on various substrates [10]. The researchers demonstrated that directly building the organic RDL on a highly rigid, low-CTE ceramic substrate reduced warpage by 95% compared to conventional photosensitive polyimides fabricated on standard carriers, and better than the 79% reduction in warpage for the non-PSPI dielectric RDL on silicon carriers.

B. Organic Substrates

Organic substrates comprise of copper clad laminates core made of glass fiber composite, multiple layers of copper and dielectric layers with bumped interface. They can be divided into two categories: the flip-chip ball grid array substrates (FCBGA) and the fan-out redistribution layer (RDL) for high density fan out (HDFO) applications.

FCBGAs have been used for the past couple of decades to power system on chip (SoC) solutions with monolithic silicon. However disaggregated architectures with HSIO channels, larger die sizes and multiple functionalities such as integration of various memory and I/O components into a system in package (SiP) have been leveraged to enable HPC and AI applications. A use case of a typical current and trending GPU package will be utilized to consider the upper bounding requirements for FCBGA substrates. Current GPUs comprises of multiple HBM dies, multiple compute dies and various power delivery components with a cumulative die area on order of 3x or greater reticle size. Increased I/O density demand drives the C4 pitch down below the 100 µm pitch which can either be directly enabled or can be enabled through 2.5D and 3D packaging architectures using silicon or RDL interposers [11]. Similarly, within layer fine line space (L/S) HSIO channels are desired to meet the bandwidth for such packages. The key substrate building block technologies have advanced to accommodate these requirements.

Organic substrates can be divided into following building blocks: substrate core, substrate buildup and substrate bumping. Substrate core provides a method to control the coefficient of thermal expansion (CTE) and consequently the warpage. While SoC's with smaller form factors can manage chip attach and SMT through coreless substrates, GPU applications with larger package sizes need thick cores generally comprising of glass fiber reinforced resin. A lower CTE core with higher modulus is desired to reduce warpage for both SMT and C4 chip attach while maintaining mechanical stability. Use of appropriate filler and glass fiber loading can reduce the core material CTE, while increasing the resin's modulus can further reduce modulus [12]. Substrate buildup comprises of iterations of copper plating, dielectric lamination, via drilling and cleaning, lithography and copper plating with detailed process flow described elsewhere [13]. Some of the critical build up manufacturing features that influence the performance include: line space features within metal layer, via dimensions, metal roughness and dielectric properties. Lithography, metal plating,

cleaning and etching technologies drive line space and via scaling. Most of these processes use wet chemistries which create challenges for scaling down the patterning dimensions and cleanability. However current photoresists, plating etch and cleaning chemistries have enabled 9/12 μm line spaces 40-50 μm via dimensions, which meet the existing performance requirements [14]. The copper roughness and dielectric material properties affect the insertion loss and thus the latency. Downside of reducing copper roughness is the poor adhesion to the dielectric leading to reliability issues [15]. Similarly, dielectrics such as ABF have evolved to enable low loss without compromising on the adhesion and reliability. Lastly, bump creation for C4 has moved from a screen-printed solder technology to electroplating to enable pitches in lower 100 μm range. As we move towards 100 μm and lower pitches, thermocompression bonding enables high yielding joints with desired reliability. Additionally, embedded multi-die interconnect bridge (EMIB) comprises of multi pitch regions, which require additional considerations and tighter controls for high yielding chip attach [16].

HDFO packages are comprised of disaggregated chiplets fanned out through RDLs. Current process involves wafer level packaging with basic building blocks comprising of die placement, mold and planarization, fan out through RDL and bumping [17], [18]. The order of these process steps depends on choice between chip first or RDL first process. These are currently commercialized through wafer level temporary carrier flow. The carriers are silicon or glass based, with better warpage control than organic substrates, thus enabling finer L/S up to 2/2 μm and via dimensions around 20-30 μm. The bump pitch between the chiplets can scale down to 40-50 μm [14]. Compared to organic FCBGA substrates, RDLs require precise patterning and plating, and leverage the liquid photoresists and dry deposition and etch techniques.

Pure organic substrate or organic RDLs limit the critical dimensions to be scaled down and thus limits the I/O density. Moving to pure silicon substrates resolves the warpage and CTE driven limitations but increases the cost and limits total die area (critical to integrate many memory and compute dies based on performance requirements) due to yield limitations. Thus, silicon bridges in either FCBGA substrates or HDFO interposers enable a higher I/O density between chiplets with lower cost than silicon interposers. The embedded silicon is typically small in dimensions which additionally improves the yield resiliency. Smaller L/S dimensions <1 μm have been demonstrated with vias < 2 μm [16], [19]. EMIB comprises of a bridge embedded in the FCBGA substrate with additional steps during panel level substrate manufacturing to embed and encapsulate the die, and fan out the bumps on C4 with a finer pitch than rest of the C4 region [14]. Embedded HDFO substrates require initial copper pillar formation, die bond, encapsulation with mold and fanout of RDLs [20].

C. Silicon Interposers and Substrates

Silicon Interposers: Silicon interposers were introduced in 2011 when Xilinx introduced a "die-splitting" methodology to partition large, low-yield Field Programmable Gate Arrays (FPGAs) into multiple high-yield functional tiles [21]. These tiles were reconnected using back-end-of-line (BEOL) copper wiring patterned onto a thin silicon interposer, using Through-Silicon Vias (TSVs) for vertical connections between the ICs and the package substrate [21]. Silicon interposers were subsequently adopted by AMD to integrate high-bandwidth memory (HBM) to graphics processing unit (GPU), leading to widespread use of silicon interposers for multi-die heterogenous integration and chiplet-based architectures [22]. Today, TSMC's CoWoS-S (Chip-on-Wafer-on-Substrate with Silicon Interposer) has been scaled to high-volume manufacturing (HVM) in 2.5D and 3D integration and is also available from a number of other foundries [23]. Silicon interposers can be fabricated as a passive silicon substrate optimized for high-density multi-die routing and interconnect pitch translation. An active interposer platform that embeds functional complementary metal-oxide-semiconductor (CMOS) logic, power distribution, or test circuitry directly within the underlying silicon interposer has been developed by Intel and others [24].

Double-Sided Silicon-Cored Substrates: Silicon core substrates have been explored and demonstrated in both wafer and panel formats with double sided RDL or build-up layers [25]. The first demonstrations utilized a polycrystalline silicon wafer or panel borrowed from the solar cell supply chain ecosystem, with laser ablated or plasma etched through silicon vias with polymer or oxide liners, polymer build-up layers and semi-additive processes for copper wiring [25]. More recent developments have focused on scaling the wiring pitch using both wafer and panel process methods [26]. Large silicon panels have recently been introduced as a manufacturing ready core material by Mitsubishi Materials, Japan.

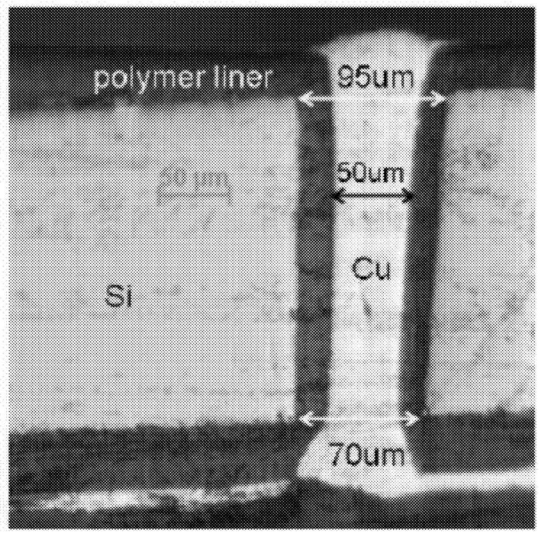

Fig. 3. Double sided Build-up Layers and polymer lined TSVs in Polycrystalline Silicon Core Substrates [25]

The major benefit of silicon interposers and silicon core substrates is the Coefficient of Thermal Expansion (CTE)

match to silicon chips, suppressing global thermo-mechanical warpage [25]. The redistribution layers (RDL) on silicon substrates can be fabricated using one of two methods, (a) copper-polymer RDLs that provide compliant, low-stress routing paths for medium-density lines and power delivery networks, and (b) Cu-SiO_2 inorganic RDLs that enable aggressive sub-micron line/space scaling via standard damascene processes to maximize parallel die-to-die interconnections.

D. Glass Substrates

Glass-based substrates can be divided into two categories, namely 1) glass core substrates, and 2) glass interposers. Both glass core substrates and glass interposers take advantage of the unique properties that glass has to offer as structural material for advanced packaging applications. For glass core substrates, the typical glass core thickness ranges from 600 µm up to 1 mm, whereas the glass interposer thickness range is typically 100 – 300 µm.

Glass core substrates are in principle an advanced version of the organic glass fiber and resin core FCBGA substrates that are described in section II B). Glass and organic core substrates share a very similar build up structure manufactured typically with a Semi-Additive Process (SAP) on laminated dielectrics such as glass filled resins (e.g. ABF), photosensitive dielectrics, or a combination thereof. In general, a glass core offers several advantages over the glass fiber / resin core: 1) a higher Young's modulus of glass allows larger packages with reduced warping at the same core thickness, 2) the CTE of glass can be altered through its composition. On the lower end of CTE, it is possible for the glass CTE to match silicon, on the higher end values much closer to metals and organics have been reported [27]. This allows further reduction of CTE impact on overall package warping and enables reliability improvements for large form factor packages. 3) Since glass is a homogeneous material, any thermal cycling as a result of, for example, ABF curing does not affect overall size integrity and pattern shift which impact overlay performance. Unlike organic core materials, glass will return to its original dimensions at room temperature which facilitates accurate patterning and via formation in the subsequent build up steps. This allows feature size scaling beyond the capability of organic core-based substrates. [28]. 4) Developments in Through Glass Via (TGV) formation have shown an excellent capability of the glass-based core to support a higher vertical I/O density as compared to Through Holes (TH) formed in organic core-based substrates. State of the art TGV formation is done with for example LPKF's Laser-Induced Deep Etching (LIDE) process where a laser is used to alter the glass structure locally to enhance its etching rate in hydrofluoric (HF) or metal / organic hydroxide-based solutions. This allows a finer pitch and a higher aspect ratio for TGVs [29, 30] as compared to mechanically drilled THs in organic cores, where the pitch is limited to drill bit size (approx. 100 µm minimum). In addition, the excellent dielectric properties of glass ensure a better electrical performance in particular for high frequency signal I/O [31, 32].

Glass interposers were initially proposed as an alternative for silicon interposer, for example in high frequency applications due to the excellent dielectric characteristics of glass compared to silicon. The main distinction between glass interposer and glass core substrate stems from functionality; glass interposers are a means of high density die-to-die I/O and pitch translation from dies to in most cases a standard organic core FCBGA substrate as opposed to glass core technology which represents the advancement of FCBGA substrate. Glass interposers typically are thinner than organic core glass, and are often manufactured on wafer scale using a carrier to handle thin glass [33]. Wafer level packaging processes and processing techniques common to silicon interposer can be used, which allows high yield, fine features to be manufactured typically beyond the capability of glass core based FCBGA substrates.

III. Comparison and Challenges of Substrate Types

A. Comparison of substrate types

In the previous sections, several types of substrates were discussed. Depending on the final intended application it makes sense to prefer one substrate type over another. Typically, this decision is driven by a consideration of capability (can it support high end application architectures through meeting required I/O densities) cost, and how well can it control large package warpage. Especially for the current and future packaging needs for AI-related chipset, large form-factor, high performance packages need to withstand CTE-driven package warpage as the silicon content is increasing dramatically. Table I summarizes the relative performance of the previously discussed substrate types against these criteria; and subsequent sections will discuss the challenges these substrate types may face for advanced substrate applications more in-depth.

TABLE I
COMPARISON OF SUBSTRATE TYPES

Property	Ceramic	Organic	Silicon	Glass
Cost	+	++	- -	-
Die Area	-	+/-	- -	++
IO Density	-	+	+++	++
Warpage	+++	+/-	+++	+++

B. Challenges for different substrate types

Various challenges for each substrate type are summarized in this section.

1) **Ceramic Substrates:** As micro-bump pitches scale below 10µm and redistribution layer (RDL) line/space (L/S) resolutions scale below 2µm to support chiplet integration, several fundamental materials and process challenges must be overcome.
   a) **Surface Roughness:** The most immediate barrier to integrating ultra-fine pitch RDLs directly onto LTCC or standard ceramic substrates is the inherent surface roughness (R_a) resulting from the sintering process.

Traditional thick-film screen printing used in LTCC is fundamentally limited to line widths of approximately 30-50µm. Transitioning to thin-film, semi-additive processes (SAP) or dual-damascene copper plating requires a nearly planar surface to prevent lithographic scattering and ensure precise photoresist adhesion. Current research is focused on chemical-mechanical planarization (CMP) of ceramics and the application of ultra-thin, low-loss planarization polymers prior to RDL fabrication.

b) **Localized Stress:** Although a high-stiffness, low-CTE ceramic substrate eliminates the global package warpage that plagues organic substrates and interposers, this mechanical rigidity can cause localized thermo-mechanical stresses on micro bumps. Such localized shear stresses concentrate at the bump interfaces, significantly increasing the risk of fatigue, crack propagation, and bump shear. Underfill materials used for chiplet assembly on ceramic substrates need to be engineered to accommodate these localized stress concentration effects.

c) **Panel size limitations:** Ceramic substrates use 150 mm and 200 mm square panels, with some leading manufacturers able to fabricate 300mm square panels. The panel size limitations of LTCC substrates are mainly due to the high shrinkage during the co-firing process. Green tape material improvements and "zero-shrink" manufacturing process innovations have reduced the shrinkage effects significantly in the last few decades; however, ceramic substrates face challenges in scaling to larger panel sizes to enable package sizes larger than 80-100mm.

2) **Organic Substrates:** The FCBGAs and HDFOs have evolved to accommodate multichip packages, however face challenges as pitch scales down, package area increases, and thermal design power increases:

a) **Substrate coplanarity:** Increased die complexity and larger packages suffer from large warpage and can reduce chip attach and SMT yield. For FCxGAs, the substrate core is modified with lower CTE or increased thickness to meet warpage targets. For HDFOs, the glass carrier, mold, and RDL stackup influence the warpage. Besides the chip attach and SMT, the warpage also limits the patterning yields, particularly at the panel level.

b) **Patterning smaller features:** Typical panel level substrates use dry film photoresists which work well for existing feature sizes. However finer L/S features would need development of higher performing thinner resists. Heterogenous integration roadmap trends towards 5/5 µm L/S on panel level FCBGAs [14]. Additionally, HDFOs will trend towards a sub 1/1 µm L/S which would require development of higher performing wafer level resists, which can accommodate higher aspect ratios [14], [19]. Development of polymer damascene provides additional scalability with these high aspect ratio features beyond the semi additive patterning used for RDLs [17]. Besides lithography, FCBGAs use panel level laser via drilling and wet cleaning. Scaling these to 30 µm and below on the panel level requires process optimizations to ensure no residue remains before plating. Lastly, feature sizes reduction combined with layer counts increase, have resulted in the need for high aspect feature plating. Development of plating process and chemistries enabling complete fill of the features is required, with desired throughput and uniform plating across the panel and wafers.

c) **HSIO requirements:** Development of newer low loss ABF has driven HSIO enablement which continues to be driven through the growing demand for low latency and higher bandwidth. As feature sizes reduce, copper roughness results in higher loss and needs to be reduced. This requires optimization of copper and dielectric adhesion to ensure good reliability. With increased layer counts and larger package areas, the stress could additionally impact reliability and interfacial adhesion is critical.

d) **Bump pitch scaling**: Bump pitch for FCBGAs are trending to sub 100 µm pitches, which requires use of panel level electroplating instead of the screen-printed solder ball technology. Furthermore, the plated bump coplanarity will be critical to ensure high yielding chip attach processes. As the package area increases, bumping will require tighter coplanarity control further increasing the manufacturing challenges.

e) **Power delivery:** As the Thermal Design Power (TDP) keeps increasing with AI and HPC workload beyond 1kW on package level, an efficient power delivery network is desired. Increased routing layers and lengths result in poor power integrity and requires simplified design and architecture which can reduce routing length and improve power efficiency. Additionally, capacitors and components can be strategically placed to enable improved power integrity.

3) **Silicon Interposers:**

Most of the technical challenges for wafer-based silicon interposers have been addressed since the technology was introduced. Silicon interposers mainly faced cost challenges in scaling to very high-volume production due to the high cost of wafer fab processes and limited number of large body size interposers from 300mm wafers.

Silicon core substrates and silicon interposers both face challenges in CTE mismatch to the organic substrates or PWBs on which they are assembled, especially for large body sizes.

4) **Glass Substrates:**

As glass-based interposer and advanced FCBGA technology continue to be developed, many challenges remain. At present glass interposer is a more mature technology than glass core FCBGA substrates, mostly due to the ability to re-use IP-blocks from silicon wafer process technology. For glass core substrate technology

many of the challenges stem from needing to fabricate in panel format as well as a much greater thickness of the glass:

a) **Processing tool availability:** The processing tool landscape is, as of today, not well developed. It remains difficult to handle large format glass panels due to the inherent brittleness of this material. In addition, development of capable tool sets has only been a focus for tool vendors since approximately 2023, when Intel revealed their glass core substrate technology [34]. Handling of thin glass cores, and also in particular dicing, has proven to be difficult, although some progress was made by Disco recently on the latter topic [35].

b) **Adhesion layer and seed for high Aspect Ratio TGV:** Metallization of high-aspect ratio through holes remains a challenge. Physical Vapor Deposition (PVD) has been evaluated and, to some extent, accepted as a means to deposit an adhesion layer and copper seed on panel surface and TGV sidewalls for aspect ratios up to approximately 6-8:1. For higher aspect ratios, PVD is less suitable; it is a line-of-sight deposition method which is generally unable to provide adequate step coverage for higher aspect ratios [36, 37]. In addition, glass core metallization requires a two-sided deposition, which further complicates PVD tool sets and impacts throughput. Development of finer pitch and higher aspect ratio TGV has brought focus on wet deposition techniques for adhesion layer and seed due to a better handling of aspect ratios above 8:1, its ability to process both sides of a panel in one step, superior conformality for high aspect ratio TGV over PVD, and capability to process multiple panels at once. Several chemistry suppliers are working on a metal-oxide based adhesion layer, which in all cases requires a high temperature activation step to ensure adhesion strength [37, 38, 39]. This is to be seeded with an electroless copper process to prepare for subsequent TGV filling.

c) **Copper filling of high aspect ratio TGV:** Wafer-based processes such as Through Silicon Via (TSV) can provide a void and inclusion-free fill for aspect ratios well above 10:1, suited well for glass interposer technology when TGVs similar in dimension to TSV can be used. TSV Cu fill rates are in general too low to be practical, and impose a major penalty on cost for the much larger TGVs typically envisioned for glass-core FCBGA substrates. Several substrate core and plating chemistry suppliers are looking to enhance filling performance through use of pulse and reverse-pulse plating techniques, already well known from organic core substrate [37, 40, 41]. Even though there is some promise in these methods, high aspect ratios and large volumes are still difficult to fill. Other plating techniques focus on filling TGVs with a single sided electrical contact and using the glass as a template for pattern fill; a technique known in tall pillar plating, or more commonly a conformal plating technique in which the copper plated sidewall grows together in order to avoid a seam. [41]. Until a reliable and cost-effective solution for high aspect ratio TGV fill is available, conformal plating and paste fill techniques such as used in organic core FCBGA substrate and High Layer Count Multi-Layer Boards (HLC-MLB) are to be considered.

d) **Reliability:** Although several reports were made on component level thermal cycle stability of filled through glass vias, as of today there is no complete picture on overall board and system level reliability of glass core-based substrates as compared to organic core FCBGA substrates. A large set of parameters such as glass type, CTE, LIDE TGV quality, pattern density and design has yet to be explored completely to form an accurate picture of the final performance and the usable application space of this technology.

IV. Emerging Technologies Future Scope

Next generation technology inflections will be enabled by advanced substrates having following attributes; a) lowest signal loss (be it electrical or optical); b) highest I/O density with lowest signal/thermal cross-talk; c) excellent thermal dissipation; d) show high thermomechanical reliability at large area form-factors to enable integration of multiple dies, thus adding more functionality on the substrate.

The following emerging technologies will be enabled by next generation packages using advanced substrate technology for heterogeneous integration:

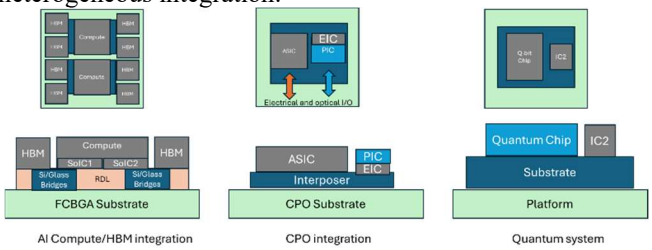

Fig. 4. Emerging subsystems needing advanced package substrates

1) AI GPU/HBM:

Building blocks of AI comprise of multiple compute and memory ICs attached first to an interposer and subsequently to an organic BGA substrate. Next generation GPUs for example, will have 2 or more GPU dies surrounded by 8 or more HBM stacked-memory dies, all integrated on a RDL interposer with silicon/glass bridges, providing high bandwidth (BW) interconnection between GPUs and memory. Further, silicon bridge technology have evolved from simple planar fine-pitch wiring levels to addition of TSVs, providing improved design flexibility for HI modules [42]. As we integrate more compute and memory chips on an interposer, the substrate onto which interposer is attached to need to have exceptional rigidity, low warpage during assembly and support small pitch I/O. The transition from organic to glass-based substrates will enable package size scaling with improved functionality [43].

Additionally, HPC and AI accelerator subsystems comprise of compute modules with hybrid bonded chip-lets integrated on a silicon interposer [44]. 3D stacking of chip-lets increase functional density, however, there is a need to effectively remove heat from 3D stacked dies. The primary heat removal pathway is away from the substrate, achieved using advanced thermal interface materials and heat sinks, through a combination of conduction, convection mechanisms. Substrates with higher thermal conductivity such as SiC have gathered active interest in industry and academia alike [45]. Future systems can be envisioned having cooling pathways both through heat sinks and advanced substrates to mitigate local thermal hotspots, thus improving overall device performance.

2) Co-Packaged Optics:

As compute and data transfer speeds increase, optical interconnects are needed to meet the growing BW demand. This requires conversion of signals between electrical and optical domains. A pluggable optical transceiver is one such module that can be attached to a package substrate to enable this signal conversion. Future systems however need lower latency, and hence there is a drive to co-locate optical components on the same package as compute/control electronic dies. This will require substrates that support very low electrical signal loss routing, and have integrated optical waveguides [46]. Interfaces between fiber and waveguides, adhesives, passive alignment strategy are key considerations for a reliable opto-electronic module.

3) Quantum Computing:

Quantum computing has been a topic of active research and development over the past few years. Unlike traditional computing that operates on binary (1s and 0s), Q-bits or quantum bits assume states between a 1 and 0, based on quantum mechanics. Manipulation of such Q-bits may in the future help solve complex problems that are not possible with traditional computers. At the heart of such systems is a quantum chip or quantum processor, that can be broadly classified into two categories: a) matter based (ions) and b) light based (photonic). Such quantum chips need to be packaged on a substrate providing reliable and efficient interconnection between chip and external world.
Such substrates need to demonstrate; a) low loss to ensure Q-bit fidelity that includes low loss waveguides on chip and on substrates, and low electrical loss interconnects on substrates for high signal and power integrity. Several of these quantum chips operate at deep cryogenic temperatures (below 4K); necessitating substrates that are reliable at extremely low temperatures. While the industry works on building the fundamental Q-bit chip, package substrates will play a pivotal role in enabling efficient scaling of quantum processors. The properties of advanced organic, silicon and glass substrates explained in the earlier sections can be leveraged to integrate a new generation of compute systems in the next decade.

V. Conclusion

As artificial intelligence and high-performance computing drive the needs for larger, more capable and reliable substrates, several technologies are emerging as enabling substrate platforms for large and complex heterogeneously integrated chipsets. Existing technologies such as organic core build-up laminate are undergoing continuous evolution to meet the ever-increasing demands associated with continued performance scaling, but may in the end not meet the most stringent demands that are required for future packages. More recently, this trend has renewed interest in ceramic substrates due to their excellent mechanical stability, high-frequency dielectric properties and reliability performance. As silicon has been the material of choice for interposer technology for some time, this mature platform offers excellent I/O density and mechanical stability. However, scaling to large chip aggregates is not cost effective at this moment due to the limited scalability of substrate size and associated processing equipment. Novel technologies based on glass as a build-up substrate core or interposer material have gained much traction over the past year. Glass is an attractive material which enables large, mechanically stable, high I/O density and high-frequency compatible packages, which allow extended performance scaling well beyond organic core build-up substrate and silicon interposer. This will enable the next generations of packages for AI, Co-packaged optics and eventually quantum computing applications.

References and Footnotes

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