Next Generation Advanced Substrate Technologies for Heterogeneous Integration

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***Abstract*— The burgeoning of high-performance computing (HPC), artificial intelligence (AI), and server applications has resulted in the need for heterogeneous integration (HI) of semiconductor components to meet the desired performance. Disaggregation of chiplets, scaling of interconnects and innovative materials enable HI through advanced packaging solutions. Substrate technology has and continues to evolve, to enable HI and these advanced packaging solutions. This article will focus on the next generation substrate technologies required to be keep up with the industry needs. Initially, the motivation for advancements in substrate packaging enabling HI is discussed. Additionally, different substrate technologies are elaborated, highlighting their key technology attributes and applications. Moreover, the advantages and challenges of each substrate technology are described. Lastly, future scope and emerging areas of innovation are highlighted.**

***Index Terms*— AI, substrate, advanced packaging, heterogeneous integration, glass substrate, ceramics, silicon interposer.**

I. INTRODUCTION

THE advent of HPC, AI, and server compute demand over last decade has driven the need for HI of semiconductor components. Transistor density has not kept up with the compute demand due to the physical limitations. Thus, larger die area is needed to enable a high transistor count [1]. Additionally, disaggregation of these chiplets provides yield resiliency and a multi-modular approach, leading to emergence of 2.5D, 3D and 3.5D advanced packaging architectures [2]. Disaggregation also enables use of discrete functionality chiplets such as memory, I/O and power delivery components which improves the customizability of components [2]. Scaling interconnects is additionally needed to enable high density of high speed I/O (HSIO) channels to keep up with the bandwidth requirements. Lastly, better performing dielectrics, photoresist, cleaning and plating materials are required to scale interconnects and meet the performance required.

Substrates are an essential part of a semiconductor package that bridges the compute chiplets with the system. Substrates play a role in multiple aspects, such as electrically providing routing with required interconnect scaling, mechanically providing reliability to the package, providing a medium for thermal management and lastly enabling heterogenous integration by leveraging disaggregated packaging architectures. Semiconductor packages during 1980s used ceramic substrates due to high thermal stability and mechanical strength, especially for aerospace applications. Multi-layer ceramic substrates with metal lead frame were used for enabling desired electrical routing. However, with scaling of transistors and the need for higher density I/O and bigger substrates, ceramics were not cost effective. Early organic substrates based on bismaleimide triazine (BT) resin enabled lower cost organic substrates and led to the rise of chip scale packaging during 1900s and early 2000s. Surface mount technology enabled the move from wire bonded lead frames to grid arrays: pin grid array (PGA) and ball grid array (BGA) [3]. Additionally, flip chip packaging was developed for direct chip attach on substrate using solder technology. To further scale I/O density, organic substrates with Ajinomoto build-up film (ABF) emerged as the build-up dielectric technology, allowing finer line/space dimensions with lower loss leading to I/O pitches on order of 100s of microns. Disaggregation to multichip packages, 2.5D packaging emerged during 2010s with development of silicon interposer technology, through-silicon via (TSV) and embedded silicon bridge [4]. This era led to development of silicon-based substrates as interposers or bridges, advancing heterogeneous integration and reducing I/O pitch to 10s of microns. With applications in server and high-performance compute needing high bandwidth memory (HBM), 2.5D technology development was critical and led to development of fanout wafer level packaging. Besides I/O density, the packages have enlarged to form factors up to 100 mm x 100 mm and beyond due to need for integration of large chiplets, components and thermal/warpage solutions. To further scale I/O density below 10 microns, 3D packaging has emerged commercially in late 2010s and early 2020s by leveraging hybrid bonding technology [4], [5]. The latest boom in AI has resulted in a need for hardware development to accelerate much faster than the past. Figure 1 shows the compute usage for training AI models which drive the need for fast innovation and commercialization of emerging technologies [6]. Some of the emerging technologies in the current decade involve use of glass-based substrates for enabling very large form factors, thus mitigating warpage driven scaling issues, enabling co-package optics and moving from wafer level packaging to panel level

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packaging.

The objective of this article is to summarize the current substrate technologies to enable HI, along with challenges that may create roadblocks for meeting future requirements to meet the HI roadmap. This article will describe various substrate technologies, based on the material type, processes and applications. The current technologies for each substrate type enabling HI will be elucidated. Subsequently, these substrates are compared for various application vectors, and their current challenges identified. The work needed to ensure substrate technologies can keep up with upcoming packaging needs and drive necessary development is highlighted.

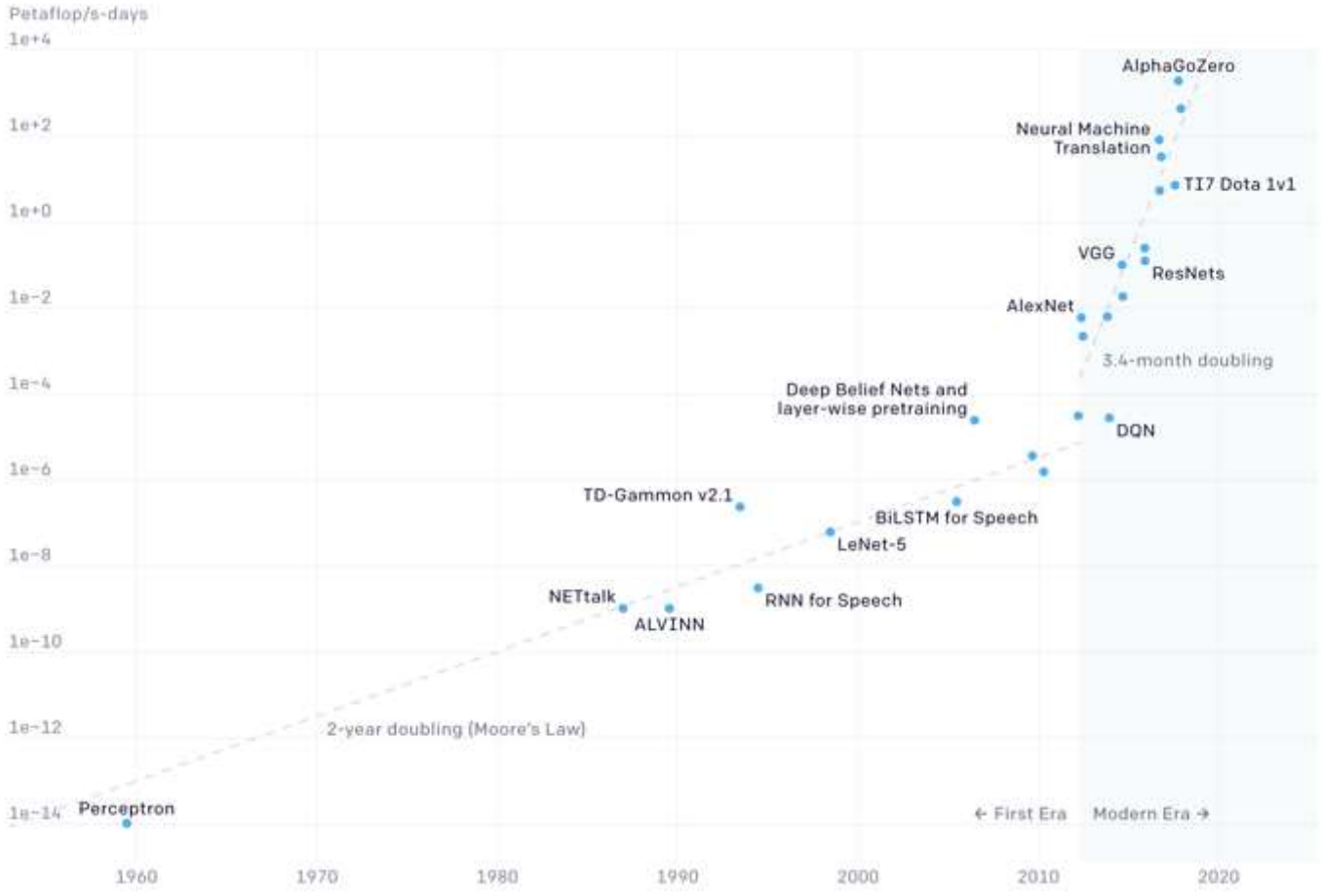

Fig. 1. Rise of compute usage accelerated by AI and HPC applications [6].

II. Type of Substrates Enabling Heterogeneous Integration

A. Ceramic Substrates

The first ceramic substrates used for semiconductor packages were High-Temperature Co-fired Ceramics (HTCC), which offered exceptional hermeticity and mechanical robustness. However, HTCC substrates were limited by the need for refractory metals (like tungsten or molybdenum) compatible with the high co-firing temperatures, and these conductors had poor electrical conductivity.

The critical inflection point for ceramics in high volume packaging occurred with the advent and maturation of Low-Temperature Co-fired Ceramics (LTCC). By lowering the sintering temperature below the melting point of highly conductive metals (such as silver, copper, and gold), LTCC enabled the co-firing of low electrical loss transmission lines. LTCC substrates also integrated high-Q passive components (inductors, capacitors) directly within the substrate. This transition firmly established ceramics as the premier platform for high-frequency RF modules, radar systems, and early-generation mobile communications, leveraging their low dielectric loss and excellent dimensional stability. Concurrently, Direct Bonded Copper (DBC) on alumina (Al_2O_3) and aluminum nitride (AlN) emerged as the standard for power electronics, driven by the need to provide improved heat spreading while providing high-voltage isolation.

LTCC substrates utilize a highly parallel "green tape" fabrication process that allows for the individual inspection and validation of each dielectric layer prior to final lamination and firing, significantly enhancing the yield of high-layer-count (often exceeding 20 layers) packages [7]. The process begins with "green" (unfired) ceramic tape, which is cast from a slurry of ceramic fillers (typically alumina or glass-ceramic composites), organic binders, and plasticizers. The tape is blanked into standard panel sizes and thermally pre-conditioned to stabilize shrinkage. Vertical interconnects or vias are formed by mechanical punching or UV laser drilling through the

individual green sheets [8]. The vias are then filled with a high-conductivity thick-film paste (typically silver, gold, or a silver-palladium alloy). Subsequently, high-precision screen printing or photo-patterning is used to define the horizontal conductive traces, ground planes, and embedded passive components (resistors, inductors, and capacitors) directly onto each individual layer. The individually metallized layers are precisely aligned using optical registration and stacked. The entire assembly is then subjected to isostatic pressing under elevated heat and pressure (e.g., 3000 psi at 70°C) to fuse the individual green sheets into a monolithic block. The laminated stack undergoes a carefully controlled, two-stage thermal profile. First, organic binder burnout occurs at approximately 300°C to 400°C. Second, the temperature is ramped up to the sintering phase at 850°C to 900°C. Because this temperature remains below the melting point of the highly conductive metals, the ceramic and the conductors "co-fire" simultaneously, forming a dense, hermetic, and rigid substrate. After cooling, the monolithic substrate can undergo post-fire metallization (for surface mount pads), singulation, and electrical testing before final die assembly.

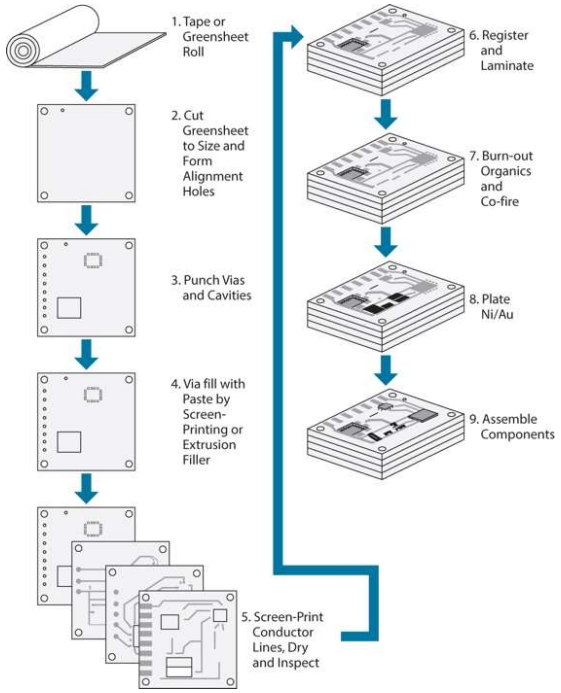

Fig. 2. Typical Process Flow for Low Temperature Co-Fired Ceramic (LTCC) Substrate Fabrication [7]

LTCC substrates are widely used in RF and mm-wave packages, such as 5G front end modules at 28 and 39 GHz bands, automotive radar modules at 77 and 79 GHz bands, and emerging applications in the sub-THz D-band (110 to 170 GHz). At these millimeter-wave frequencies, transmission line losses and parasitic inductances from standard board-level interconnects become prohibitive. This has led to a resurgence of advanced Low-Temperature Co-fired Ceramic (LTCC) and hybrid packaging technologies specifically engineered to enable highly integrated Antenna-in-Package (AiP) architectures [9]. A recent development in LTCC substrates is the fabrication of polyimide copper thin film redistribution layers (RDL) directly on the LTCC substrates to allow for fine pitch chip assembly in heterogenous integration applications. A systematic study presented in 2025 evaluated the direct fabrication of novel non-photosensitive polyimide (non-PSPI) dielectrics on various substrates [10]. The researchers demonstrated that directly building the organic RDL on a highly rigid, low-CTE ceramic substrate reduced warpage by 95% compared to conventional photosensitive polyimides fabricated on standard carriers, and better than the 79% reduction in warpage for the non-PSPI dielectric RDL on silicon carriers.

B. Organic Substrates

Organic substrates comprise of copper clad laminates core made of glass fiber composite, multiple layers of copper and dielectric layers with bumped interface. They can be divided into two categories: the flip-chip ball grid array substrates (FCBGA) and the fan-out redistribution layer (RDL) for high density fan out (HDFO) applications.

FCBGAs have been used for the past couple of decades to power system on chip (SoC) solutions with monolithic silicon. However disaggregated architectures with HSIO channels, larger die sizes and multiple functionalities such as integration of various memory and I/O components into a system in package (SiP) have been leveraged to enable HPC and AI applications. A use case of a typical current and trending GPU package will be utilized to consider the upper bounding requirements for FCBGA substrates. Current GPUs comprises of multiple HBM dies, multiple compute dies and various power delivery components with a cumulative die area on order of 3x or greater reticle size. Increased I/O density demand drives the C4 pitch down below the 100 μm pitch which can either be directly enabled or can be enabled through 2.5D and 3D packaging architectures using silicon or RDL interposers [11]. Similarly, within layer fine line space (L/S) HSIO channels are desired to meet the bandwidth for such packages. The key substrate building block technologies have advanced to accommodate these requirements.

Organic substrates can be divided into following building blocks: substrate core, substrate buildup and substrate bumping. Substrate core provides a method to control the coefficient of thermal expansion (CTE) and consequently the warpage. While SoC's with smaller form factors can manage chip attach and SMT through coreless substrates, GPU applications with larger package sizes need thick cores generally comprising of glass fiber reinforced resin. A lower CTE core with higher modulus is desired to reduce warpage for both SMT and C4 chip attach while maintaining mechanical stability. Use of appropriate filler and glass fiber loading can reduce the core material CTE, while increasing the resin's modulus can further reduce modulus [12]. Substrate buildup comprises of iterations of copper plating, dielectric lamination, via drilling and cleaning, lithography and copper plating with detailed process flow described elsewhere [13]. Some of the critical build up manufacturing features that influence the performance include: line space features within metal layer, via dimensions, metal roughness and dielectric properties. Lithography, metal plating,

cleaning and etching technologies drive line space and via scaling. Most of these processes use wet chemistries which create challenges for scaling down the patterning dimensions and cleanability. However current photoresists, plating etch and cleaning chemistries have enabled 9/12 μm line spaces 40-50 μm via dimensions, which meet the existing performance requirements [14]. The copper roughness and dielectric material properties affect the insertion loss and thus the latency. Downside of reducing copper roughness is the poor adhesion to the dielectric leading to reliability issues [15]. Similarly, dielectrics such as ABF have evolved to enable low loss without compromising on the adhesion and reliability. Lastly, bump creation for C4 has moved from a screen-printed solder technology to electroplating to enable pitches in lower 100 μm range. As we move towards 100 μm and lower pitches, thermocompression bonding enables high yielding joints with desired reliability. Additionally, embedded multi-die interconnect bridge (EMIB) comprises of multi pitch regions, which require additional considerations and tighter controls for high yielding chip attach [16].

HDFO packages are comprised of disaggregated chiplets fanned out through RDLs. Current process involves wafer level packaging with basic building blocks comprising of die placement, mold and planarization, fan out through RDL and bumping [17], [18]. The order of these process steps depends on choice between chip first or RDL first process. These are currently commercialized through wafer level temporary carrier flow. The carriers are silicon or glass based, with better warpage control than organic substrates, thus enabling finer L/S up to 2/2 μm and via dimensions around 20-30 μm. The bump pitch between the chiplets can scale down to 40-50 μm [14]. Compared to organic FCBGA substrates, RDLs require precise patterning and plating, and leverage the liquid photoresists and dry deposition and etch techniques.

Pure organic substrate or organic RDLs limit the critical dimensions to be scaled down and thus limits the I/O density. Moving to pure silicon substrates resolves the warpage and CTE driven limitations but increases the cost and limits total die area (critical to integrate many memory and compute dies based on performance requirements) due to yield limitations. Thus, silicon bridges in either FCBGA substrates or HDFO interposers enable a higher I/O density between chiplets with lower cost than silicon interposers. The embedded silicon is typically small in dimensions which additionally improves the yield resiliency. Smaller L/S dimensions <1 μm have been demonstrated with vias < 2 μm [16], [19]. EMIB comprises of a bridge embedded in the FCBGA substrate with additional steps during panel level substrate manufacturing to embed and encapsulate the die, and fan out the bumps on C4 with a finer pitch than rest of the C4 region [14]. Embedded HDFO substrates require initial copper pillar formation, die bond, encapsulation with mold and fanout of RDLs [20].

C. Silicon Interposers and Substrates

Silicon Interposers: Silicon interposers were introduced in 2011 when Xilinx introduced a "die-splitting" methodology to partition large, low-yield Field Programmable Gate Arrays (FPGAs) into multiple high-yield functional tiles [21]. These tiles were reconnected using back-end-of-line (BEOL) copper wiring patterned onto a thin silicon interposer, using Through-Silicon Vias (TSVs) for vertical connections between the ICs and the package substrate [21]. Silicon interposers were subsequently adopted by AMD to integrate high-bandwidth memory (HBM) to graphics processing unit (GPU), leading to widespread use of silicon interposers for multi-die heterogenous integration and chiplet-based architectures [22]. Today, TSMC's CoWoS-S (Chip-on-Wafer-on-Substrate with Silicon Interposer) has been scaled to high-volume manufacturing (HVM) in 2.5D and 3D integration and is also available from a number of other foundries [23]. Silicon interposers can be fabricated as a passive silicon substrate optimized for high-density multi-die routing and interconnect pitch translation. An active interposer platform that embeds functional complementary metal-oxide-semiconductor (CMOS) logic, power distribution, or test circuitry directly within the underlying silicon interposer has been developed by Intel and others [24].

Double-Sided Silicon-Cored Substrates: Silicon core substrates have been explored and demonstrated in both wafer and panel formats with double sided RDL or build-up layers [25]. The first demonstrations utilized a polycrystalline silicon wafer or panel borrowed from the solar cell supply chain ecosystem, with laser ablated or plasma etched through silicon vias with polymer or oxide liners, polymer build-up layers and semi-additive processes for copper wiring [25]. More recent developments have focused on scaling the wiring pitch using both wafer and panel process methods [26]. Large silicon panels have recently been introduced as a manufacturing ready core material by Mitsubishi Materials, Japan.

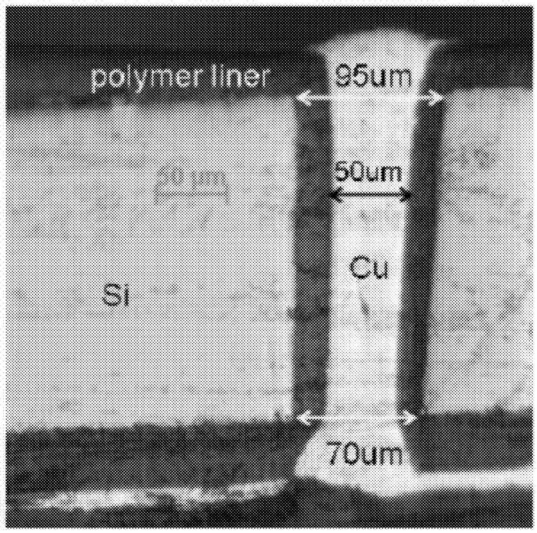

Fig. 3. Double sided Build-up Layers and polymer lined TSVs in Polycrystalline Silicon Core Substrates [25]

The major benefit of silicon interposers and silicon core substrates is the Coefficient of Thermal Expansion (CTE)

match to silicon chips, suppressing global thermo-mechanical warpage [25]. The redistribution layers (RDL) on silicon substrates can be fabricated using one of two methods, (a) copper-polymer RDLs that provide compliant, low-stress routing paths for medium-density lines and power delivery networks, and (b) Cu-SiO_2 inorganic RDLs that enable aggressive sub-micron line/space scaling via standard damascene processes to maximize parallel die-to-die interconnections.

D. Glass Substrates

Glass-based substrates can be divided into two categories, namely 1) glass core substrates, and 2) glass interposers. Both glass core substrates and glass interposers take advantage of the unique properties that glass has to offer as structural material for advanced packaging applications. For glass core substrates, the typical glass core thickness ranges from 600 µm up to 1 mm, whereas the glass interposer thickness range is typically 100 – 300 µm.

Glass core substrates are in principle an advanced version of the organic glass fiber and resin core FCBGA substrates that are described in section II B). Glass and organic core substrates share a very similar build up structure manufactured typically with a Semi-Additive Process (SAP) on laminated dielectrics such as glass filled resins (e.g. ABF), photosensitive dielectrics, or a combination thereof. In general, a glass core offers several advantages over the glass fiber / resin core: 1) a higher Young's modulus of glass allows larger packages with reduced warping at the same core thickness, 2) the CTE of glass can be altered through its composition. On the lower end of CTE, it is possible for the glass CTE to match silicon, on the higher end values much closer to metals and organics have been reported [27]. This allows further reduction of CTE impact on overall package warping and enables reliability improvements for large form factor packages. 3) Since glass is a homogeneous material, any thermal cycling as a result of, for example, ABF curing does not affect overall size integrity and pattern shift which impact overlay performance. Unlike organic core materials, glass will return to its original dimensions at room temperature which facilitates accurate patterning and via formation in the subsequent build up steps. This allows feature size scaling beyond the capability of organic core-based substrates. [28]. 4) Developments in Through Glass Via (TGV) formation have shown an excellent capability of the glass-based core to support a higher vertical I/O density as compared to Through Holes (TH) formed in organic core-based substrates. State of the art TGV formation is done with for example LPKF's Laser-Induced Deep Etching (LIDE) process where a laser is used to alter the glass structure locally to enhance its etching rate in hydrofluoric (HF) or metal / organic hydroxide-based solutions. This allows a finer pitch and a higher aspect ratio for TGVs [29, 30] as compared to mechanically drilled THs in organic cores, where the pitch is limited to drill bit size (approx. 100 µm minimum). In addition, the excellent dielectric properties of glass ensure a better electrical performance in particular for high frequency signal I/O [31, 32].

Glass interposers were initially proposed as an alternative for silicon interposer, for example in high frequency applications due to the excellent dielectric characteristics of glass compared to silicon. The main distinction between glass interposer and glass core substrate stems from functionality; glass interposers are a means of high density die-to-die I/O and pitch translation from dies to in most cases a standard organic core FCBGA substrate as opposed to glass core technology which represents the advancement of FCBGA substrate. Glass interposers typically are thinner than organic core glass, and are often manufactured on wafer scale using a carrier to handle thin glass [33]. Wafer level packaging processes and processing techniques common to silicon interposer can be used, which allows high yield, fine features to be manufactured typically beyond the capability of glass core based FCBGA substrates.

III. Comparison and Challenges of Substrate Types

A. Comparison of substrate types

In the previous sections, several types of substrates were discussed. Depending on the final intended application it makes sense to prefer one substrate type over another. Typically, this decision is driven by a consideration of capability (can it support high end application architectures through meeting required I/O densities) cost, and how well can it control large package warpage. Especially for the current and future packaging needs for AI-related chipset, large form-factor, high performance packages need to withstand CTE-driven package warpage as the silicon content is increasing dramatically. Table I summarizes the relative performance of the previously discussed substrate types against these criteria; and subsequent sections will discuss the challenges these substrate types may face for advanced substrate applications more in-depth.

TABLE I
COMPARISON OF SUBSTRATE TYPES

Property	Ceramic	Organic	Silicon	Glass
Cost	+	++	- -	-
Die Area	-	+/-	- -	++
IO Density	-	+	+++	++
Warpage	+++	+/-	+++	+++

B. Challenges for different substrate types

Various challenges for each substrate type are summarized in this section.

1) **Ceramic Substrates:** As micro-bump pitches scale below 10µm and redistribution layer (RDL) line/space (L/S) resolutions scale below 2µm to support chiplet integration, several fundamental materials and process challenges must be overcome.
   a) **Surface Roughness:** The most immediate barrier to integrating ultra-fine pitch RDLs directly onto LTCC or standard ceramic substrates is the inherent surface roughness (R_a) resulting from the sintering process.

Traditional thick-film screen printing used in LTCC is fundamentally limited to line widths of approximately 30-50μm. Transitioning to thin-film, semi-additive processes (SAP) or dual-damascene copper plating requires a nearly planar surface to prevent lithographic scattering and ensure precise photoresist adhesion. Current research is focused on chemical-mechanical planarization (CMP) of ceramics and the application of ultra-thin, low-loss planarization polymers prior to RDL fabrication.

b) **Localized Stress:** Although a high-stiffness, low-CTE ceramic substrate eliminates the global package warpage that plagues organic substrates and interposers, this mechanical rigidity can cause localized thermo-mechanical stresses on micro bumps. Such localized shear stresses concentrate at the bump interfaces, significantly increasing the risk of fatigue, crack propagation, and bump shear. Underfill materials used for chiplet assembly on ceramic substrates need to be engineered to accommodate these localized stress concentration effects.

c) **Panel size limitations:** Ceramic substrates use 150 mm and 200 mm square panels, with some leading manufacturers able to fabricate 300mm square panels. The panel size limitations of LTCC substrates are mainly due to the high shrinkage during the co-firing process. Green tape material improvements and "zero-shrink" manufacturing process innovations have reduced the shrinkage effects significantly in the last few decades; however, ceramic substrates face challenges in scaling to larger panel sizes to enable package sizes larger than 80-100mm.

2) **Organic Substrates:** The FCBGAs and HDFOs have evolved to accommodate multichip packages, however face challenges as pitch scales down, package area increases, and thermal design power increases:

a) **Substrate coplanarity:** Increased die complexity and larger packages suffer from large warpage and can reduce chip attach and SMT yield. For FCxGAs, the substrate core is modified with lower CTE or increased thickness to meet warpage targets. For HDFOs, the glass carrier, mold, and RDL stackup influence the warpage. Besides the chip attach and SMT, the warpage also limits the patterning yields, particularly at the panel level.

b) **Patterning smaller features:** Typical panel level substrates use dry film photoresists which work well for existing feature sizes. However finer L/S features would need development of higher performing thinner resists. Heterogenous integration roadmap trends towards 5/5 μm L/S on panel level FCBGAs [14]. Additionally, HDFOs will trend towards a sub 1/1 μm L/S which would require development of higher performing wafer level resists, which can accommodate higher aspect ratios [14], [19]. Development of polymer damascene provides additional scalability with these high aspect ratio features beyond the semi additive patterning used for RDLs [17]. Besides lithography, FCBGAs use panel level laser via drilling and wet cleaning. Scaling these to 30 μm and below on the panel level requires process optimizations to ensure no residue remains before plating. Lastly, feature sizes reduction combined with layer counts increase, have resulted in the need for high aspect feature plating. Development of plating process and chemistries enabling complete fill of the features is required, with desired throughput and uniform plating across the panel and wafers.

c) **HSIO requirements:** Development of newer low loss ABF has driven HSIO enablement which continues to be driven through the growing demand for low latency and higher bandwidth. As feature sizes reduce, copper roughness results in higher loss and needs to be reduced. This requires optimization of copper and dielectric adhesion to ensure good reliability. With increased layer counts and larger package areas, the stress could additionally impact reliability and interfacial adhesion is critical.

d) **Bump pitch scaling**: Bump pitch for FCBGAs are trending to sub 100 μm pitches, which requires use of panel level electroplating instead of the screen-printed solder ball technology. Furthermore, the plated bump coplanarity will be critical to ensure high yielding chip attach processes. As the package area increases, bumping will require tighter coplanarity control further increasing the manufacturing challenges.

e) **Power delivery:** As the Thermal Design Power (TDP) keeps increasing with AI and HPC workload beyond 1kW on package level, an efficient power delivery network is desired. Increased routing layers and lengths result in poor power integrity and requires simplified design and architecture which can reduce routing length and improve power efficiency. Additionally, capacitors and components can be strategically placed to enable improved power integrity.

3) **Silicon Interposers:**

Most of the technical challenges for wafer-based silicon interposers have been addressed since the technology was introduced. Silicon interposers mainly faced cost challenges in scaling to very high-volume production due to the high cost of wafer fab processes and limited number of large body size interposers from 300mm wafers.

Silicon core substrates and silicon interposers both face challenges in CTE mismatch to the organic substrates or PWBs on which they are assembled, especially for large body sizes.

4) **Glass Substrates:**

As glass-based interposer and advanced FCBGA technology continue to be developed, many challenges remain. At present glass interposer is a more mature technology than glass core FCBGA substrates, mostly due to the ability to re-use IP-blocks from silicon wafer process technology. For glass core substrate technology

many of the challenges stem from needing to fabricate in panel format as well as a much greater thickness of the glass:

a) **Processing tool availability:** The processing tool landscape is, as of today, not well developed. It remains difficult to handle large format glass panels due to the inherent brittleness of this material. In addition, development of capable tool sets has only been a focus for tool vendors since approximately 2023, when Intel revealed their glass core substrate technology [34]. Handling of thin glass cores, and also in particular dicing, has proven to be difficult, although some progress was made by Disco recently on the latter topic [35].

b) **Adhesion layer and seed for high Aspect Ratio TGV:** Metallization of high-aspect ratio through holes remains a challenge. Physical Vapor Deposition (PVD) has been evaluated and, to some extent, accepted as a means to deposit an adhesion layer and copper seed on panel surface and TGV sidewalls for aspect ratios up to approximately 6-8:1. For higher aspect ratios, PVD is less suitable; it is a line-of-sight deposition method which is generally unable to provide adequate step coverage for higher aspect ratios [36, 37]. In addition, glass core metallization requires a two-sided deposition, which further complicates PVD tool sets and impacts throughput. Development of finer pitch and higher aspect ratio TGV has brought focus on wet deposition techniques for adhesion layer and seed due to a better handling of aspect ratios above 8:1, its ability to process both sides of a panel in one step, superior conformality for high aspect ratio TGV over PVD, and capability to process multiple panels at once. Several chemistry suppliers are working on a metal-oxide based adhesion layer, which in all cases requires a high temperature activation step to ensure adhesion strength [37, 38, 39]. This is to be seeded with an electroless copper process to prepare for subsequent TGV filling.

c) **Copper filling of high aspect ratio TGV:** Wafer-based processes such as Through Silicon Via (TSV) can provide a void and inclusion-free fill for aspect ratios well above 10:1, suited well for glass interposer technology when TGVs similar in dimension to TSV can be used. TSV Cu fill rates are in general too low to be practical, and impose a major penalty on cost for the much larger TGVs typically envisioned for glass-core FCBGA substrates. Several substrate core and plating chemistry suppliers are looking to enhance filling performance through use of pulse and reverse-pulse plating techniques, already well known from organic core substrate [37, 40, 41]. Even though there is some promise in these methods, high aspect ratios and large volumes are still difficult to fill. Other plating techniques focus on filling TGVs with a single sided electrical contact and using the glass as a template for pattern fill; a technique known in tall pillar plating, or more commonly a conformal plating technique in which the copper plated sidewall grows together in order to avoid a seam. [41]. Until a reliable and cost-effective solution for high aspect ratio TGV fill is available, conformal plating and paste fill techniques such as used in organic core FCBGA substrate and High Layer Count Multi-Layer Boards (HLC-MLB) are to be considered.

d) **Reliability:** Although several reports were made on component level thermal cycle stability of filled through glass vias, as of today there is no complete picture on overall board and system level reliability of glass core-based substrates as compared to organic core FCBGA substrates. A large set of parameters such as glass type, CTE, LIDE TGV quality, pattern density and design has yet to be explored completely to form an accurate picture of the final performance and the usable application space of this technology.

IV. Emerging Technologies Future Scope

Next generation technology inflections will be enabled by advanced substrates having following attributes; a) lowest signal loss (be it electrical or optical); b) highest I/O density with lowest signal/thermal cross-talk; c) excellent thermal dissipation; d) show high thermomechanical reliability at large area form-factors to enable integration of multiple dies, thus adding more functionality on the substrate.

The following emerging technologies will be enabled by next generation packages using advanced substrate technology for heterogeneous integration:

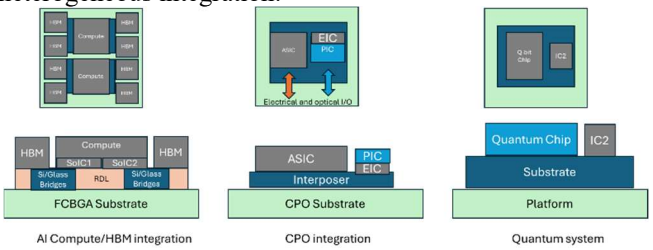

Fig. 4. Emerging subsystems needing advanced package substrates

1) AI GPU/HBM:

Building blocks of AI comprise of multiple compute and memory ICs attached first to an interposer and subsequently to an organic BGA substrate. Next generation GPUs for example, will have 2 or more GPU dies surrounded by 8 or more HBM stacked-memory dies, all integrated on a RDL interposer with silicon/glass bridges, providing high bandwidth (BW) interconnection between GPUs and memory. Further, silicon bridge technology have evolved from simple planar fine-pitch wiring levels to addition of TSVs, providing improved design flexibility for HI modules [42]. As we integrate more compute and memory chips on an interposer, the substrate onto which interposer is attached to need to have exceptional rigidity, low warpage during assembly and support small pitch I/O. The transition from organic to glass-based substrates will enable package size scaling with improved functionality [43].

Additionally, HPC and AI accelerator subsystems comprise of compute modules with hybrid bonded chip-lets integrated on a silicon interposer [44]. 3D stacking of chip-lets increase functional density, however, there is a need to effectively remove heat from 3D stacked dies. The primary heat removal pathway is away from the substrate, achieved using advanced thermal interface materials and heat sinks, through a combination of conduction, convection mechanisms. Substrates with higher thermal conductivity such as SiC have gathered active interest in industry and academia alike [45]. Future systems can be envisioned having cooling pathways both through heat sinks and advanced substrates to mitigate local thermal hotspots, thus improving overall device performance.

2) Co-Packaged Optics:

As compute and data transfer speeds increase, optical interconnects are needed to meet the growing BW demand. This requires conversion of signals between electrical and optical domains. A pluggable optical transceiver is one such module that can be attached to a package substrate to enable this signal conversion. Future systems however need lower latency, and hence there is a drive to co-locate optical components on the same package as compute/control electronic dies. This will require substrates that support very low electrical signal loss routing, and have integrated optical waveguides [46]. Interfaces between fiber and waveguides, adhesives, passive alignment strategy are key considerations for a reliable opto-electronic module.

3) Quantum Computing:

Quantum computing has been a topic of active research and development over the past few years. Unlike traditional computing that operates on binary (1s and 0s), Q-bits or quantum bits assume states between a 1 and 0, based on quantum mechanics. Manipulation of such Q-bits may in the future help solve complex problems that are not possible with traditional computers. At the heart of such systems is a quantum chip or quantum processor, that can be broadly classified into two categories: a) matter based (ions) and b) light based (photonic). Such quantum chips need to be packaged on a substrate providing reliable and efficient interconnection between chip and external world.

Such substrates need to demonstrate; a) low loss to ensure Q-bit fidelity that includes low loss waveguides on chip and on substrates, and low electrical loss interconnects on substrates for high signal and power integrity. Several of these quantum chips operate at deep cryogenic temperatures (below 4K); necessitating substrates that are reliable at extremely low temperatures. While the industry works on building the fundamental Q-bit chip, package substrates will play a pivotal role in enabling efficient scaling of quantum processors. The properties of advanced organic, silicon and glass substrates explained in the earlier sections can be leveraged to integrate a new generation of compute systems in the next decade.

V. Conclusion

As artificial intelligence and high-performance computing drive the needs for larger, more capable and reliable substrates, several technologies are emerging as enabling substrate platforms for large and complex heterogeneously integrated chipsets. Existing technologies such as organic core build-up laminate are undergoing continuous evolution to meet the ever-increasing demands associated with continued performance scaling, but may in the end not meet the most stringent demands that are required for future packages. More recently, this trend has renewed interest in ceramic substrates due to their excellent mechanical stability, high-frequency dielectric properties and reliability performance. As silicon has been the material of choice for interposer technology for some time, this mature platform offers excellent I/O density and mechanical stability. However, scaling to large chip aggregates is not cost effective at this moment due to the limited scalability of substrate size and associated processing equipment. Novel technologies based on glass as a build-up substrate core or interposer material have gained much traction over the past year. Glass is an attractive material which enables large, mechanically stable, high I/O density and high-frequency compatible packages, which allow extended performance scaling well beyond organic core build-up substrate and silicon interposer. This will enable the next generations of packages for AI, Co-packaged optics and eventually quantum computing applications.

References and Footnotes

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