Nanopackaging Solutions for Interconnections, Power, and RF Integration Challenges

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***Abstract*—Heterogeneous integration (HI) enabled by advanced packaging serves as an overarching strategy to integrate disparate, specialized materials and components across various architectures into a high-performance system. The ongoing miniaturization of interconnect dimensions from the micron scale to the sub-micron regime, driven by high-bandwidth and fine-pitch routing requirements to advance HI, increases the significance of nanoscale phenomena in governing package reliability. As the characteristic dimensions approach nanoscale, several key phenomena such interconnect resistance, diffusion kinetics, nonlinear phenomena, phonon transport, deformation behavior etc. are affected and lead to new important considerations in modeling, design and characterization. Similarly, embedded components for vertical power delivery or RF functions in the package invariably rely on advanced nanomaterials and architectures for performance, process compatibility and reliability. Understanding and mitigating reliability challenges at the nanoscale has therefore become essential for ensuring performance and reliability of HI packages through nanopackaging advances. This article reviews the underlying reliability mechanisms, characterization, and modeling techniques required to address these challenges, with particular emphasis on package level interconnects and interfaces, and embedded components for integrated power and RF functions. Finally, emerging nano-engineered thermal materials for enhanced reliability are discussed, along with challenges and opportunities for RF substrate integration.**

I. Packaging at Nanoscale for Heterogeneous Integration (HI)

High-density heterogeneous package integration leads to escalating challenges in modeling, design, characterization, and manufacturing in order to ensure that the package meets customer's performance and reliability requirements (See Figure 1) [1], [2]. Solving these challenges has always been a key objective of nanopackaging, which leverages nanoscale materials and processes in advanced semiconductor packaging to enable continued miniaturization, enhance performance, functionality, reliability, and cost efficiency [3]. Nanoscale materials in this article refer to materials that are synthesized, processed or modeling at any characteristic dimension (film thickness, particle size, particle coating thickness, grain size etc.) at nanoscale to benefit or alter package design features such as interconnect layouts, routing densities, or properties such as magnetic (frequency stability and quality factor), dielectric (capacitance densities), mechanical (creep, deformation behavior), thermal (enhanced conductivity with superior phonon coupling in one or more directions).

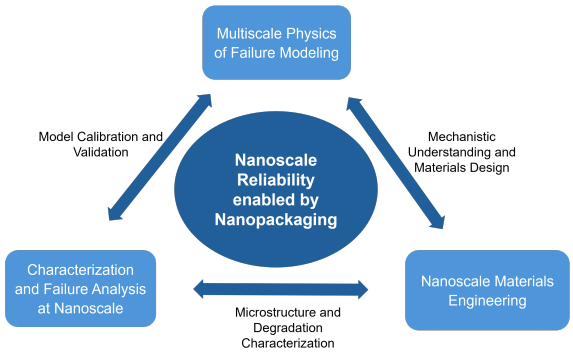


Fig. 1. Nanoscale Reliability Enabled by Nanopackaging Technologies [1].

As Moore's law approaches its practical limits, the semiconductor industry is pivoting towards advanced packaging as its primary scaling approach. High-performance substrate platforms with 2.5D, 3D integrated circuit (IC) packaging, fan-out wafer level packaging (FOWLP), fan-out panel level packaging (FOPLP), etc., are evolving at an accelerated pace to advance HI, meet increasingly demanding form factors, and improve system performance and efficiency. Among these advanced technologies, for example, FOWLP has emerged as a key platform for HI, offering high input/output (I/O) density, reduced form factor, and superior electrical performance. Central to the FOWLP architectures are redistribution layers (RDLs) which are Cu-dielectric interfaces acting as high-density routing infrastructures providing necessary electrical pathways to connect disparate dies embedded into epoxy matrices, enabling high-bandwidth, and low latency communication required for HI.

Continued-package level scaling relies on reducing RDL line width and spacing (L/S) to sub-micron scale, where nanoscale phenomena become significant. As interconnect dimensions continue to shrink, they become increasingly vulnerable to atomic-scale defects, material degradation, thermo-mechanical stresses, and interfacial failures that can compromise reliability. Nanoscale degradation mechanisms contribute to key reliability concerns, including electromigration (EM)-

induced failure through atomic diffusion, void/hillock evolution, and interfacial delamination through localized stresses and bond breaking associated with coefficient of thermal expansion (CTE) mismatch [4]–[6]. On the other hand, scaling to nanodiensions often enhance properties compared to micro-dimensional materials and are of high interest to provide various package functions. For example, exchange coupling at nanoscale gives the most desirable softness in magnetic cores. Nanodielectrics and nanoelectrodes provide the capacitance density for power delivery applications. They may also improve fracture resistance in some architectures and provide a new class of 2D thermal materials. However, they also degrade some attributes such as interconnect resistance. All of these are key considerations in nanopackaging. Therefore, Nanopackaging plays a critical role in addressing these challenges by enabling robust interconnects, efficient heat dissipation, mechanical integrity, and interfacial stability to ensure long-term performance of next-generation semiconductor packages.

II. Characterization and Failure Analysis at Nanoscale

Nanoscale failure analysis of scaled interconnects such as RDLs, solder bumps and copper pillars etc., requires advanced characterization techniques capable of resolving structural and chemical changes at atomic and nanoscale resolution as reliability becomes increasingly microstructure- and interface-dominated. Experimental analysis coupled with high resolution microscopy techniques enables identification of localized voiding, atomic migration, oxidation and interfacial degradation, while establishing relationship between these failure mechanisms and underlying microstructure and heterogeneous interfaces.

For instance, to study EM and interfacial delamination, Do *et al.* employed focused ion beam (FIB) analysis to localize EM-induced voiding, oxidation and Cu-dielectric delamination, while transmission electron microscopy (TEM-EDS) resolved the Cu/Ti/dielectric interfaces and confirmed suppression of Cu diffusion through Ti barrier [7]. In-situ high resolution transmission electron microscopy (HRTEM) analysis by Shen *et al.* revealed that columnar grain structure confined EM-induced voids, reducing their expansion rate while twin boundaries in nanotwinned copper constrained void growth. EM resistance was also dependent on the direction of electron flow relative to the twin boundary orientation, highlighting the influence of microstructure on atomic migration and void evolution [8]. Zhang *et al.* demonstrated that analyzing microstructural parameters (See Figure 2) such as annealing temperature, grain size, and orientation is essential to understand the mechanisms influencing EM lifetime and reliability of copper interconnects [9]. Such studies based on experimentation along with microscopy analysis provide insights into microstructure-dependent failure mechanisms, enabling enhanced interconnect design and reliability.

Furthermore, interfaces such as RDL/passivation, die-attach-underfill can fail at nanoscale where conventional peel, pull and four-point bend tests become inadequate, especially for ultrathin barrier and seed layers and low-k dielectrics. Nanoindentation based techniques induce localized delamination and enable extraction of interfacial fracture energy (G_c), while FIB-milled micro-cantilever and double cantilever beam methods with in-situ nanoindentation enable localized measurement of G_c under mixed mode loading, relevant to interconnects and interfaces such as RDLs, through silicon vias (TSVs) and hybrid bonding [10]–[12].

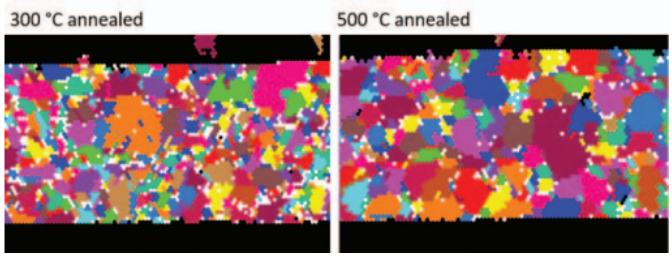


Fig. 2. Grain Map based on Annealing Temperatures [9].

III. Multiscale Reliability Modeling and Prediction

Multiscale modeling is essential to analyze mechanisms governing interconnect reliability as continuum physics fails to predict material behavior at the nanoscale. Atomistic modeling is valuable for resolving failure process of interfaces that are difficult to isolate experimentally, enabling identification of atomic level failure drivers, optimization of interfacial strength, and design of strain-tolerant materials for enhanced reliability. Modeling techniques across multiple length scales have been employed to address the reliability challenges of advanced packaging. Among these, molecular dynamics (MD) simulations are particularly suited well for investigating nanoscale reliability issues as they provide insights into atomic scale bonding, interfacial behavior, and predict material properties essential for informing continuum models to accurately estimate package-level stress distributions.

MD simulations have been applied to characterize nanoscale interfacial separation behavior of Copper/Polyimide interfaces to calculate intrinsic traction-separation relationships governing crack initiation and delamination. These parameters derived from atomistic perspective were incorporated into finite element analysis (FEA) based cohesive zone model (CZM) for efficient reliability prediction of RDLs in FOWLP. This approach demonstrates multiscale framework translating nanoscale interfacial behavior into macroscale reliability models as shown in Figure 3 [13]. To investigate the electromigration failure of copper interconnects, MD simulations were coupled with FEA by establishing a framework enabling dynamic interaction between evolving microstructural characteristics and continuum-scale field distributions [14]. Additionally, MD simulations combined with nanoindentation experiments by Feng *et al.* revealed that EM-induced voids in Al interconnects influence dislocation behavior, leading to progressive degradation of mechanical properties [15].

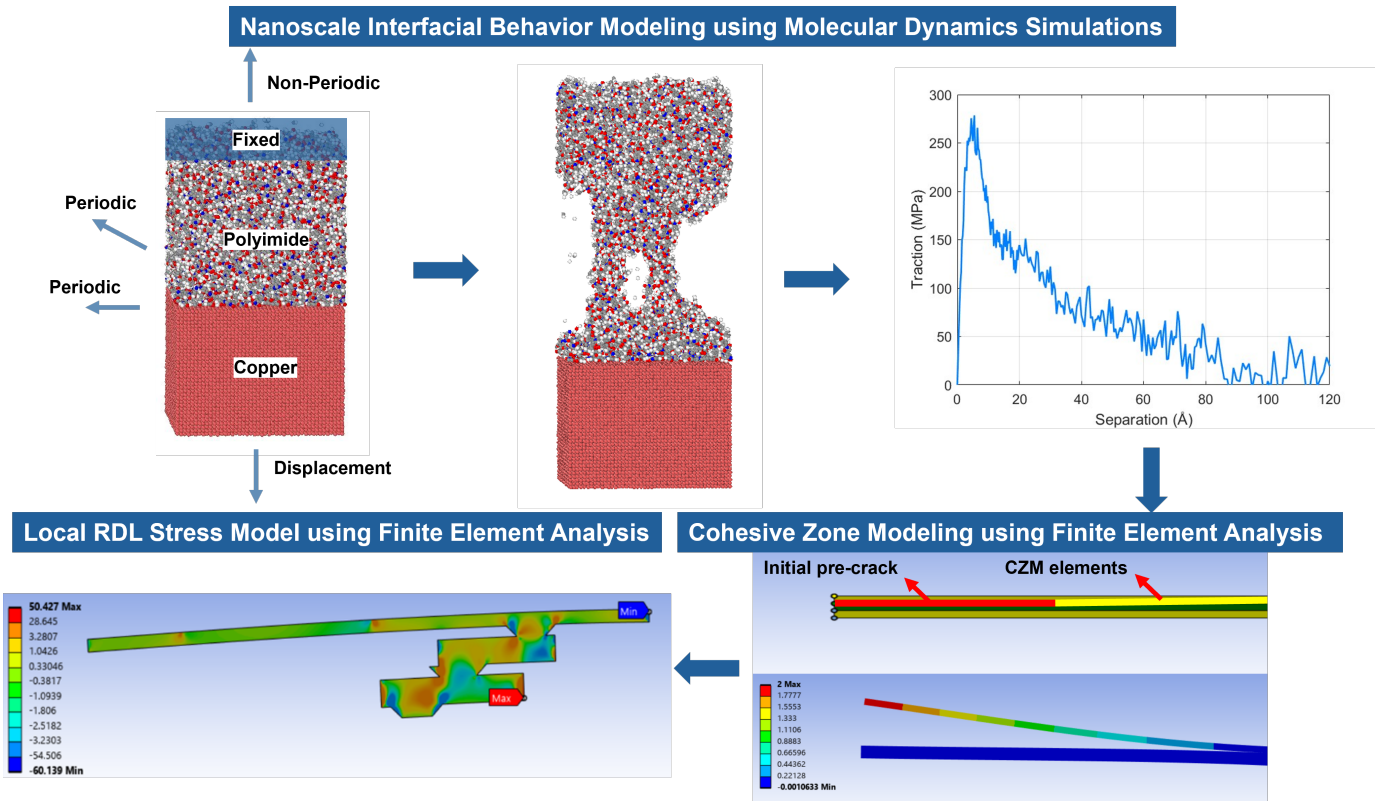


Fig. 3. Multiscale RDL Reliability Modeling: MD informed CZM Modeling [13].

Therefore, as feature sizes continue to shrink and the complexity of HI packages increases, MD provides fundamental insights into nanoscale behavior, facilitates identification of favorable material and microstructural configurations, and enables the extraction of key parameters for continuum-scale models. As a result, MD serves as a predictive screening tool that guides experimental design by narrowing the design space and directing experimental efforts toward the most promising conditions. Multiscale modeling, wherein macroscale models are informed by nanoscale characteristics, along with multiphysics modeling accounting for coupled interactions, is crucial for designing defect-resistant package architectures prior to high-cost fabrication [4].

IV. Materials Engineering for Enhanced Reliability

Nanoscale geometries are strongly dependent on microstructural features, making materials engineering at nanoscale such as tailoring grain structures, interfaces, barriers, and nanocomposites rather than optimizing bulk properties is an important strategy for reliability enhancement. Microstructure engineering of copper, including coarse-grained, nanocrystalline, nanotwinned, heterogeneous, and low dimensional architectures, are therefore being explored to strengthen electrical, thermal, mechanical reliability of scaled interconnects. Due to suppression of void nucleation and enhanced twin boundary strength, nanotwinned copper (NT-Cu) demonstrated superior mechanical strength, electrical conductivity, and excellent thermal conductivity, making it promising approach for RDLs [8], [16].

Nanocomposites provide another approach to tailor interconnect properties, for example, graphene-copper(GC-Cu) has demonstrated longer EM lifetimes, reduced oxidation and voiding, and lower current crowding and stress concentration than NT-Cu [17].

Beyond engineering the metal interconnect, nanoscale barrier and interface engineering can further restrict interfacial transport as they are important pathways for diffusion, electromigration and delamination. Do et al. demonstrated that nanometer scale titanium (Ti) barrier with top-side capping suppresses Cu diffusion and oxidation in embedded trace RDLs, thereby reducing void formation and enhancing EM reliability [7].

V. Nanoscale Reliability Challenges and Solutions for Power Components

The rapid increase in power density in high-performance computing, AI accelerators, and advanced semiconductor packages is driving a transition toward vertical power delivery, in which power inductors and capacitors are positioned increasingly close to, or directly above and around, the power-management circuitry and processor. This is illustrated in Figure 4. These architectures require inductor traces with magnetic cores that are capable of operating at high current

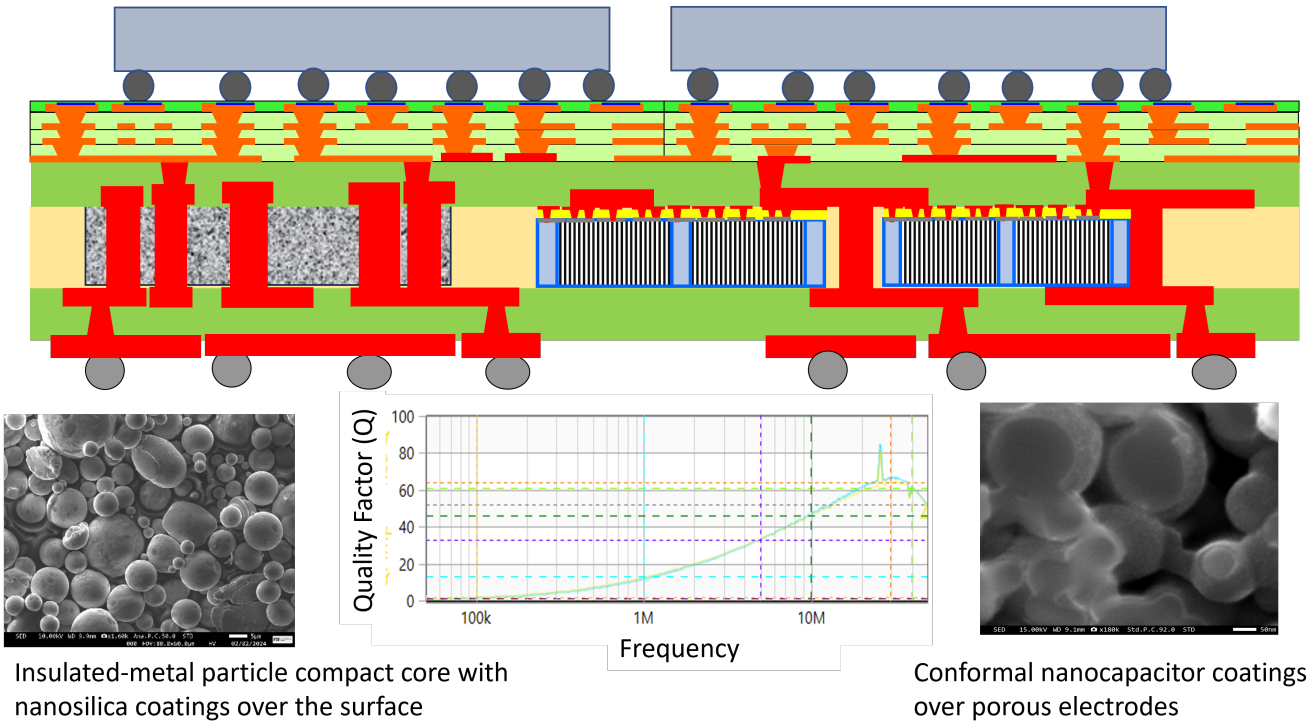


Fig. 4. Vertical power delivery drives conformal insulation coatings on metal particles (left, from Himet Materials LLC), conformal nanoscale ALD coatings for nanocapacitors (right, from IEEE PwrSoc 2025)

density (for example, 10 A/mm^2 with 1 A ripple current) without saturation while maintaining low electrical loss, high thermal stability, and long-term reliability.

Insulated metal composite (IMC) magnetic cores, consisting of electrically conductive magnetic particles separated by thin insulating layers, provide an attractive pathway towards these requirements. A critical limitation of conventional organic-binder magnetic composites is their thermal stability. For vertical power delivery, inorganic insulation also offers an important reliability advantage. The oxide coating can withstand substantially higher processing and operating temperatures than many polymeric insulation systems, enabling more aggressive thermal processing and improved compatibility with high-temperature packaging environments. Polymer insulation and binders can soften, decompose, outgas, or undergo dimensional changes at elevated temperatures. These effects can degrade interparticle insulation, increase eddy-current loss, and produce mechanical or electrical failure during extended high-temperature operation.

In contrast, inorganic dielectric coatings, such as silica, alumina, zirconia, or other oxide-based layers, can provide thermally stable electrical isolation between individual magnetic particles. A thin conformal oxide shell allows the magnetic material to retain a high volumetric magnetic fraction while interrupting electrically conductive paths between particles. During compaction, the insulated particles form a dense magnetic network while the oxide interfaces suppress interparticle circulating currents. This is particularly important at the elevated switching frequencies associated with modern voltage-regulator modules, where eddy-current loss can become a major contributor to total core loss.

Increasing the electrical resistivity of the interparticle pathways therefore provides an opportunity to simultaneously maintain magnetic permeability and reduce frequency-dependent loss. Stable inorganic interfaces can also reduce thermally induced degradation of the magnetic composite during repeated power cycling. The key engineering challenge is to optimize coating thickness, particle insulation, compaction density, and magnetic permeability simultaneously: excessive insulation or porosity reduces magnetic loading, while insufficient insulation increases eddy-current loss because of conduction through particle contacts. Thus, controlled inorganic surface engineering provides a pathway toward compact, high-current, thermally robust inductors suitable for high-density vertical power delivery architectures.

A. Nanoscale Conformal Coatings in Vertical Power Delivery

Nanoscale electrode and dielectrics for capacitors provide a pathway to integrate substantial decoupling capacitance directly within the power-delivery structure, reducing the electrical distance between the power source and high-current switching loads. The central materials challenge is achieving a high capacitance density while maintaining dielectric stability, low leakage, low equivalent series resistance, and long-term reliability under high electric field and temperature. Nanoscale conformal deposition, particularly atomic layer deposition

(ALD), is attractive because it can uniformly coat high-aspect-ratio trenches or other high surface-area architectures and precisely control dielectric and electrode thickness at the nanometer scale.

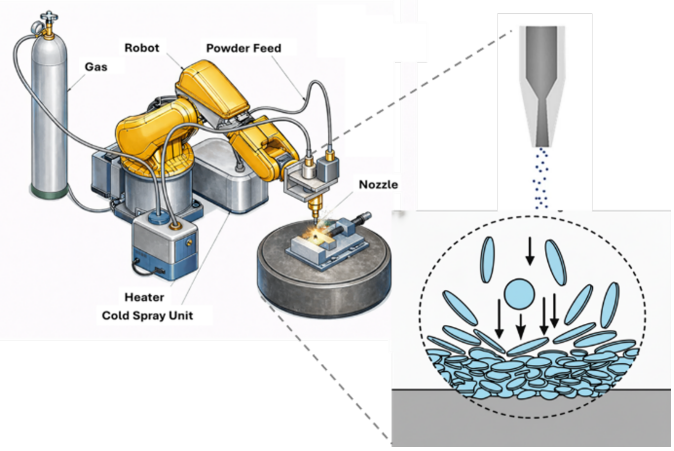


Fig. 5. Schematic of the cold spray process for depositing 2D materials. The magnified view shows 2D material particles accelerated through a converging-diverging nozzle, impacting the substrate at high velocity and deforming and stacking to form a dense, binder-free deposit without melting.

A representative structure can employ a conductive TiN electrode/high-k dielectric/TiN electrode stack, with HfO_2-based ferroelectric or antiferroelectric materials such as $Hf_{0.5}Zr_{0.5}O_2$ (HZO) providing substantially higher effective capacitance than conventional SiO_2 or Al_2O_3. HZO is particularly attractive because its electrical properties can be engineered through composition, thickness, crystallization conditions, dopants, interfaces, and electrode constraints. Other electrode materials are being considered, including Ru, W, or suitably engineered metal nitrides, depending on the required thermal budget, work function, diffusion resistance, and integration compatibility. Thin interfacial layers such as Al_2O_3 or SiO_2 are also introduced to control leakage and interface reactions, although excessive interfacial thickness results in a trade-off in capacitance density.

The main reliability challenge is that the thickness of the nanoscale amplifies the consequences of defects. Pinholes, nonuniform thickness, grain boundaries, oxygen vacancies, electrode roughness, and nonuniform trench-bottom or sidewall deposition can produce localized high electric fields. These sites can initiate trap generation, charge trapping, field-assisted leakage, soft breakdown, and eventually hard dielectric breakdown. In HZO specifically, repeated electrical cycling can produce polarization fatigue, wake-up behavior, imprint, and phase evolution, while oxygen-vacancy migration and electrode/dielectric interfacial reactions can degrade the electrical characteristics. For example, oxygen scavenging by ALD TiN electrodes increases the Equivalent Series Resistance (ESR) in capacitor stacks. Thermal cycling introduces additional concerns because differences in thermal expansion between the substrate, electrode, dielectric, and surrounding materials generate mechanical stress. In very deep trenches, these effects can be compounded by aspect-ratio- and roughness-dependent curvatures, residual stress, and incomplete conformality.

Reliability therefore requires controlling the entire nanoscale stack, rather than evaluating the dielectric alone. ALD process windows should establish conformality, thickness uniformity, defect control and interface quality throughout the trench.

VI. Nanoscale reliability challenges and solutions for RF components

Embedded RF packaging needs high thermal conductivity dielectrics that also provide for low signal losses as the medium carries high-frequency signal pathways. Thermal management in embedded RF integrated-circuit (IC) packaging differs fundamentally from conventional power-electronics cooling because the thermal solution must coexist with stringent electromagnetic, dielectric, dimensional, and signal-integrity constraints. Ceramic packaging appears to be a viable option for this, but is limited in achieving low-cost and scalable manufacturing. However, localized ceramic, glass or metal tiles in a laminate panel fan-out packaging is a compelling heterogeneous integration solution to benefit from the unique advantages of inorganic and laminate packaging without compromising scaling densities [19] as shown in Figure 6. Materials with thickness in the atomic scale and microscale lateral dimensions known as 2D materials offer distinct advantages for enhancing reliability in heterogenous integration and electronics packaging. These atomically thin layered materials with strong in plane covalent bonding and weak van der Waals forces between layers due their structural anisotropy possess excellent mechanical properties, thermal stability/barrier behavior, device-functionality and tunability [20]. Graphene, Hexagonal Boron Nitride, Transitonal Metal dichalcogenides (TMDCs), $HfSe_2$, MXenes etc are some of the promising 2D materials.

Integrating these materials as heterostructures and super lattices for potential state-of-the art applications require complex epitaxial growth and vapor deposition routes. However, these methods have their own limitations. They depend on one-to-one chemical bonding, which restricts integration to materials with similar lattice symmetry, lattice constants and processing conditions. Dissimilar systems, therefore, suffer from interface disorder, strain and misfit dislocations [21]. Integrating dissimilar materials with pristine interfaces remains a major challenge, because interface defects often initiate the reliability failures that limit device performance.

Cold-spray, a solid-state deposition technique, offers a promising alternative to overcome these constraints. In this process, powders are accelerated to high velocity and deposited by impact, which allows thick, pristine, binder-free layers to be built on a variety of substrates. As the process operates well below the melting temperature of the feedstock, it helps retain the intrinsic properties of the 2D materials and avoids thermally induced phase changes and interfacial reactions. Figure 5 shows a schematic of the cold spray process

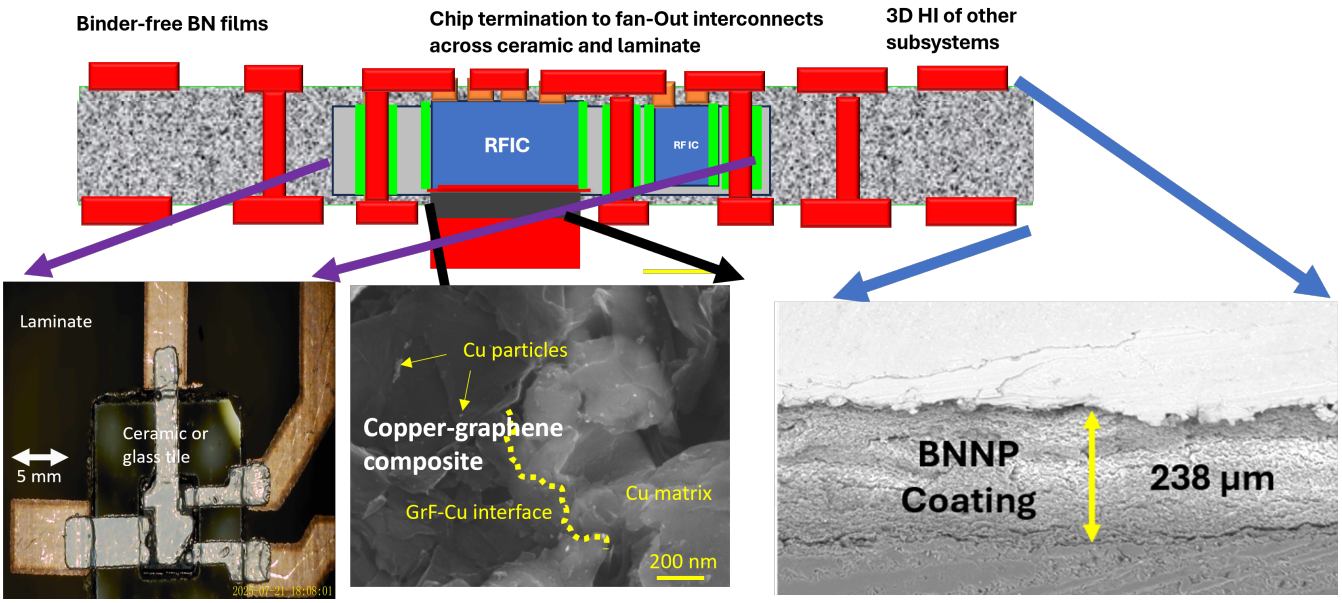


Fig. 6. Nanoscale copper-graphene composites as backside heat-spreader along with shielding functions [18] and BN films as volumetric heat-spreaders in an embedded panel fan-out RF package.

for 2D materials. Impact-induced plastic deformation of the 2D material, together with mechanical interlocking between the feedstock particles and the substrate, promotes strong interfacial bonding and results in reliable coating-substrate interfaces.

Among 2D materials, boron nitride (BN) stands out for its thermal dissipation properties. Its layered structure and atomic-level thickness give it an in-plane thermal conductivity of 400 W/mK, while its electrical insulation, low coefficient of thermal expansion (CTE) and low dielectric loss make it suite well to demanding electronic environments [22], [23]. For embedded RF ICs, hexagonal boron nitride (h-BN) is particularly attractive because it provides a route to increasing thermal conductivity while retaining electrical insulation. Unlike graphitic carbon, h-BN does not create an electrically conductive path around high-frequency interconnects, transmission lines, or active devices. Its layered crystal structure provides high intrinsic phonon conductivity, although the extreme anisotropy of the individual platelets means that the composite architecture is as important as filler concentration in determining the anisotropic properties. These attributes position BN as a game-changing material for electronics packaging and heterogeneous integration (HI) applications.

Recent work on h-BN/polymer composites demonstrates that nanoscale and few-layer BN, combined with controlled orientation and three-dimensional heat-conduction networks, can produce substantially higher composite thermal conductivity than conventional randomly dispersed BN systems. However, realizing these benefits in practice depends on how BN is deposited. Current BN coatings and deposits rely on polymer binders or additives, or use BN as a filler in epoxy. The polymer phase dilutes the intrinsic properties of BN and introduces reliability challenges and thermal instabilities. A binder-free deposition route is therefore needed to retain the intrinsic properties of BN in functional coatings. Figure 6 shows that cold-spray additive manufacturing deposited a thick, binder-free coating of 2D boron nitride nanoplatelets (BNNPs) on a commercially pure aluminum substrate, reaching a thickness of 238 μm. The coating was built up through high-velocity impact, with boron nitride deforming at localized impact zones and bonding both to the substrate and between neighboring platelets. The binder-free architecture improves heat dissipation, since heat can travel through continuous BN rather than being interrupted by a low-conductivity polymer phase, while strong particle-substrate adhesion enhances interfacial reliability for advanced electronic packaging applications.

The thermal benefit must also be evaluated against RF degradation. Adding ceramic particles changes the effective permittivity according to filler volume fraction, morphology, and interfacial polarization. It can also alter surface roughness and local electromagnetic field distributions. Experimental dielectric characterization should therefore be performed at the actual operating frequency range rather than inferred from low-frequency measurements. This is particularly important because the influence of packaging materials on RF losses becomes increasingly significant as frequency rises.

The backside thermal path is equally important, as shown in Figure 6. For an embedded RF IC, the preferred architecture is often to minimize the thermal path through the electrically functional front side and instead transfer heat vertically through the die/package stack into a backside spreader. Cu/graphite or emerging Cu/diamond composites are particularly compelling for this role. Copper provides high thermal

conductivity and excellent manufacturability, while graphite contributes high in-plane phonon conductivity and reduces CTE. Such structures combine the solderability and mechanical robustness of copper skins with the high lateral thermal conductivity and reduced mass of graphite. Importantly for package integration, the copper exterior enables conventional solder attachment; experiments and simulations have shown substantially lower chip temperatures when a Sn solder interface is used compared with a polymer adhesive interface. The principal challenge is that graphite is strongly anisotropic and has poor intrinsic wetting with copper; therefore, interfacial engineering becomes a first-order design variable. Modeling and experiments on graphite-flake/Cu systems show that the thermal conductance of the Cu/graphite interface and the thickness of any reaction or coating layer can strongly affect the resulting effective thermal conductivity. Excessively thick interfacial layers can become thermal barriers. Experimental Cu-graphite-Cu spreaders with innovative processing techniques have demonstrated thermal conductance values of above 500 W/mK, while also showing lower density than copper and potentially resulting in lower interfacial stresses with active devices.

VII. Emerging Reliability Challenges and Opportunities in Heterogeneous Integration

Despite the significant advances, ensuring the reliability of future HI platforms remains challenging with continued scaling of interconnects to sub-micron dimensions and increasing integration density, and material diversity. Key challenges and research directions for enabling reliable future HI systems include [3]–[5], [12], [24], [25]:

- **Predictive Reliability:** Predicting reliability in HI packages remains challenging due to coupled and time-dependent nature of degradation mechanisms, the increasing influence of nanoscale interfaces and microstructural heterogeneity, and the limited availability of scale-appropriate material properties under realistic operating conditions.
- **Characterization and Multiscale Modeling:** Reliability assessment methods will require feature-size representative characterization, and physics-based multiscale modeling and predictive simulation frameworks that incorporate microstructural behavior.
- **Failure Analysis:** Rigorous reliability and failure analysis studies are required to ensure the long-term performance of HI packages with increasing material and interfacial complexity.
- **Functional Integration:** Nanoscale material architectures enable an optimal combination of system performance metrics without trading off one for the other. This becomes extremely crucial for embedded power and RF functions with advanced components that operate in complex embedded package environment.
- **Advances in Nanopackaging:** Mitigating nanoscale reliability challenges will rely on continued advances in nanopackaging technologies to support the development of future HI systems.

References

[1] B. Wunderle and B. Michel, "Progress in reliability research in the micro and nano region," *Microelectronics Reliability*, vol. 46, no. 9-11, pp. 1685–1694, 2006.

[2] S.-L. Jeng, J.-C. Lu, and K. Wang, "A review of reliability research on nanotechnology," *IEEE Transactions on reliability*, vol. 56, no. 3, pp. 401–410, 2007.

[3] M. R. Pulugurtha and A. Bonyár, "Packaging at nanoscale will advance future heterogeneous system integration [guest editorial]," *IEEE Nanotechnology Magazine*, vol. 18, no. 2, pp. 3–4, 2024.

[4] C. Bailey, "Reliability challenges for advanced packaging," in *2025 IEEE 43rd VLSI Test Symposium (VTS)*. IEEE, 2025, pp. 1–4.

[5] M. Manley, A. Victor, H. Park, A. Kaul, M. Kathaperumal, and M. S. Bakir, "Heterogeneous integration technologies for artificial intelligence applications," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 10, pp. 89–97, 2024.

[6] M. B. Hachemi, "Advanced packaging–A must for the next-gen AI and HPC hardware and not only!" in *2025 25th European Microelectronics and Packaging Conference & Exhibition (EMPC)*. IEEE, 2025, pp. 1–12.

[7] W. Do, J. Ju, M. Kim, I. Choi, S. Jin, M. Lee, H. Yang, and J. Jeong, "An embedded trace redistribution layer with rounded-bottom Cu geometry and Ti capping for enhanced electromigration reliability," *Micromachines*, vol. 17, no. 5, p. 604, 2026.

[8] F.-C. Shen, C.-Y. Huang, H.-Y. Lo, W.-Y. Hsu, C.-H. Wang, C. Chen, and W.-W. Wu, "Atomic-scale investigation of electromigration with different directions of electron flow into high-density nanotwinned copper through in situ HRTEM," *Acta Materialia*, vol. 219, p. 117250, 2021.

[9] Y. Zhang, Y. Yan, S. Vollebregt, and G. Zhang, "In situ analysis of copper microstructures in electromigration using sem-ebsd techniques," in *2024 IEEE 74th Electronic Components and Technology Conference (ECTC)*. IEEE, 2024, pp. 1317–1321.

[10] P. Ren, C. Liu, Y. Liang, S. Liu, and P. Du, "A finite element-based method for cohesive zone model parameter extraction in 2.5 D packaging interfaces," in *2025 26th International Conference on Electronic Packaging Technology (ICEPT)*. IEEE, 2025, pp. 1–5.

[11] K.-C. Chang, S.-C. Tseng, C.-H. Hsu, W.-H. Tu, C.-F. Han, J.-L. Wu, M.-J. Lii, C.-S. Chen, K. Yan, and J. He, "A novel fracture mechanics technique on studying passivation crack behavior for advanced Si package with aluminum redistribution layer (AL-RDL) routing," in *2025 IEEE 75th Electronic Components and Technology Conference (ECTC)*. IEEE, 2025, pp. 1–7.

[12] A. Bradicich, C. R. Allemang, S. Addamane, S. D. House, A. Chen, J. Yoo, E. Bussmann, C. M. Smyth, P. Maksymovych, M. Checa *et al.*, "Advancing microelectronics through nanoscale science: A perspective on needs and opportunities from the nanoscale science research centers," *Applied Physics Reviews*, vol. 12, no. 4, 2025.

[13] R. Gandhi, N. Poornabodha, P. Jithendrriyan, P. Srinivasan, A. Bharamgonda, C. Bailey, and A. Dasgupta, "Predicting redistribution layer (RDL) interfacial strength and delamination in fan-out wafer level packaging," in *2026 27th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*. IEEE, 2026, pp. 1–8.

[14] R. Zhang, K. Tang, J. Yuan, F. Wu, Y. Mao, and Y. Zhu, "Atomic-scale insights into electromigration in Cu interconnects via a new molecular dynamics approach," in *2025 26th International Conference on Electronic Packaging Technology (ICEPT)*. IEEE, 2025, pp. 1–5.

[15] S. Feng, L. Du, Z. Cui, X. Zhu, X. Fan, G. Zhang, and J. Fan, "Evaluating the electromigration effect on mechanical performance degradation of aluminum interconnection wires: A nanoindentation test with molecular dynamics simulation study," *Applied Surface Science*, vol. 676, p. 160992, 2024.

[16] D.-P. Tran, K.-P. Lee, H.-E. Lin, Y.-W. Hung, M.-P. La, and C. Chen, "Recent advances in nanostructured copper: From fabrication to applications," *Crystal Growth & Design*, vol. 26, no. 11, pp. 4374–4410, 2026.

[17] Z. Shi, Z. Wang, L.-Y. Gao, C. Zhong, P. Li, Z.-Q. Liu, and R. Sun, "Improving electromigration resistance of fine-pitch redistributed layer using graphene-doped twinned copper composites," *Advanced Engineering Materials*, vol. 26, no. 6, p. 2301649, 2024.

[18] A. Nisar, G. Al Duhni, C. Zhang, P. M. Raj, and A. Agarwal, "Reticular graphene reinforced copper for electromagnetic shielding application," in *2023 Fourth International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*. IEEE, 2023, pp. 1–5.

[19] M. PULUGURTHA, S. B. Venkatakrishnan, J. Volakis, and S. Rathnayaka, "Scalable electronics manufacturing with rigid tile panel embedding," Sep. 11 2025, uS Patent 12,702,025.

[20] T. Niu and A. Li, "From two-dimensional materials to heterostructures," *Progress in Surface Science*, vol. 90, no. 1, pp. 21–45, 2015.

[21] Y. Liu, Y. Huang, and X. Duan, "Van der waals integration before and beyond two-dimensional materials," *Nature*, vol. 567, no. 7748, pp. 323–333, 2019.

[22] L. Lindsay and D. Broido, "Enhanced thermal conductivity and isotope effect in single-layer hexagonal boron nitride," *Physical Review B—Condensed Matter and Materials Physics*, vol. 84, no. 15, p. 155421, 2011.

[23] E. Sichel, R. Miller, M. Abrahams, and C. Buiocchi, "Heat capacity and thermal conductivity of hexagonal pyrolytic boron nitride," *Physical review B*, vol. 13, no. 10, p. 4607, 1976.

[24] IEEE Electronics Packaging Society, "Heterogeneous integration roadmap," 2025. [Online]. Available: https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2025-edition/

[25] G. Refai-Ahmed, V. V. Zhirnov, S. Park, A. S. Helmy, B. Sammakia, K. Ghose, J. A. Ang, G. Bonilla, T. Mahdi, J. Wieser *et al.*, "New roadmap for microelectronics: Charting the semiconductor industry's path over the next 5, 10, and 20 years," in *2024 IEEE 26th Electronics Packaging Technology Conference (EPTC)*. IEEE, 2024, pp. 1260–1266.