Quantum Infrastructure for AI Applications

Packaging Challenges and Roadmap

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1. Executive Summary

The panel examined a central engineering question for the emerging quantum-computing industry: How can packaging evolve from supporting laboratory-scale processors to enabling reliable, modular, and manufacturable systems capable of supporting AI-related applications and other computationally demanding workloads? Across superconducting, trapped-ion, photonic, and topological platforms, the presentations reached a common conclusion: scaling is no longer solely a device-physics problem. It is a system-integration challenge governed by heat, signal density, loss, noise, control complexity, optical and electrical I/O, assembly yield, and supply-chain maturity.

The discussion highlighted distinct but complementary paths toward large-scale quantum systems. MIT Lincoln Laboratory described highly integrated approaches for superconducting and trapped-ion systems, including 3D superconducting integration, photonic routing, integrated detectors, and on-chip control electronics. IBM outlined a modular fault-tolerant roadmap in which processors containing hundreds of qubits are linked through sparse, meter-scale couplers and supported by scalable cryogenics, cryogenic CMOS (cryo-CMOS), dense superconducting wiring, and an increasingly mature foundry ecosystem. PsiQuantum presented a silicon-photonic path to utility-scale fault-tolerant computing based on high-volume semiconductor manufacturing, integrated optoelectronic packaging, modular cryogenic blades, and networked high-power cryogenic cabinets. Google Quantum AI emphasized the electrical performance, density, shielding, and yield needed to scale surface-code processors, while Microsoft Quantum described Majorana 2 and the materials-driven path toward compact, digitally controlled topological qubits.

Taken together, the presentations indicate that the packaging roadmap must progress beyond isolated demonstrations toward co-designed platforms with standardized interfaces, qualified materials and interconnects, modular serviceability, design kits, test vehicles, automated assembly, and manufacturing feedback. The ECTC community is well positioned to lead this transition because the required capabilities closely match its strengths in heterogeneous integration, advanced substrates, photonics, thermal engineering, reliability, and high-volume manufacturing.

2. Session Context and Objectives

Quantum processors offer the prospect of addressing selected problems that are intractable or prohibitively expensive for conventional architectures, including quantum chemistry, materials modeling, optimization, differential equations, and certain machine-learning workloads. Realizing practical value, however, will require quantum processors to operate as tightly integrated accelerators within classical high-performance computing and AI environments. These environments demand rapid data movement, low control latency, predictable quality of service, and efficient feedback among quantum hardware, real-time decoders, control electronics, and classical computing resources.

The session focused on the packaging technologies required to scale quantum hardware while preserving qubit fidelity, coherence, and overall system performance. Particular attention was given to cryogenic and thermal constraints, high-density, low-loss interconnects, integrated control and readout, electromagnetic isolation, modular architectures, manufacturability, and the transition from bespoke research hardware to qualified, scalable industrial supply chains.

3. Recommended Packaging Roadmap

Near term: Establish measurable building blocks

- Develop cross-platform test vehicles and standardized methods for insertion loss, thermal conductance, crosstalk, magnetic compatibility, optical coupling, connector repeatability, and assembly yield under cryogenic operating conditions.
- Advance cryogenic-compatible process design kits, multiphysics co-design, known-good-die screening, and qualification of materials, flex circuits, connectors, and bonding interfaces.

Midterm: Integrate modular subsystems

- Combine qubit, interposer, control/readout, amplification, photonic I/O, shielding, and thermal-management functions in repeatable module platforms with inline metrology and traceability.
- Validate module-to-module electrical and photonic links under realistic fidelity, latency, vibration, thermal-cycling, and uptime conditions, including repair and rework strategies.

Long term (beyond 2030): Deploy scalable infrastructure

- Scale to networked cryogenic cabinets or modular millikelvin systems with data-center-class monitoring, field-replaceable units, digital twins, and workload-specific qualification.
- Build a resilient industrial ecosystem based on multi-vendor foundry access, qualified second sources, capacity planning, workforce development, and stable procurement specifications.

4. Conclusions

The panel demonstrated that practical quantum computing will depend on packaging innovation as much as on advances in qubit technology. Although superconducting, trapped-ion, photonic, and topological technologies operate at different temperatures and use different signal modalities, they share the need for dense low-loss I/O, careful thermal design, integrated control and readout, shielding, modularity, manufacturing discipline, and a scalable supplier base.

The most important roadmap shift is from optimizing individual components to engineering complete, testable, serviceable, and replaceable quantum subsystems. Progress will require coordinated development of devices, packages, cryogenic infrastructure, classical control, software, facilities, and supply chains. ECTC participants can make a decisive contribution by converting promising quantum-hardware demonstrations into robust integration platforms that can be manufactured, deployed, serviced, and improved at scale.

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